GEH-6721_Vol_II_BL

Mark* VIe and Mark VIeS Control Systems

Volume II: General-purpose Applications

Dec 2018

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Revised: Dec 2018
Issued: Jan 2004

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Document Updates

Rev	Location	Description
BL	*UCSC Controllers*	Added content for *UCECH1B* module
		Added content for *Mark VIe UCSCH2x* controller
		Updated *UCSC Specifications* with correct UCSCH1, H2, and H3 Reliability MTBF hours
		Updated *UCSC Embedded Field Agent (EFA)* section with references to EFA-related documentation
		Updated *UCSC Embedded PROFINET Gateway (Embedded PPNG) Module* section with content for PROFINET system redundancy
	Controller Interoperability	New section to describe the Mark VIe Controller Interoperability feature
	UCSB LEDs and Connections	Changed Diag LED state description in the graphic from solid red to flashing red to indicate an active diagnostic alarm
	UCSA LEDs and Connections	
	UCCA Processor	
	UCCC Processor	
	Mark VIe PROFINET Gateway (PPNG) Module	Added Note stating content is not applicable to UCSC Embedded PPNG module
	PPNG Specific Alarms	Added Embedded PPNG *alarm 165*
BK	*UCSCH1x Controllers*	Added content for Embedded EtherCAT USCSH1C controller
		Added UCEC Power Adapter Cable to the table *UCSC Accessories*
	UCSC Embedded EtherCAT Controller	Added content for Embedded EtherCAT USCSH1C controller
	Controller Diagnostic Alarms	Added Embedded EtherCAT USCSH1C controller diagnostic alarms 2400–2410
	YAIC Compatibility	Updates for clarification and firmware version support
	YDIA Compatibility	
	YDOA Compatibility	
	YVIB Compatibility	Removed statement from Attention concerning YVIBS1A compatibility firmware version
BJ	Contents	Added Attention statement that users application may not be licensed to access full system capability and I/O types described in this document
	Mark VIeS YAIC Analog I/O Pack	Updated the input current configuration value for the last two inputs
	TRLYH1D, S1D Relay Output with Solenoid Integrity Sensing	Updated the following: • *TRLY_1D Block Diagram*: Updates specific for PDOA and YDOA I/O packs plug-ins and redundancy, and indicated TB3 should not be used • *TRLY_1D Compatibility*: Added IS420 versions of PDOA and YDOA I/O packs • *TRLY_1D Installation*: Removed irrelevant Caution statement, indicated TB3 should not be used, and updated the TRLY_1D Terminal Board Wiring drawing • *TRLY_1D Operation*: Updated *TRLY_1D Circuits (TMR)* drawing • *TRLY_1D Specifications*: Power solenoids and wiring updates • *TRLY_1D Diagnostics*: Removed monitoring of relay coil outputs and checks again frame rate, and removed contact voltage monitoring
	PFFA FOUNDATION Fieldbus Linking Device, *H1 Connections*	Added a Note that PFFA is not rating for Intrinsic Safety (IS) but IS is part of H1 standard, with reference to drawing 238A7779 for details
	PSCA Serial Communication Module, *Ethernet Modbus Master Service*	Updated the TCP/IP parameter for Read time-out
	JPDG Core Power Distribution	Updated the following: • *Compatibility*: Removed IS200JPDGH1 as the only version of JPDG • *JPDG Specifications*: Added temperature ratings for power inputs and outputs specs • *JPDG Control Power Distribution 28 V dc*: Added temperature ratings
	JPDD DC Power Distribution	Updated JPDDG4A fuse length
	Wetting Power Distribution 24/48 V dc	Added temperature ratings for JFA through JFG

Document Updates — continued

Rev	Location	Description
BH	PUAA, YUAA Universal I/O Modules, *PUAA Diagnostic Alarms*	Added the following diagnostic alarms: • Alarm 2819–2820, *Cold Junction Sensor [ ] failure* • Alarm 2821, *Cold Junction difference detected* • Alarm 2822, *Internal hardware issue detected (code[ ])*
	PUAA, YUAA Universal I/O Modules, *YUAA Diagnostic Alarms*	Added the following diagnostic alarms: • Alarm 2819–2820, *Cold Junction Sensor [ ] failure* • Alarm 2821, *Cold Junction difference detected* • Alarm 2822, *Internal hardware issue detected (code[ ])*
BG	*UCSC Mounting Requirements*	Replaced airflow diagram with separate airflow diagrams for 70°C and 65°C
	Mark VIe, Mark VIeS, and MarkStat UCSC Controllers	Added UCSCS2 controller for Mark VIeS Safety Control
		Added the section *Mark VIeS UCSCS2x Controllers*
	Mark VIe and Mark VIeS UCCx Controllers	Added this section with a note that Mark VIeS Safety Controller V05.03 is the most current version that supports the UCCx platform, which is installed from the ControlST DVD by selecting the ControlST Supplement Package installation option
	UCSC *UDH Network Configuration*	Added a Note to inform users that new UCSCs shipped from the factory do not include the software that supports communication from the PHY PRES button to the EFA. Users must download to the controller at least once to enable this functionality.
	UCSC Restore	
	ESWA and ESWB Industrial Unmanaged Ethernet Switches, *Available Form Factors*	Updated the list of available ESWx form factors
	PFFA FOUNDATION fieldbus Linking Device, *PPRAH1B Linking Device*	Updates to the section *Firmware Update* for bug fixes: • Updated the Note to state that passwords no longer reset to the default password if the Erase Linking Device Configuration button is checked. • Added Note stating that in the case of a power loss during firmware update, the PFFAH1B will return to its default factory image and the user should upgrade the firmware using the webpage
		Added a Note in the section *Set Password* stating that there is no method to reset the password to factory defaults
	PDOA, YDOA Discrete Output Modules, *TRLY* relay sections	Removed all reference to 240 V ac; it not a supported voltage
	YAIC Specifications	Updated the Scan Time specification with a Note that states that the update rate in the controller is based on the frame rate
	YHRA Specifications	
	PPRF PROFIBUS Master Gateway	Updates to PPRF PROFIBUS I/O pack section: • Number of supported slave devices • Number of extendable stations • Added the Total I/O Data Maximum specification
	PVIB, YVIB Vibration Monitor Modules	Added content throughout this chapter for the following terminal boards: • TVBAH1B (PVIB) • TVBAH2B (PVIB) • TVBAS2B (YVIB)
		Updated the ToolboxST Component Editor configuration setting range for *Filtrlpcutoff* in the table for *Vib 1-8*
		Added more headings to the *TVBA Compatibility* table to identify the different attributes included with each terminal board version
	PUAA, YUAA Universal I/O Modules	Added content throughout the chapter for Mark VIeS YUAA Universal I/O pack

Document Updates — continued

Rev	Location	Description
BG	PUAA, YUAA Universal I/O Modules, *PUAA Specifications*	Updated the PUAA specification SharedIONet to indicate that Shared IONet is supported
	PUAA, YUAA Universal I/O Modules, *PUAA Performance*	Updated the PUAA Discrete Inputs rating to include Sequence of Events tagging
		Updated the PUAA Discrete Outputs rating to indicate that Sequence of Events is not supported on analog outputs
	PUAA, YUAA Universal I/O Modules, *PUAA Operation*	Added this section to provide PUAA switch and channel configuration
	PUAA, YUAA Universal I/O Modules, *Pulse Accumulator*	Added this section to provide information on PUAA/YUAA support for simple Pulse Accumulator inputs
	PUAA, YUAA Universal I/O Modules, *PUAA_YUAA Diagnostic Alarms*	Added the *Outputs Disabled* alarm (2818)
	BPPx Processor LEDs	Updated the table names for clarification and added Red ATTN flashing pattern for 4 Hz pulses every 4 sec to both tables
	PUAA, YUAA Universal I/O Modules, YUAA Specific Diagnostic Alarms	Added the diagnostic alarm that is specific to only the YUAA I/O pack
	PUAA, YUAA Universal I/O Modules, *External Wetted Contact Inputs*	Updated PUAA/YUAA external wetted contact inputs field voltage sources to 20 V
	Throughout the document	Added support for Modbus for the Mark VIeS Safety controller
	PVIB or YVIB Specific Diagnostic Alarms	Updated diagnostic alarm 65 to include possible cause as power failure on terminal boards
BF	*Mark VIe and Mark Stat UCSC Controllers*	Replaced UCSC photos to reflect updated faceplate and functionality
		Added the section *Virtual Network* to describe how the virtual network transfers data between the virtual machines (VMs) in the UCSCH1 controller
	UCSC LEDs	Updated the Boot LED indication in the LED illustration for UCSC, UCSB, and UCSA, which flashes once every three seconds to indicate Baseload signature verification failure
	UCSB LEDs and Connections	
	UCSA LEDs and Connections	
	ESWA and ESWB Industrial Unmanaged Ethernet Switches Installation	Updated the orientation of the DIN-rail clips in the table of DIN-rail clips qualified for use with ESWx switches
	YAIC Compatibility	Added a bullet to the compatibility section to make the user is aware that ControlST includes versions of firmware that support both S1A and S1B I/O packs
	YDIA Compatibility	
	YDOA Compatibility	
	YVIB Compatibility	
	Controller Setup and Download	Moved the procedures from this section to the *ToolboxST User Guide for Mark Controls Platforms* (GEH-6703)
	Embedded PROFINET Controller Specifications	Removed the statement from PROFINET Network Speed table item that IONet must be on a separate switch; this is no longer true
	PDII/ SDII Operation, *Voltage Ranges for Parallel Resistor Configuration*	Added a Note concerning AC sensors acting as switches causing voltage to drop below wetting range when using a parallel resistor for measurement
	TDBS Terminal Board for Simplex Discrete I/O *Configuration* and SRLY + WROG *Configuration*	Removed relay specific fuse information related to dry contacts to reduce confusion on WROGH1 functionality
	TVBA Seismic Sensors	Updated the Seismic Sensor illustration and changed the position of the JPxC jumper to PCOM to allow the corresponding buffered output to be scaled the same as the signal input
	PPRAH1B Linking Device	Added this section containing details for PPRAH1B (this module replaces PPRAH1A, which is obsolete)
	PFFA Configuration Parameters	Moved this section to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703), the section *PFFA Configuration Parameters*

Document Updates — continued

Rev	Location	Description
BF	*PPRF PROFIBUS Master Gateway*	Added parameter *SetDiagOnExtDiag* with a description to the *Parameters and Online Loads* table in the section *Configuration*
	PUAA Universal I/O Module, *PUAA Analog Inputs (Voltage or mA Current)*	Revised the diagram *Analog Inputs* to clarify that HART is not supported with externally powered devices.
BE	*Replacing a PFFA Linking Device*	Added a Note to notify the user that PFFA will not be online until the Inputs Enabled or Controlling state is reached after reboot
	Controllers and Unmanaged Switches	New platform, *Mark VIe and Mark Stat UCSC Controllers*
	Common Controller Diagnostic Alarms	Update to *Alarm 542*
	YVIB	Updated the table, *YVIB Supported Sensor Inputs*
	The Chapter, PVIB and YVIB	*Vib1 - 8*: changed Fltrlpcutoff max. limit from 42300 to 4300 *Gap 1 - 3*: added a footnote regarding Vib_Type4 = VibLMAccel PVIB or YVIB Diagnostic Alarms update to *Diagnostic Alarms 33-45*
	PUAA Universal I/O Module	Updates for phase II, includes HART, digital I/O, and pulse accumulators
BD	*PVIB* and *YVIB*	Added info on PVIBH1B and YVIBS1B, including the following new sections: *Vibration Monitoring Overview*, *PVIB or YVIB Functions*, *TVBA Installation, Operation, and Jumper Configuration*, *PVIB I/O Pack Replacement*, *YVIB I/O Pack Replacement*
	PUAA	A new universal analog I/O module
	PCNO	Added support for the Woodward Liquid DLE Fuel Metering System (LFMS)
	UCSA	An available Mark VIe controller platform (moved information from GEH-6721_Vol_III into this manual)
	How to Set Up and Download to the Controllers	Moved these procedures from GEH-6808 into this manual, and updated the procedures to make them more user friendly
	How to Perform an Initial Download to the I/O Modules	
	PRTD	New section, *RTD Excitation Signal*
	Mark VIeS Black Channel	Added this section from GEH-6723
	PDOA or YDOA Component Editor	Updated to be in sync with GEH-6723

Document Updates — continued

Rev	Location	Description
BC	PDIA	Corrected *Compatibility*, redundancy options. Corrected *Specifications*, Ambient Rating. Corrected *Parameters*. Updated PDIA and YDIA *Variables*.
	YDIA	Changed graphic to be the *BPPC faceplate version* and updated overview graphic with searchable text. Corrected the redundancy options in the *Compatibility* section. YDIA *Configuration* section is now the same as with PDIA Configuration section. YDIA *Specific Alarms* are now the same as with PDIA Specific alarms. Updated PDIA and YDIA *Variables*.
	TBCI	Updated *Installation* for Dual packs. Added note for Dual packs to the figure, *TBCI Wiring and Cabling*. Updated Fault Detection *Specification*. Updates to the *Diagnostics* section. Updated Fault detection in I/O board *Specification*.
	TICI	Updated *Installation* for Dual packs. Updated *Diagnostics*.
	STCI	Updated Fault detection in I/O board, *Specification*. Updated *Diagnostics*.
	SRLY, *TDBS*, and *TDBT*	When using WROB, WROF, or WROG, the incoming wetting voltage can be either ac or dc.
	SRLY, *TDBS*	Added compatibility for WROF and WROG feedback voltages
	PHRA and *YHRA*	Added instructions for how to unlatch diagnostics 123–135
	I/O Pack Replacement	Removed Attention regarding incorrect firmware during download as this is not a problem of the I/O pack functionality, and this information is provided in the ToolboxST Download Wizard help.
	SDII	Added info on SDIIH2A version
	JPDG	Added info on JPDGH2A version
	PAOC	Updated the table, *PAOCH1A Derating*
	PAIC and YAIC	Added info on *PAICH1B* and *YAICS1B*. Corrected all instances of jumper names.
	Replace Mark VIeS Safety I/O Packs	New section provides replacement procedure for Mark VIeS Safety I/O packs
	YDOA	Updated *Compatibility* section
	PRTD	Updated the Specification for *Scan time*.
	UCPA	*UCPA Performance and Limitations*, updated to state that FOUNDATION Fieldbus is not supported

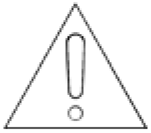
Document Updates — continued

Rev	Location	Description
bb	*PPNG*	New section, *Variables* Specifications, added *PROFINET Network Speed*, and *Conformance Class* Updated *Required ID Assembly for PROFINET Licensing* *Performance Limits*, added information on update rates Removal of Reason codes from *diagnostic alarms*. *Compatibility*, online downloads are supported with ControlST V06.00
	UCPA	Limit of six distributed I/O pack connections at 20 ms frame period New parameter, *LatchedPulseAcc1AtPulse2* *Limitations* — does not have a real-time clock
	Common I/O Module	New section, *TBSW Terminal Board Disconnect Switch* Updated the Attn Led Flash codes table titles to reflect processor type
	SRSA	Updated to provide the remainder of instructions to coincide with initial hardware release
	PPRF	Changes to allow 20 ms frame period with PPRFH1A, but with caution as a not recommended configuration
	JPDF	Updated the figures: *JPDF Electrical Diagram*, *JPDF Mechanical Board Layout* Updated *JPDF Connections* for G01 and G02 differences Updated the fuses in the section, *Specifications* Fixed part number for *DACA* New sections: *JPDF I/O Characteristics*, *JPDF Application Notes*
	PHRA	Added note regarding *Hart_CtrlVars*
	YHRA	Added note regarding *Hart_CtrlVars*, and also corrected various parameter names to match what is displayed from the ToolboxST application.
	PAIC	Updated *Specifications* for AI types and noise suppression
	TBAI	Updated *Specifications* for AI types
	STAO	In the section, *Installation*, fixed descriptions of H1 and H2 board revisions
	Controller Diagnostics	New alarms: *375*, *546*, and *547*
	TDBT	Updated Specification for *Max load current*
	JPDC	Fixed part number for *DACA* New section, *JPDC I/O Characteristics*
	Ordering Parts	Added reference to GEH-6721_Vol_I, the new *Component Part Numbers* section
	PDOA, YDOA Discrete Output Modules	Added information on the BPPC form of the YDOA I/O pack Updated specific alarms to be the same for PDOA and YDOA Updated configuration to be the same for PDOA and YDOA
	JPDC	Added additional *specification* information for *28 V dc control power distribution*
	Replacing S-type Boards	Fixed procedure for removable terminal blocks

Document Updates — continued

Rev	Location	Description
bb	JPDB	Added to *Application Notes* section, and new section: *PPDA Configuration for JPDB*
	JPDE	Updates to section, *Functional Description* New section, *JPDE I/O Characteristics*
	JPDM	Updates to section, *Functional Description* New sections: *JPDM I/O Characteristics*, *JPDM Application Notes*
	JPDS	Updates to section, *Functional Description* New sections: *JPDS I/O Characteristics*, *JPDS Application Notes*
	PPDA	New sections: *Compatibility*, *Signal Input*, *PPDA LED Control*
	DACA	New section, *DACA Application Notes*
	VCMPS	Added more information to section *introduction*
	SDII	Correction to *channel 13* of the table, *SDII Field Terminal Definitions*.
	TBCI	Updated the table in the section, *Compatibility* and removed the legacy board revisions where not appropriate.
	STAI	Updated *Specifications* for AI types, added S3A board revision
	SAII	Updated *Specifications* for AI types
	Various	The following component's specification was expanded to –40 to 70°C for ambient temperate rating: ESWA, PAICH1B, PAOCH1B, PDIAH1B, PDIIH1B, PDIOH1B, PDOAH1B, PHRAH1B, PRTDH1B, PSCAH1B, PTCCH1B, PPDAH1B, DACA, JPDA, JPDB, JPDC, JPDD, JPDE, JPDF, JPDG, JPDH, JPDL, JPDM, JPDP, JPDS, JGND
	PSCA	To explain limitations with RS-422 mode, updated *Specifications* and *Serial Modbus Master Service*, and SSCA *Specifications* sections.
	PCNO	Updated to include support for Moog valves
	YTCC	Updated the graphic for *TMR redundancy*, the graphic in *YTCC Analog Input Hardware*, the *YTCC Thermocouple Limits*, the *YTCC Cold Junctions* limit, and many of the *YTCC Configuration* parameters.
	TBTC	Updated the *TBTC Specification* for Cold junction compensation.
	STTC	Updated the graphic in the section, *STTC Operation*
	TDBS	Removed the rating information from the section, *TDBS Relay Outputs* because it is accurate as listed in Specifications section.
	I/O Module Common Alarms	Added alarms *348*, *349*, and *350*
	Password Protection	New feature for Mark VIe controllers
	TRLY_ID	Update to the figure, *TRLY_1D Solenoid Fault Announcement*

Safety Symbol Legend

 Warning	**Indicates a procedure or condition that, if not strictly observed, could result in personal injury or death.**
 Caution	**Indicates a procedure or condition that, if not strictly observed, could result in damage to or destruction of equipment.**
 **Attention**	**Indicates a procedure or condition that should be strictly followed to improve these applications.**

Control System Warnings

Warning

To prevent personal injury or damage to equipment, follow all equipment safety procedures, Lockout Tagout (LOTO), and site safety procedures as indicated by Employee Health and Safety (EHS) guidelines.

Warning

This equipment contains a potential hazard of electric shock, burn, or death. Only personnel who are adequately trained and thoroughly familiar with the equipment and the instructions should install, operate, or maintain this equipment.

Warning

Isolation of test equipment from the equipment under test presents potential electrical hazards. If the test equipment cannot be grounded to the equipment under test, the test equipment's case must be shielded to prevent contact by personnel.

To minimize hazard of electrical shock or burn, approved grounding practices and procedures must be strictly followed.

Warning

To prevent personal injury or equipment damage caused by equipment malfunction, only adequately trained personnel should modify any programmable machine.

Warning

Always ensure that applicable standards and regulations are followed and only properly certified equipment is used as a critical component of a safety system. Never assume that the Human-machine Interface (HMI) or the operator will close a safety critical control loop.

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Notes

Attention

The information in this document applies to the overall Mark VIe control system or Mark VIeS Functional Safety control system products; however, your application may not be licensed to access full system capability and I/O packs as described in this document. For example, the Mark VIeS Functional Safety control system for General Markets only utilizes the following I/O packs:

- **Analog I/O (YAIC)**
- **Universal Analog (YUAA)**
- **Vibration Input Monitor (YVIB)**
- **Relay Output (YDOA)**
- **Discrete Contact Input (YDIA)**
- **Power Distribution System Diagnostics (PPDA)**
- **Serial Modbus Communication (PSCA)**
- **Mark VIeS Safety Controller (UCSCS2x)**
- **Mark VIe Controller for Gateway (UCSCH1x)**

Notes

1 Controllers and Unmanaged Switches

1.1 UCSC Controllers

UCSC controllers are compact, stand-alone controllers that run application-specific control system logic used in a diverse range of applications, such as wind turbines, gas and steam turbines, and combined-cycle power plants.

The UCSC controller offers the following advantages:

- Single module
- No battery
- No fan
- No jumper settings required
- Flash memory can be conveniently updated
- Can be expanded to include seven additional I/O ports

The UCSC controller mounts in a panel and communicates with I/O modules through on-board I/O network (IONet), PROFINET, EtherCAT, High-speed Serial Link (HSSL) and/or other interfaces.

IS420UCSCH1A, IS420UCSCH2A, IS420UCSCS1A
See GEH-6725 for instructions /
Voir GEH-6725 pour obtenir des instructions
Power Supply: 28 VDC ⎓ 1.1 A
Ta: -40°C to 70°C
Engineering Sample
GENERAL ELECTRIC
2500 Austin Drive
Charlottesville, VA 22911 USA
IS420UCSCH2A-PR4
UD7K01R
Made in Germany

UCSC Controller Data Name Plate

Note For additional information, refer to the following documents:

• *Mark VIe and Mark VIeS Control Systems, Volume I System Guide* (GEH-6721_Vol_I)

• *ToolboxST User Guide for Mark Controls Platform* (GEH-6703)

• *UCSC Installation and Maintenance Requirements (IMR)* (GFK-3006)

• *ControlST Software Suite Release Notes* (GEI-100746)

1.1.1 UCSCH1x Controllers

The UCSCH1x controller is available in the standard three I/O port configuration and a 10 I/O port configuration. The 10 I/O port configuration, UCECH1x, consists of a standard UCSCH1x controller coupled with a seven I/O port expansion board.

1.1.1.1 Mark* VIe UCSCH1x Controller

The Mark VIe UCSCH1x quad core controller uses real-time hypervisor technology and QNX® Neutrino, a real-time, multi-tasking operating system (OS), to run the following virtual machines, depending on the platform configuration:

- The UCSCH1B controller is designed for high-speed, high-reliability industrial applications.
- The UCSCH1A Embedded PROFINET® Gateway (Embedded PPNG) module allows communication with PROFINET I/O devices, including RSTi-EP Slice I/O.
- The UCSCH1C Embedded EtherCAT® controller enables communications with EtherCAT I/O devices, including RSTi-EP Slice I/O. Line and Ring topologies are supported.
- Embedded Field Agent (EFA) technology is used to apply Predix™ cloud-based applications and/or locally hosted web applications over a secure connection and deliver real-time data.

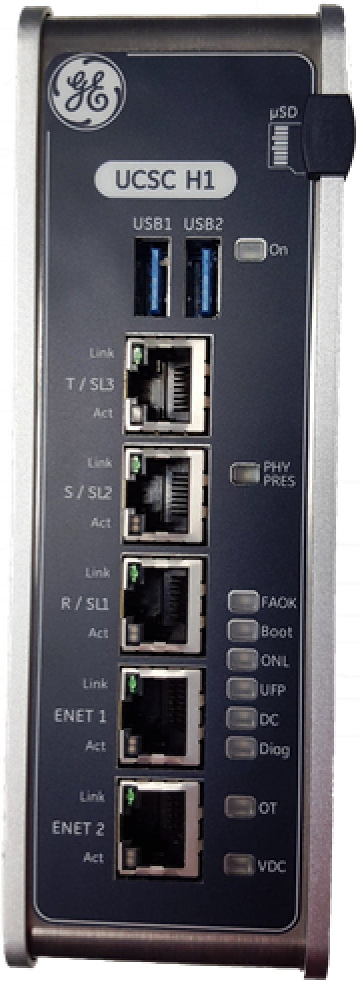
The UCSCH1x controller is loaded with software specific to its application. As a turbine or balance of plant (BoP) controller, it runs the Mark VIe firmware and applications and utilizes IONet interfaces. IONet is a private special-purpose Ethernet that only supports Mark controls I/O packs and controllers. IEEE 1588 protocol is used through the IONet interfaces to synchronize the clock of the I/O modules and controllers to within ±100 microseconds. External data is transferred to and from the control system database in the controller over the IONet interfaces. This includes process inputs/outputs to the I/O modules. Unlike traditional controllers where I/O is on a backplane, the UCSC controller does not host any application I/O. In a redundant set, all I/O networks are attached to each controller, providing them with all input data. This hardware and software architecture guarantees that no single point of application input is lost if a controller is powered down for maintenance or repair.

The UCSCH1x is available beginning with ControlST V07.01, and supports Simplex, Dual, and Triple Modular Redundant (TMR) redundancy.

The UCSCH1C is available beginning with ControlST V07.03, and supports Simplex redundancy only.

UCSCH1 Platform Configuration Supported Features

Platform	Embedded PPNG	Embedded EtherCAT	EFA
UCSCH1A	✓	X	✓
UCSCH1B	X	X	✓
UCSCH1C	X	✓	✓



Mark VIe UCSCH1x Controller

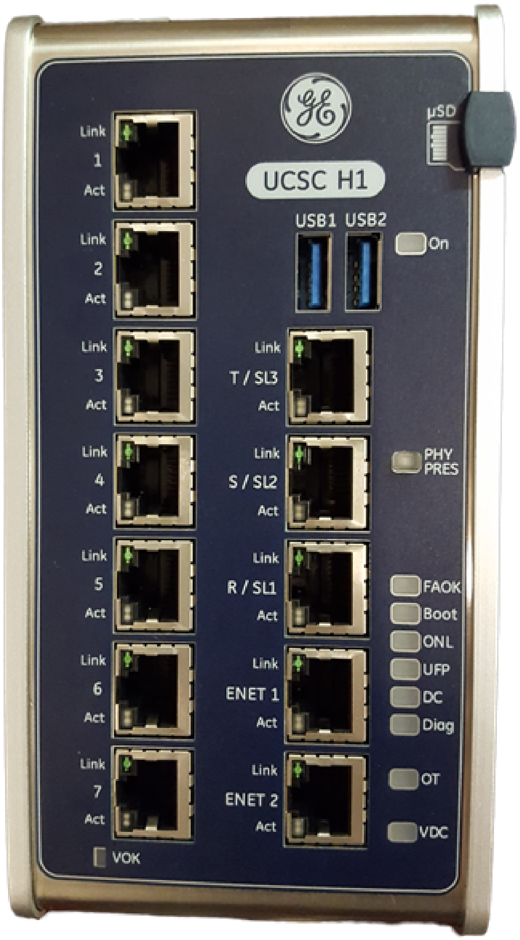
1.1.1.2 UCECH1x I/O Port Expansion Module

The UCECH1x module is a UCSCH1x controller coupled with a seven I/O port expansion board. The UCSCH1x controller contained within the UCECH1x module has the same features and benefits as the stand-alone UCSCH1x controller. The controller is loaded with software specific to its application.

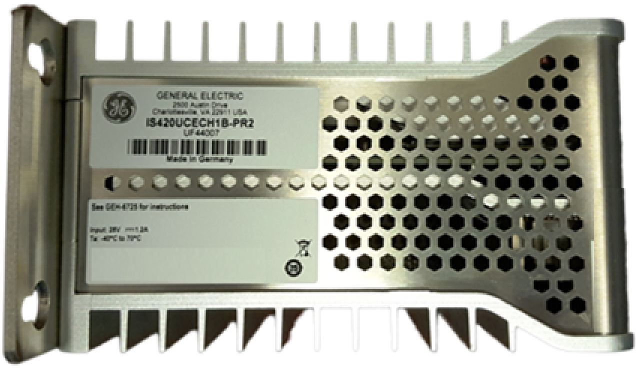
The UCECH1x is available beginning with ControlST V07.03, and supports Excitation control applications.

UCECH1x Module and Platform Configuration Supported Features

Module	Platform	Expansion I/O Ports	Embedded PPNG	Embedded EtherCAT	EFA
UCECH1B	UCSCH1x	7, RJ-45	X	X	✓



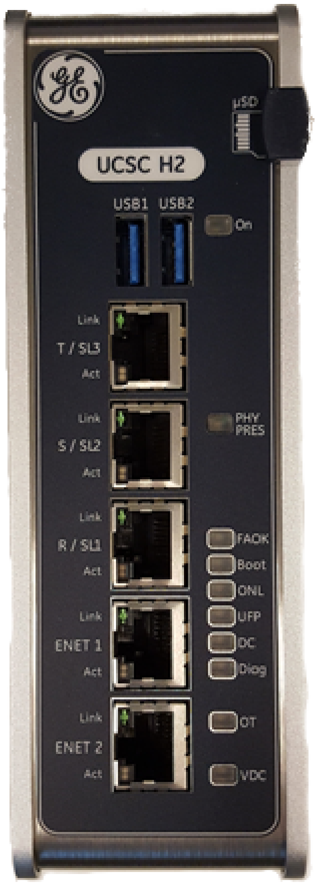
UCECH1x Module



Example UCEC Data Name Plate

1.1.2 UCSCH2x Controllers

The UCSCH2 dual core controller is available in the standard three I/O port configuration.



UCSCH2x Controller

1.1.2.1 Mark VIe UCSCH2x Controller

The Mark VIe UCSCH2A dual core controller running on QNX Neutrino, a real-time, multi-tasking operating system (OS), is designed for high-speed, high-reliability industrial applications.

The controller is loaded with software specific to its application. As a turbine or balance of plant (BoP) controller, it runs the Mark VIe firmware and applications and utilizes IONet interfaces. IONet is a private special-purpose Ethernet that only supports Mark controls I/O packs and controllers. IEEE 1588 protocol is used through the IONet interfaces to synchronize the clock of the I/O modules and controllers to within ±100 microseconds. External data is transferred to and from the control system database in the controller over the IONet interfaces. This includes process inputs/outputs to the I/O modules. Unlike traditional controllers where I/O is on a backplane, the UCSC controller does not host any application I/O. In a redundant set, all I/O networks are attached to each controller, providing them with all input data. This hardware and software architecture guarantees that no single point of application input is lost if a controller is powered down for maintenance or repair.

The UCSCH2A controller is available beginning with ControlST V07.04, and supports Simplex, Dual, and TMR redundancy.

UCSCH2 Platform Configuration Supported Features

Platform	Embedded PPNG	Embedded EtherCAT	EFA
UCSCH2A	N/A	N/A	N/A

1.1.2.2 MarkStat UCSCH2x Controller

The MarkStat UCSCH2A dual core controller running on QNX Neutrino, a real-time, multi-tasking operating system (OS), runs the MarkStat Power Conversion applications. It is loaded with software specific to its applications.

The UCSCH2A controller communicates with the wind turbine control system and applications through the IONet interface. External data is transferred to and from the control system database in the controller over the IONet interface. The MarkStat UCSC communicates with the bridge interface modules through three high-speed serial link (HSSL) connections, and communicates with the ToolboxST application over UDH.

The UCSCH2A controller is available beginning with ControlST V07.01, and supports only the Simplex configuration.

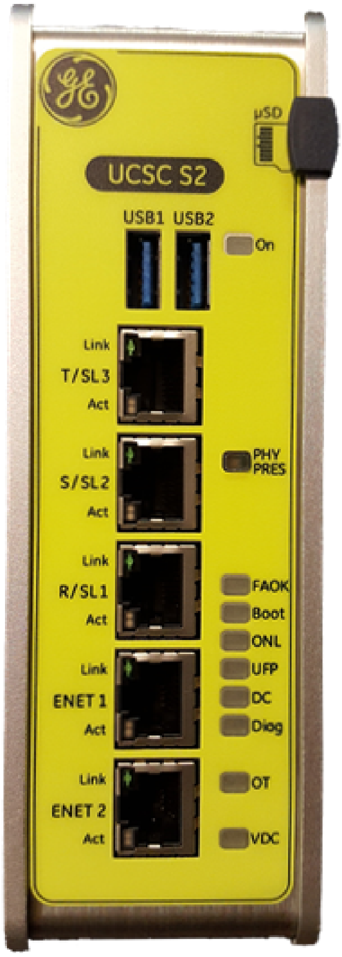
UCSCH2 Platform Configuration Supported Features

Platform	Embedded PPNG	Embedded EtherCAT	EFA
UCSCH2A	N/A	N/A	N/A

1.1.3 UCSCS2x Controllers

The UCSCS2 dual core controller runs the Mark VIeS Safety control applications used for functional safety loops to achieve SIL 2 and 3 capabilities. Mark VIeS Safety equipment is used by operators that are knowledgeable in safety-instrumented system (SIS) applications to reduce risk in critical safety functions. Safety controllers and distributed I/O modules are specifically programmed for safety control use, and this specific control hardware and software is compliant with the IEC 61508 certification. The Mark VIeS Safety controller runs on QNX Neutrino, a real-time, multi-tasking operating system (OS).

The UCSCS2A is available beginning with ControlST V07.02, and supports Simplex, Dual, and TMR redundancy.



Mark VIeS Safety UCSCS2x Controller

1.1.4 UCSC Specifications

1.1.4.1 UCSC Specifications

Item	UCSC Specification
Microprocessor	IS420UCSCH1: quad core, 1.2 GHz AMD G-Series IS420UCSCH2: dual core, 1.6 GHz AMD G-Series IS420UCSCS2: dual core, 1.6 GHz AMD G-Series
Memory	IS420UCSCH1: 4 GB DDR3-1333 SDRAM IS420UCSCH2: 2 GB DDR3-1066 SDRAM IS420UCSCS2: 2 GB DDR3-1066 SDRAM
NVSRAM	Supports 3067 nonvolatile program variable, 338 forces, and 64 totalizers *Not supported by the Mark VIeS Safety control*
Ports	• 5 Ethernet ports on front panel (Refer to the section *Interface Details*.) • 1 Ethernet port on bottom used for connectivity to Predix • 2 USB ports only used to initially set up UDH network IP address or for restore function • 1 COM port is 115200 bit/s, 8N1, RJ-45 connector, no Flow-Control, serial redirection of UEFI-setup, and typically used by GE for troubleshooting in field • 1 Display Port (disabled after startup) • 1 microSD (not currently supported)
LEDs	Refer to the section *LEDs*.
Input Power	Refer to the section *Power Requirements*.
HMI	ControlST* Software Suite V07.00.00C or later
Programming	Control block language with analog and discrete blocks; Boolean logic represented in relay ladder diagram format. Supported data types include: • Boolean • 16-bit signed integer • 16-bit unsigned integer • 32-bit signed integer • 32-bit unsigned integer • 32-bit floating point • 64-bit long floating point
Dimensions	UCSC: 168 x 150 x 55 mm (6.61 x 5.90 x 2.17 in) (H x D x W) UCSC with mounting: 204 x 152 x 55 mm (8.03 x 5.99 x 2.17 in) (H x D x W)
Weight	1,327 g (46.8 oz)
Mounting	Refer to the section *Mounting Requirements*.
Cooling	Convection
Operating temperature	-40 to 70 °C (-40 to 158 °F), ambient 25 mm (0.98 in) from any point on UCSC
Storage Temperature	-40 to 85 °C (-40 to 185 °F)
Humidity	95% non-condensing
Altitude	Normal Operation: 0 to 1,000 m (0 to 3281 ft) at 101.3 to 89.8 kPa Extended Operation: 1,000 to 3,000 m (3281 to 9,843 ft) at 89.8 to 69.7 kPa; requires temperature derating up to 3000 m (9,843 ft) = 65°C (149 °F) max
Reliability MTBF at 30°C (86 °F)	IS420UCSCH1: 414,248 hours IS420UCSCH2: 417,821 hours IS420UCSCS2: 417,821 hours
ECCN US Classification	Can be supplied upon request
Certifications	Refer to the section *Agency Certifications and Standards*.

1.1.4.2 UCEC Module Specifications

Note All specifications provided in the table *UCSC Specifications* are also applicable to the UCEC module, with the following exceptions.

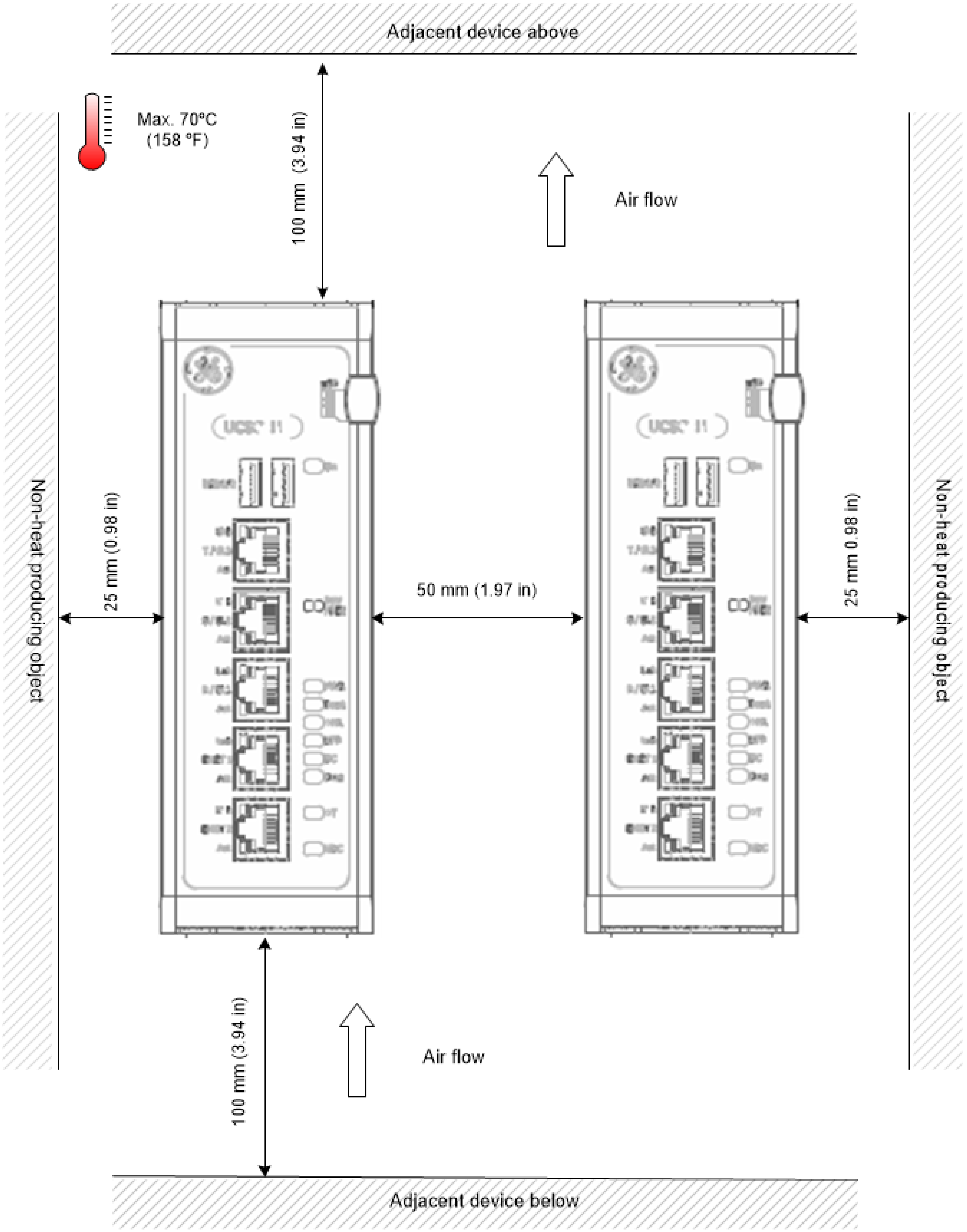
Item	UCEC Module Specification
Ports	7 expansion I/O ports (in addition to all UCSCH1x ports listed in *UCSC Specifications* table) Refer to the section *Interface Details*.
LEDs	Refer to the section *LEDs*.
Input Power	Refer to the section *Power Requirements*.
HMI	ControlST* Software Suite V07.03.00C or later
Dimensions	UCEC: 168 x 150 x 85 mm (6.61 x 5.91 x 3.35 in) (H x D x W)
	UCEC with mounting: 204 x 153 x 85 mm (8.03 x 6.02 x 3.35 in) (H x D x W)
Weight	2,060 g (72.7 oz)
Mounting	Refer to the section *UCEC Module Mounting Requirements*.
Cooling	Convection
Operating temperature	-40 to 70 °C (-40 to 158 °F), ambient 25 mm (0.98 in) from any point on UCEC
Storage Temperature	-40 to 85 °C (-40 to 185 °F)
Humidity	95% non-condensing
Altitude	Normal Operation: 0 to 1,000 m (0 to 3281 ft) at 101.3 to 89.8 kPa Extended Operation: 1,000 to 3,000 m (3281 to 9,843 ft) at 89.8 to 69.7 kPa; requires temperature derating up to 3000 m (9,843 ft) = 65°C (149 °F) max
Reliability MTBF at 30°C (86 °F)	IS420UCECH1: 329,615 hours
Certifications	Refer to the section *Agency Certifications and Standards*.

1.1.5 UCSC Mounting and Installation Requirements

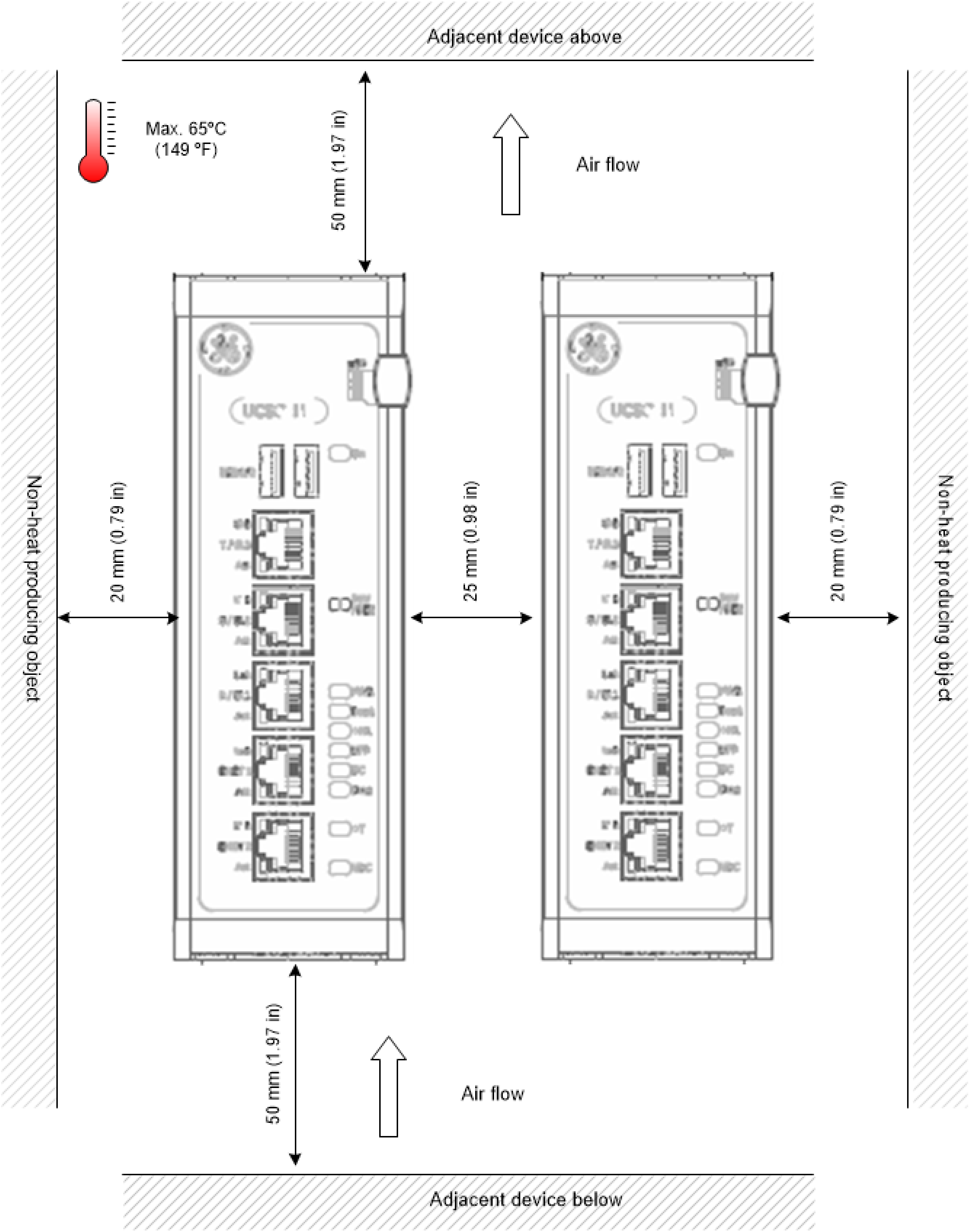
1.1.5.1 UCSC Mounting Requirements

The following are requirements for mounting the UCSC controller:

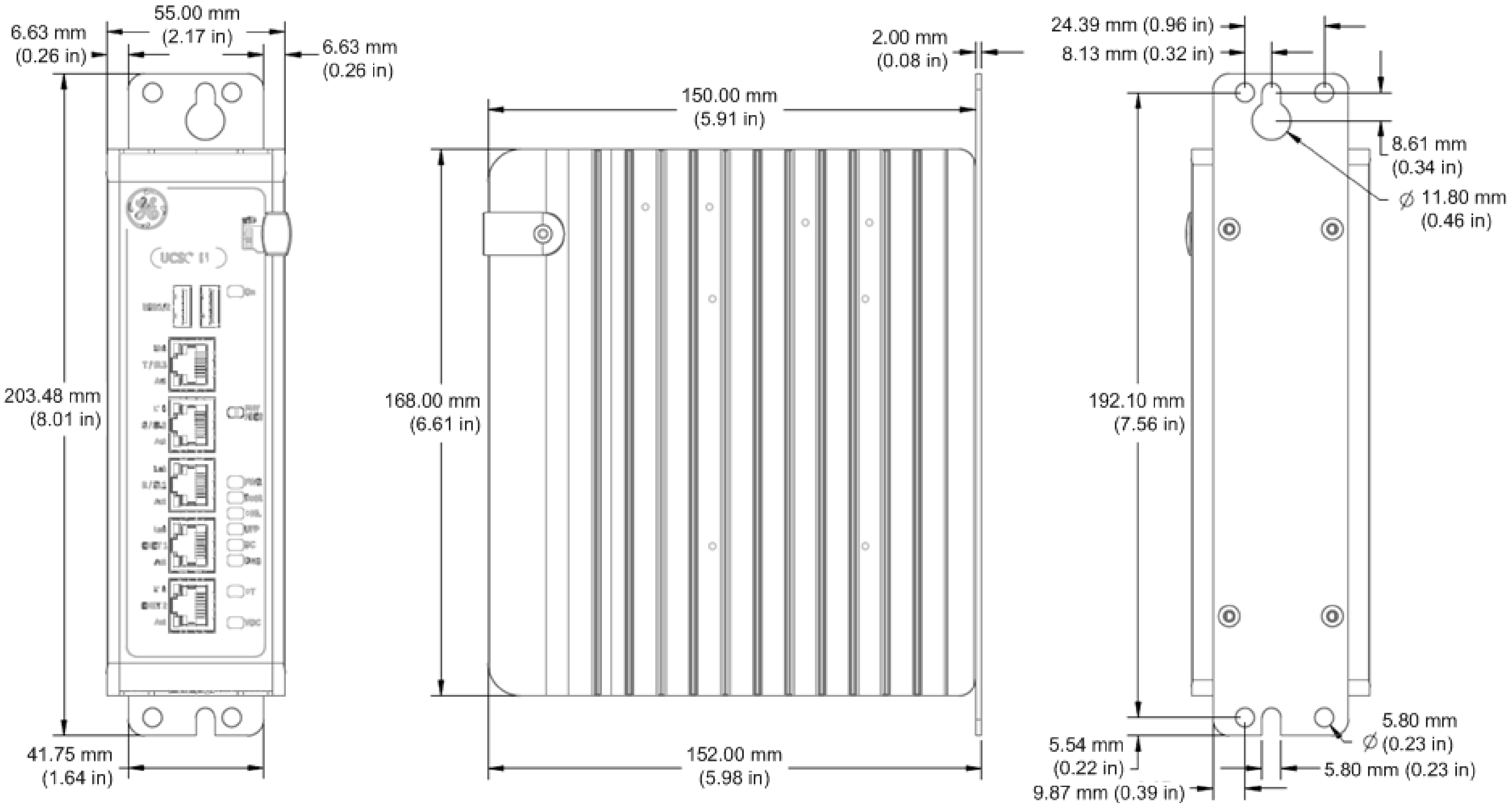
- Directly mount the UCSC to the mounting base using the two mounting screws.
- Vertical mount with unobstructed air flow through fins.
- Leave a minimal 100 mm (3.94 in) air gap above and below the UCSC.
- Parallel mount UCSC to UCSC requires a minimal 50 mm (1.97 in) spacing to achieve full temperature rating.
- The *operating temperature* envelope is 25 mm (0.98 in) from any point on UCSC.



UCSC Mounting Requirements to Achieve 70ºC Operating Temperature



UCSC Mounting Requirements to Achieve 65ºC Operating Temperature

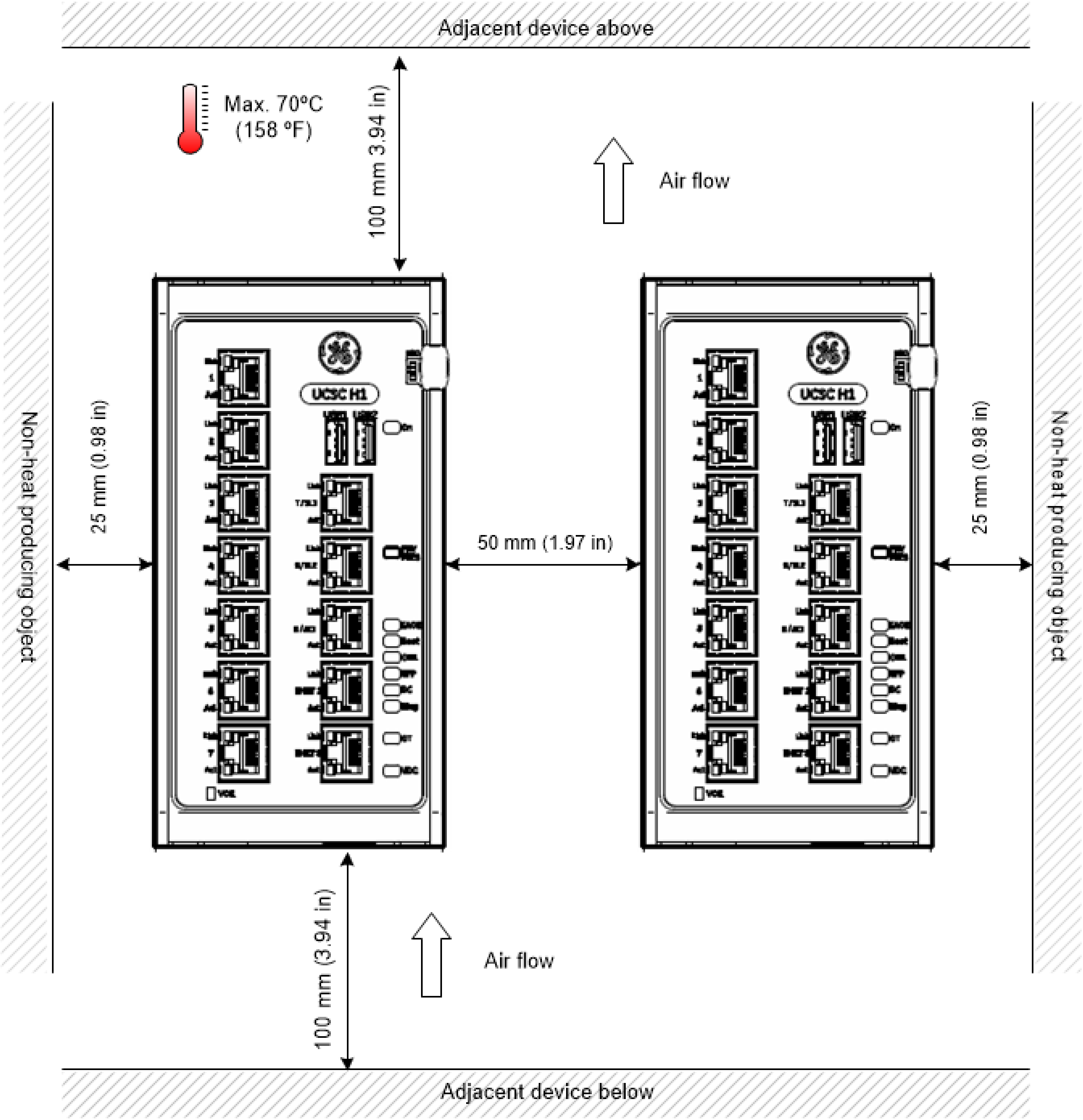


UCSC Controller Mounting Dimensions

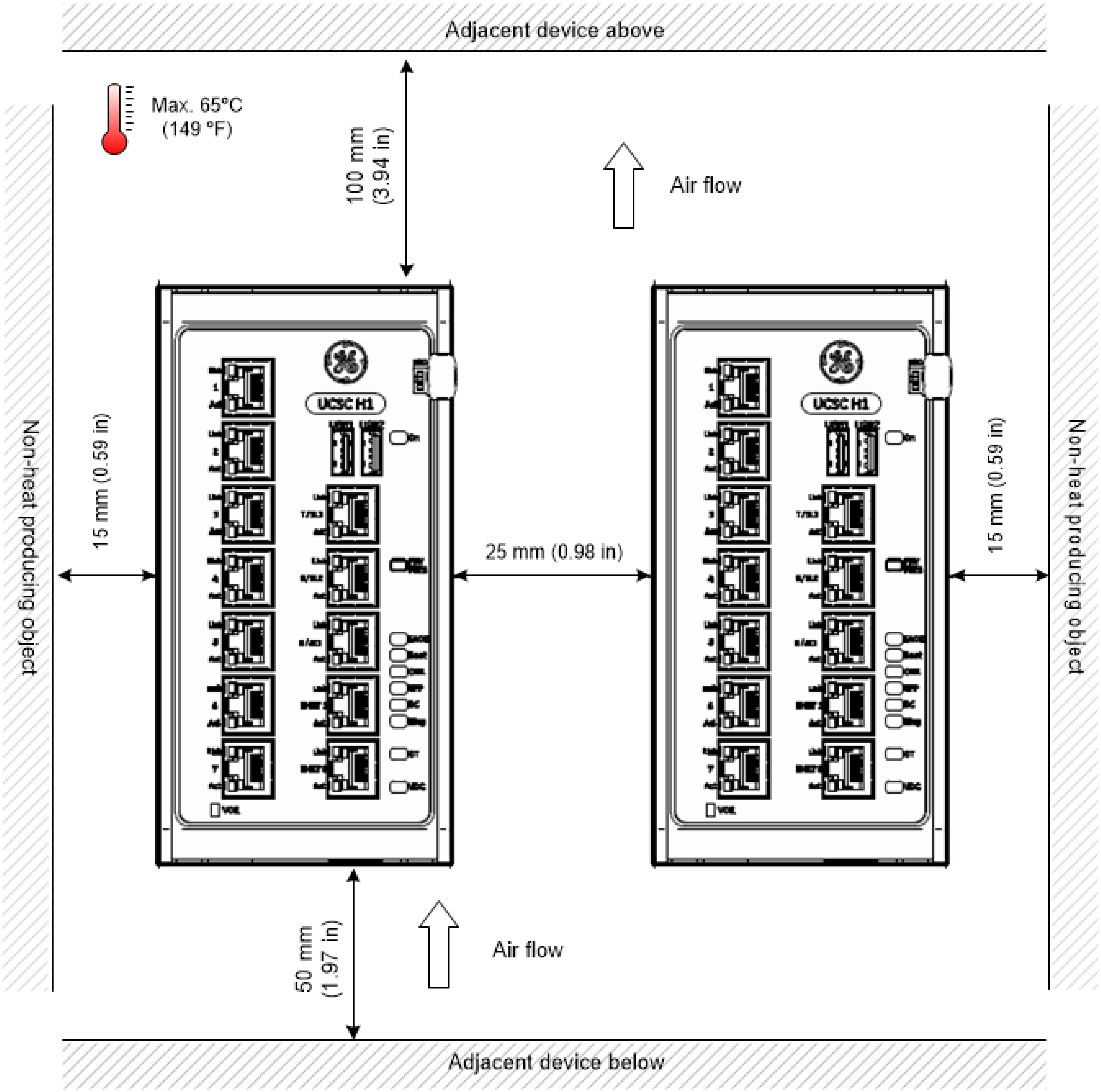
1.1.5.2 UCEC Module Mounting Requirements

The following are requirements for mounting the UCEC module:

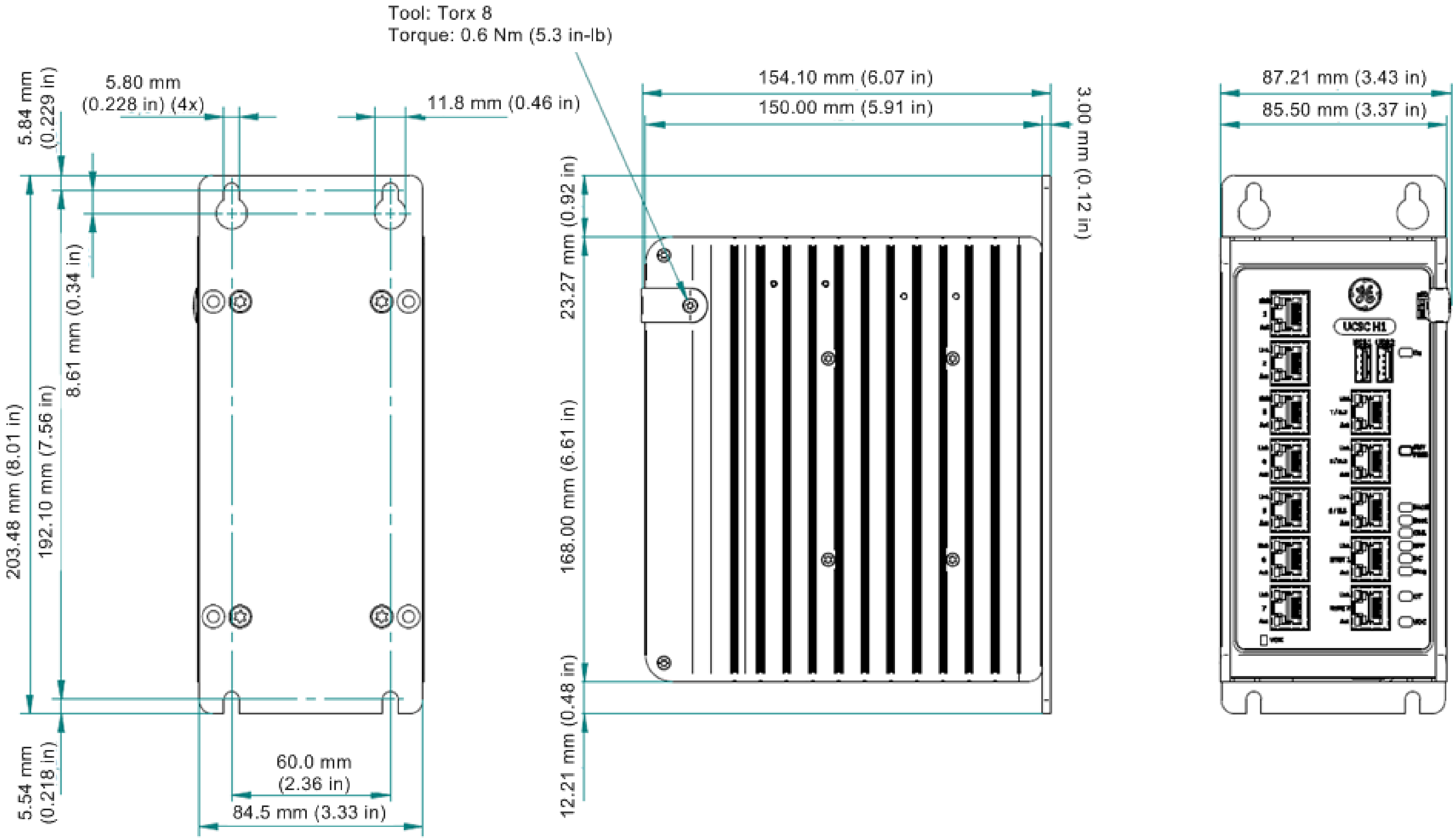
- Directly mount the UCEC to the mounting base using the four mounting screws.
- Vertical mount with unobstructed air flow through fins.
- Leave a minimal 100 mm (3.94 in) air gap above and below the UCEC module.
- Parallel mount UCEC to UCEC requires a minimal 50 mm (1.97 in) spacing to achieve full temperature rating
- The *operating temperature* envelope is 25 mm (0.98 in) from any point on UCEC.



UCECH1 Mounting Requirements to Achieve 70°C Operating Temperature



UCECH1 Mounting Requirements to Achieve 65ºC Operating Temperature


Tool: Torx 8
Torque: 0.6 Nm (5.3 in-lb)

UCEC Module Mounting Dimensions

1.1.5.3 Power Requirements

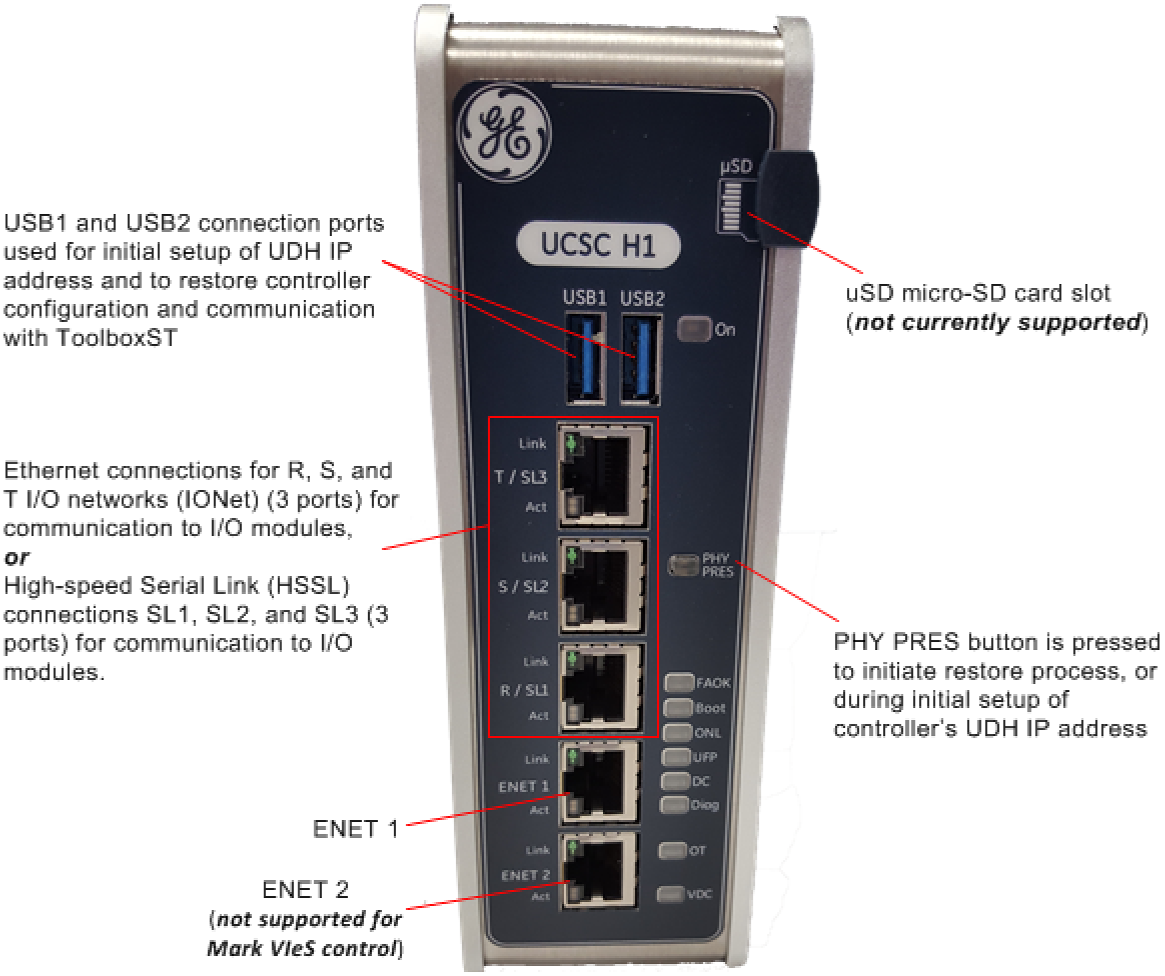
Power Requirements

Item	Min	Nom	Max	Units
UCSC Controller Input Power	—	18	30.8	Watts
UCEC Module Input Power	—	28	42	Watts
Voltage	18	24/28	30	V dc
Input Capacitance	—	25	—	uF
Surge Protection	Non-replaceable 4 A 125 V dc rated fuse Nominal melting: 26 A squared seconds (A^2 sec)			
Reverse Polarity Protection	Provided *Reversing the + and - input will not damage the UCSC, nor will it power up.*			

3-pin Power Plug

Item	Description
Pin 1	Ground
Pin 2	Negative *The UCSC case is bonded to power supply negative.*
Pin 3	Positive
Wire Sizes	28 to 16 AWG
Screw Torque	0.23 Nm (2 in-lb)
Part Number	Phoenix Contact MC 1,5/ 3-STF-3,81 - 1827716

1.1.5.4 Interface Details



USB1 and USB2 connection ports used for initial setup of UDH IP address and to restore controller configuration and communication with ToolboxST

uSD micro-SD card slot (***not currently supported***)

Ethernet connections for R, S, and T I/O networks (IONet) (3 ports) for communication to I/O modules, ***or*** High-speed Serial Link (HSSL) connections SL1, SL2, and SL3 (3 ports) for communication to I/O modules.

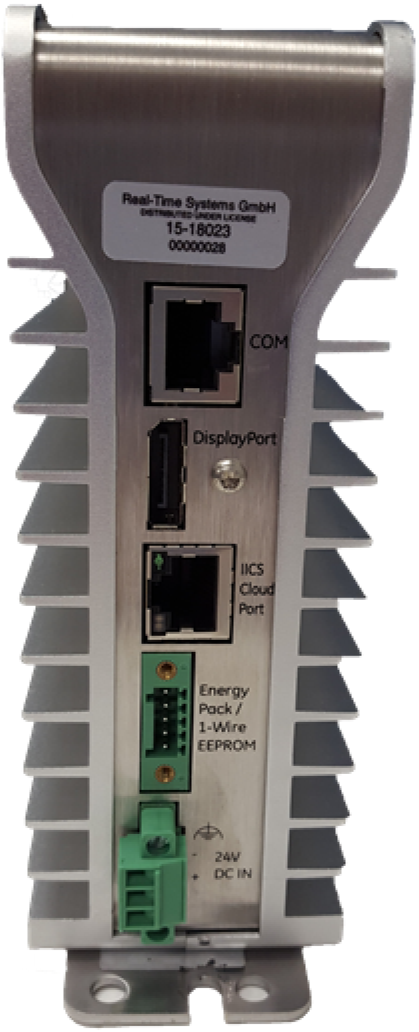
PHY PRES button is pressed to initiate restore process, or during initial setup of controller's UDH IP address

ENET 1

ENET 2 (***not supported for Mark VIeS control***)

UCSC Connection Ports (Front View)

Note For further information, refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703), the section *System Controller Device Types*.



† **COM** serial port can be used as an alternate way to set up controller IP address instead of using a flash device

DisplayPort provides signals for connecting a display monitor or video adapter (***not currently supported***)

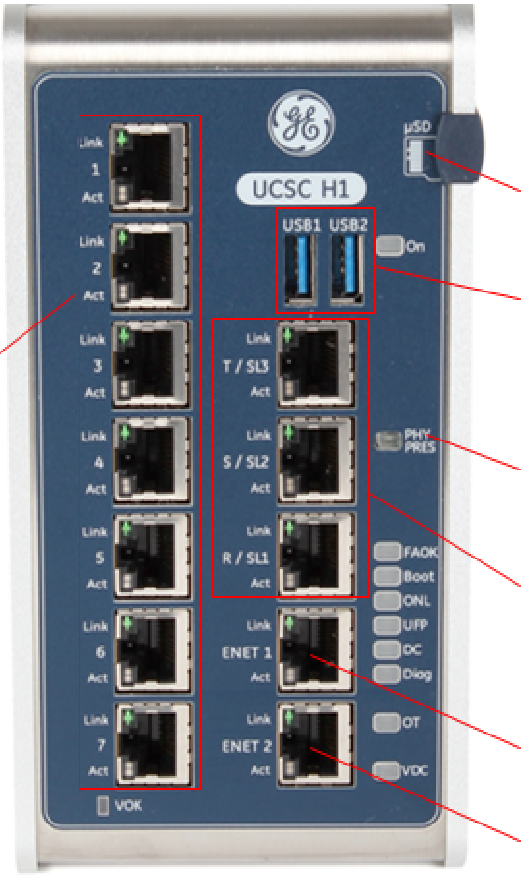
IICS Cloud Port (Ethernet port) is used to configure the EFA and to communicate with the Predix cloud environment (***not supported for Mark VIeS or MarkStat control***)

Energy Pack / 1-wire EEPROM allows energy pack connection to enable the controller to save its current state in the event of power loss (***not currently supported***)

24/28 V DC IN input power connection

UCSC Connection Ports (Bottom View)

Note † For instructions to set up the controller Internet Protocol (IP) address using the COM port, refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703), the section *Configure and Transfer IP Address to UCSB / UCSC Controller.*



uSD micro-SD card slot
(***not currently supported***)

USB1 and USB2 connection ports used for initial setup of UDH IP address and to restore controller configuration and communication with ToolboxST

High-speed Serial Link (HSSL) connection expansion port 1 through 7 for communication to I/O modules

PHY PRES button used to initiate restore process, or during initial setup of controller's UDH IP address

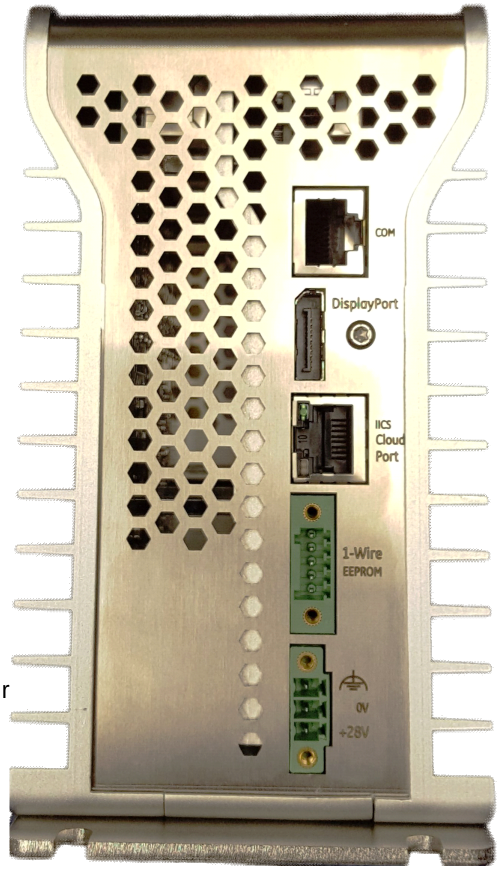
Ethernet connections for R, S, and T IONets (3 ports) for communication to I/O modules

ENET 1

ENET 2
(***not supported for Mark VIeS control***)

UCEC Connection Ports (Front View)

Note For further information, refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703), the section *System Controller Device Types*.



† **COM** serial port can be used as an alternate way to set up controller IP address instead of using a flash device

DisplayPort provides signals for connecting a display monitor or video adapter (***not currently supported***)

IICS Cloud Port (Ethernet port) is used to configure the EFA and to communicate with the Predix cloud environment (***not supported for Mark VIeS or MarkStat control***)

Energy Pack / 1-wire EEPROM allows energy pack connection to enable the controller to save its current state in the event of power loss (***not currently supported***)

24/28 V DC IN input power connection

UCEC Connection Ports (Bottom View)

Note † For instructions to set up the controller Internet Protocol (IP) address using the COM port, refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703), the section *Configure and Transfer IP Address to UCSB / UCSC Controller.*

Mark VIe UCSCH1x Ethernet Ports

Ethernet Port	Description
IONet Ethernet Interface (3 Ports)	UCSCH1A / UCSCH1B: T/SL3 is <T> network for TMR (using all three ports). S/SL2 is <S> network for Dual redundancy (used with R/SL1). R/SL1 is <R> network for Simplex redundancy. *Twisted pair 10Base-TX/100Base-TX, RJ-45 connector is used.* *TCP/IP protocols is used to communicate between controllers and I/O modules.* *For TMR and Dual configurations, IONet redundancy is equal to controller redundancy.* *For Simplex configurations, both Simplex and TMR IONet redundancy are supported.*
	UCSCH1C: T/SL3 is EtherCAT redundant (Ring topology). S/SL2 is not supported. R/SL1 is <R> IONet network *Twisted pair 100Base-TX, RJ-45 connector is used.* *TCP/IP protocols is used to communicate between controllers and I/O modules.* *Simplex IONet redundancy is the only supported configuration.*
ENET 1 Primary Ethernet Interface to LAN	UDH *Twisted pair 10Base-T/100Base-TX, RJ-45 connector is used.* *TCP/IP protocol is used for communication between controller and ToolboxST application.* *TCP/IP protocol is used for alarm communication to HMIs.* *Modbus TCP Slave and/or OPC UA* *EGD protocol is used for application variable communication to HMIs.*
ENET 2	UCSCH1A: *PROFINET* *Twisted pair 10Base-T/100Base-TX, RJ-45 connector is used.*
	UCSCH1B: Secondary plant network *Twisted pair 10Base-T/100Base-TX, RJ-45 connector is used.* *Modbus TCP Slave, OPC UA, and/or EGD*
	UCSCH1C: EtherCAT Primary (Line and Ring topologies) *Twisted pair 100Base-TX, RJ-45 connector is used.*

UCECH1B Ethernet Ports

Ethernet Port	Description
High-speed Serial Link (HSSL) Interface (10 Ports)	GE Proprietary protocol that provides high-speed point-to-point synchronous communication between a controller and any HSSL–enabled I/O module. R/SL1, S/SL3, T/SL3, expansion ports 1 through 7 are 10 independent serial link interfaces. *Twisted pair 10Base-TX/100Base-TX, RJ-45 connector is used.* *HSSL I/O module support is defined by the controller firmware.*
ENET 1 Primary Ethernet Interface to LAN	UDH *Twisted pair 10Base-T/100Base-TX, RJ-45 connector is used.* *TCP/IP protocol is used for communication between controller and ToolboxST application.* *TCP/IP protocol is used for alarm communication to HMIs.* *Modbus TCP Slave and/or OPC UA* *EGD protocol is used for application variable communication to HMIs.*
ENET 2	Secondary plant network *Twisted pair 10Base-T/100Base-TX, RJ-45 connector is used.* *Modbus TCP Slave, OPC UA, and/or EGD*

MarkStat UCSCH2x Ethernet Ports

Ethernet Port	Description
High-speed Serial Link (HSSL) Interface (3 Ports)	GE Proprietary protocol that provides high-speed point-to-point synchronous communication between a controller and any HSSL–enabled I/O module. R/SL1, S/SL3, T/SL3 are three independent serial link interfaces. *Twisted pair 10Base-TX/100Base-TX, RJ-45 connector is used.* *HSSL I/O module support is defined by the controller firmware.*
ENET 1 Primary Ethernet Interface to LAN	UDH *Twisted pair 10Base-T/100Base-TX, RJ-45 connector is used.* *TCP/IP protocol is used for communication between controller and the ToolboxST application.* *TCP/IP protocol is used for alarm communication to HMIs.* *EGD protocol is used for application variable communication to HMIs.*
ENET 2	IONet Interface *Twisted pair 10Base-T/100Base-TX, RJ-45 connector is used.*

Mark VIeS UCSCS2x Ethernet Ports

Ethernet Port	Description
IONet Ethernet Interface (3 Ports)	T/SL3 is <T> network for TMR (using all three ports). S/SL2 is <S> network for Dual redundancy (used with R/SL1). R/SL1 is <R> network for Simplex redundancy. *Twisted pair 10Base-TX/100Base-TX, RJ-45 connector is used.* *TCP/IP protocols is used to communicate between controllers and I/O modules.* *For TMR and Dual configurations, IONet redundancy is equal to controller redundancy.* *For Simplex configurations, both Simplex and TMR IONet redundancy are supported.*
ENET 1 Primary Ethernet Interface to LAN	UDH *Twisted pair 10Base-T/100Base-TX, RJ-45 connector is used.* *TCP/IP protocol is used for communication between controller and the ToolboxST application.* *TCP/IP protocol is used for alarm communication to HMIs.* *Modbus TCP Slave* *EGD protocol is used for application variable communication to HMIs.*
ENET 2	Not supported

Note For further information, refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703), the section *System Controller Device Types*.

1.1.6 UCSC Operation

1.1.6.1 UDH Network Configuration

The UCSC is typically set up for communications on the UDH network using an unencrypted minimum 4 GB flash drive that is configured with the ToolboxST application. The factory default IP address is 192.168.101.111. The correct UDH IP address must be properly set up so that the controller can communicate to the site HMIs.

Note The UCSC, as shipped from the factory, does not include the software on the controller to support communication from the PHY PRES button to the EFA. The user needs to download to the controller at least once (using ToolboxST) to enable this.

➢ To change the UDH network IP address for the UCSC

1. Verify that the HMI computer running the ToolboxST application has been configured (through Windows OS) with the correct IP address for the UDH network.
2. From the ToolboxST Component Editor, verify that the controller Platform is set as UCSCxxx.
3. From the Component Editor **General** tab Property Editor **Network Adapter 0**, configure the appropriate controller IP address as a relative subnet to the HMI's UDH IP address from Step 1.
4. Insert a non-encrypted, USB 2.0 only flash drive with a minimum 4 GB capacity into a USB port of the computer that is running the ToolboxST application.
5. From the ToolboxST Component Editor, select **Device**, **Download**, and **Controller Setup** to launch the Controller Setup Wizard.
6. Follow the on-screen instructions to load the flash drive. Refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703), the section *Configure and Transfer IP Address to UCSB / UCSC Controller* for further instructions.

➢ To set the controller's network address using the COM port

Attention

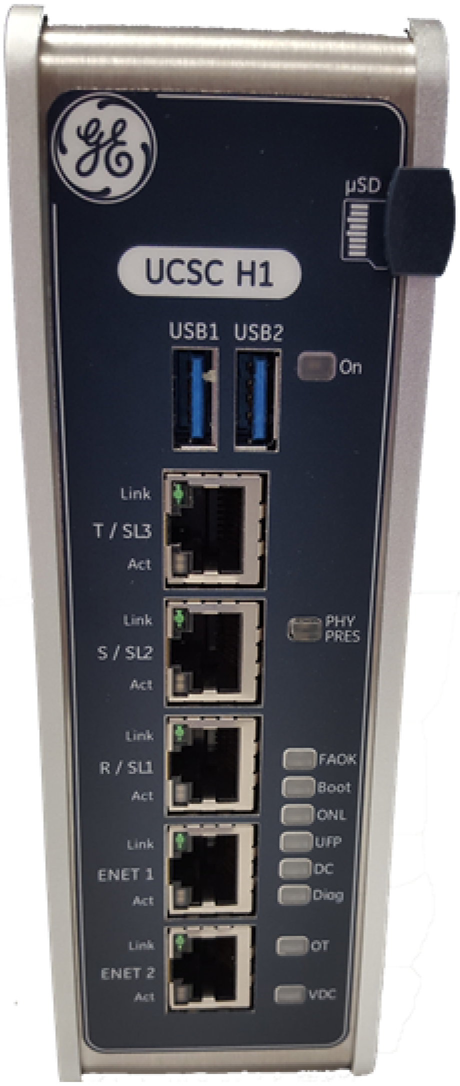
Use a UCSC COM port *adapter*, a standard serial to USB cable, and/or a Cat5e or better Ethernet cable for this connection.

---

1. Connect the UCSC COM port adapter to the Ethernet cable and the other end of the cable to the UCSC COM port.
2. Connect the UCSC COM port adapter to the serial to USB cable, then to the computer that runs the ToolboxST application.
3. From the ToolboxST Component Editor **General** tab, select **Device**, **Download**, and **Controller Setup** to launch the *Controller Setup Wizard*.
4. Follow the on-screen instructions to transfer the UDH network address to the controller. Refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703), the section *Configure and Transfer IP Address to UCSB / UCSC Controller* for further instructions.

1.1.6.2 LEDs

The locations and descriptions of the LED indicators that are located on the front panel of the UCSC controller and the UCEC module are as follows.



UCSCH1 Controller

Link LED (RJ-45 connector) (qty 5):
Solid green = connection has been established
Solid green ***plus*** **Boot LED** solid red = startup in progress

Act LED (RJ-45 connector) (qty 5):
Solid green = packet traffic
Solid green ***plus*** **Boot LED** solid red = startup in progress

On LED:
Solid green = one of the USB drives is running the restore process
Flashing green = restore process failure

FAOK LED indicates status of Embedded Field Agent (EFA)
Solid green = EFA connected to cloud.
Flashing green = refer to *CPE400 Quick Start Guide* (GFK-3002)
(***not supported for Mark VIeS or MarkStat control)***

Boot LED:
Solid red = startup in progress
Off = startup completed
Flashing red = controller firmware failed to load properly
Flashing once every 3 seconds = Baseload signature verification failure

ONL LED:
Solid green = controller is online and running the application

UFP LED indicates status of FPGA program updates:
Off = normal operation
Solid amber[†] = internal software update in progress
Solid green = controller is online and running the application

DC LED:
Solid green = controller is designated controller
(***always on for Simplex configurations***)

Diag LED:
Flashing red = active diagnostic alarm

OT LED:
Solid amber [‡] = temperature of internal components exceeds recommended limit

VDC LED:
Solid red = stand-by power on board in soft-off or suspend to disk mode
Solid amber = suspend to RAM, memory power on
Solid green = full power on
Flashing red = Missing internal voltage
Flashing amber = all voltages asserted but system reset in progress

[†] *An internal software update may take several minutes. Do not cycle controller power during this update because this could cause potential damage to the controller.*

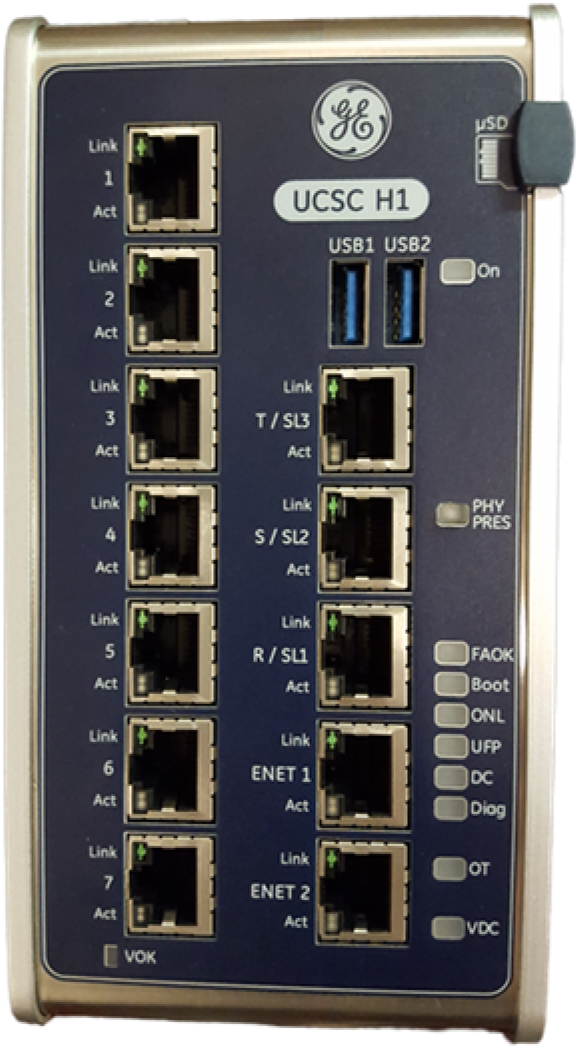
[‡] *A diagnostic alarm for temperature is also annunciated. When the temperature exceeds the max threshold, the controller automatically shuts down to prevent damage.*

Link LED (RJ-45 connector) (qty 12):
Solid green = connection has been established
Solid green ***plus*** Boot LED solid red = startup in progress

Act LED (RJ-45 connector) (qty 12):
Solid green = packet traffic
Solid green ***plus*** Boot LED solid red = startup in progress

VOK LED:
Solid green = All voltages are operating correctly
Flashing green = internal voltage has failed
Off = input voltage or primary internal voltage has failed

Note: *All other LED functionality is as described for the UCSC controller.*



UCECH1 Module

1.1.6.3 Over-temperature Protection

The UCSC controller uses internal temperature readings and logic to protect its internal electronics. Internal circuitry generates a warning at 85°C (185 °F) and shuts down at 95°C (203 °F). The UCSC will reboot once the internal circuitry detects the temperature has dropped below 75°C (167 °F). Independently, the microprocessor monitors its operating temperature and generates a warning at 105°C (221 °F) and shuts down at 107°C (225 °F). A power cycle is required to recover from a microprocessor over-temperature shut down. Both of these warnings drive the OT LED and are annunciated as diagnostic alarms.

1.1.6.4 UCSC COM Port

Typically used by GE to troubleshoot in the field, the UCSC COM port accepts a UCSC COM port *adapter* and a standard serial to USB cable is used to connect to another computer. Use Cat5e or better Ethernet cable for this connection. The COM port can also be used to set the controller’s UDH network address. For these instructions, refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703), the section *Configure and Transfer IP Address to UCSB / UCSC Controller*.

1.1.7 UCSC Embedded Field Agent (EFA)

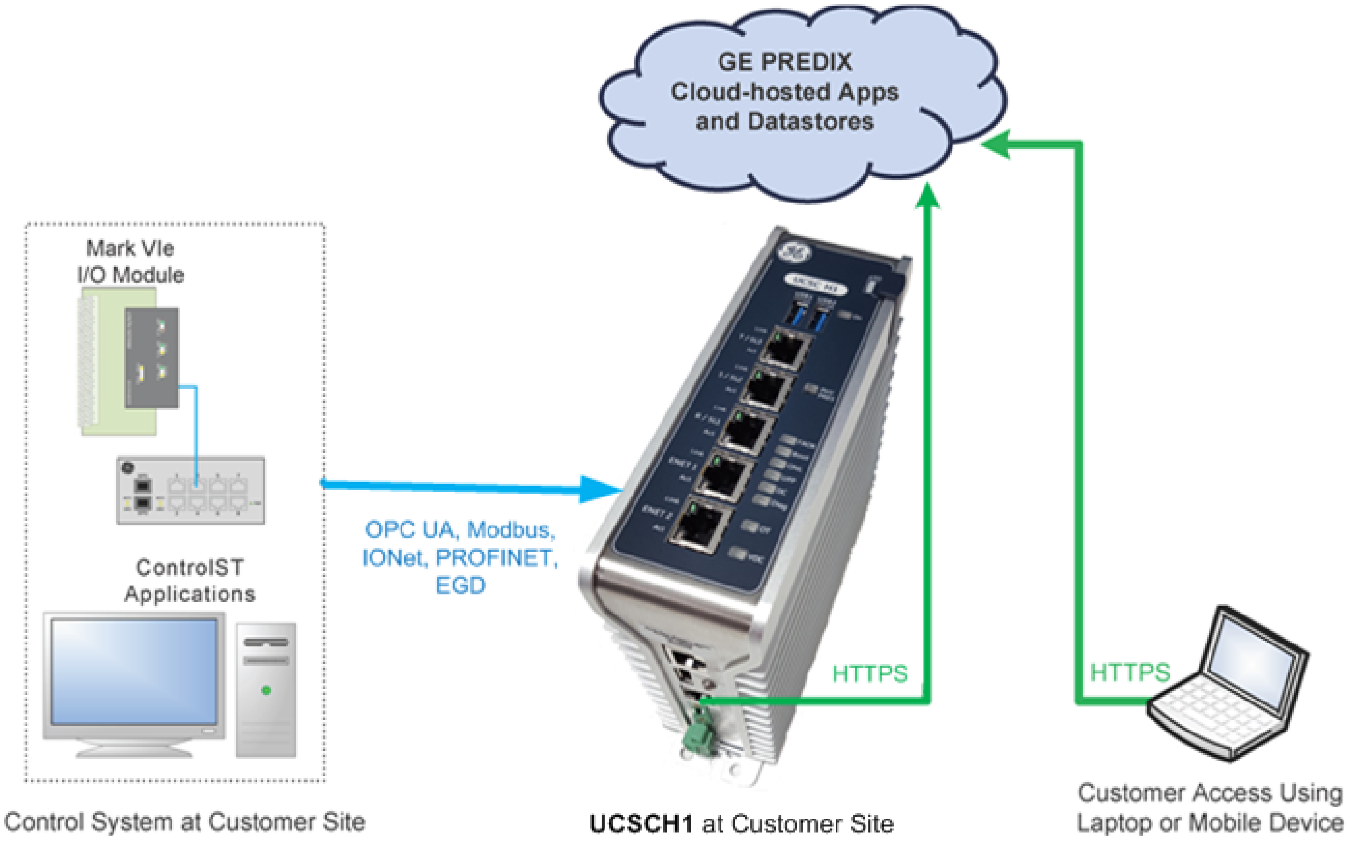
The Embedded Field Agent (EFA) provides connectivity to GE Predix* cloud-hosted applications and datastores through a local Predix machine interface that runs within a Linux virtual machine on the UCSCH1. The EFA has two primary functions:

- Collecting and transmitting machine data securely
- A platform for running Predix apps on the Edge directly on the machine

Once a Field Agent is up and running, data is transferred from the plant to the cloud over encrypted channels, preserving its time stamp, quality, and fidelity. It also provides a rich domain application environment for edge processing, so logic can be executed at the most appropriate place in the architecture — locally on the machine or in the cloud.

Note For more information, refer to the following documentation:

- *Field Agents User Guide* (GFK-2993)
- *Field Agent Secure Deployment Guide* (GFK-3009)
- *Field Agents Upgrade Guide* (GFK-3017)



1.1.8 UCSC Virtual Network

The virtual network is a feature of the hypervisor used in UCSCH1 controllers. The virtual network transfers data between the virtual machines (VMs) in the UCSCH1 controller like an Ethernet network transfers data between physical machines over a physical network. The virtual network in the UCSCH1 controller is used to transfer data between the Mark VIe control running in one VM, and the Embedded Field Agent (*EFA*) running in another VM. The EFA requires a connection to the Mark VIe control and a connection to the cloud. However, the Mark VIe control must not have a connection to the cloud, so a physical managed switch must be used to segment the networks. To resolve this issue, data is passed through the virtual network so the EFA can connect directly to the cloud and eliminate the need of a managed switch.

The virtual network transfers data through memory shared between the VMs instead of the wires of a physical network. The Mark VIe control uses a network firewall to prevent all other traffic.

Like a physical network, the virtual network must be configured with an IP address and subnet mask. The VMs in the UCSCH1 controller must be on the same subnet to function properly. The Mark VIe virtual network is configured using the ToolboxST application. The default configurations for the Mark VIe control and the EFA provide a working virtual network. However, changing the configuration in one VM may interrupt communication over the virtual network until a corresponding change is made to the other VM.

Note To configure virtual network adapters, refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6700), the section *Virtual Network Adapters*. To configure the virtual network in the EFA, refer to the *Field Agents User Guide* (GFK-2993).

1.1.9 UCSC Embedded PROFINET Gateway (Embedded PPNG) Module

Attention

The information provided in this section is only applicable beginning with ControlST V07.04 / PPNG V05.11 and higher.

This information does not apply to the stand-alone PPNG PROFINET Gateway (PPNG) module. For information on the PPNG module, refer to the chapter *PPNG PROFINET Gateway Module*.

The UCSCH1A Embedded PROFINET Gateway (Embedded PPNG) module is a virtual machine that maps I/O from PROFINET Slave devices to the Mark VIe controller. It connects to a high-speed PROFINET local area network (LAN), enabling communication with PROFINET I/O devices. The Embedded PPNG module provides the functionality, services, and protocols required for certification as a PROFINET RT Version 2.2 I/O controller, running 100 Mbps Ethernet interfaces.

Embedded PPNG features include:

- One RJ-45 shielded-twisted pair 10/100 Mbps port for PROFINET communication
- Simplex or Hot Backup module redundancy (Hot Backup configuration supports PROFINET system redundancy)
- Support for star (connect to switch), line/bus (connect directly to I/O device), or mixed network topologies on the PROFINET network, and Ring topology with MRP devices
- PROFINET I/O device configuration
- Cyclic exchange of input and output data from PROFINET I/O devices, asynchronous with Mark VIe controller frame
- Input and output values displayed in the ToolboxST application
- Device diagnostic messages for troubleshooting

From the ToolboxST application, users can add and configure PROFINET I/O devices and smart sensors in a typical Mark VIe control system architecture. Any change made to the configuration of attached PROFINET devices requires a new configuration file to be downloaded to the Embedded PPNG, which reboots the virtual machine. Afterwards, a local variable can be connected to a particular I/O point from PROFINET device I/O and used in Mark VIe controller application logic.

1.1.9.1 Compatibility

The following table lists the available Embedded PPNG configurations. For details on switching between configurations, refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703), the section *Embedded PPNG Hot Backup and Simplex Configuration*.

Supported Embedded PPNG Configurations

UCSCH1A Controller Redundancy	Simplex Embedded PPNG	Hot Backup Embedded PPNG
Simplex	Supported; 1 Embedded PPNG	Not supported
Dual	Supported; 1-2 Embedded PPNGs	Supported
Triple Modular Redundancy (TMR)	Supported; 1-3 Embedded PPNGs	Supported

The following is an explanation of redundancy options:

- Dual UCSCH1A controller redundancy supports up to two Simplex Embedded PPNGs or a Hot Backup configuration
- TMR UCSCH1A controller redundancy supports up to three Simplex Embedded PPNGs or a Hot Backup configuration
- In the Hot Backup configuration, R and S Embedded PPNGs are used; the T Embedded PPNG is not used.

Migration from Prior Embedded PPNG Version

Prior to ControlST V07.04 (which includes PPNG V05.11 firmware), the only supported Embedded PPNG configuration was a Simplex Embedded PPNG in the R UCSCH1A controller, regardless of controller redundancy. Also, the R IONet and PROFINET networks had to be combined because the Embedded PPNG's only available network connection was the ENET2 port (this port was required for communication over IONet to the Mark VIe controller(s) and PROFINET devices).

Beginning with ControlST V07.04, PROFINET system redundancy support has been added, as well as the support for multiple Simplex Embedded PPNGs. IONet communication between the Embedded PPNG and the Mark VIe controller(s) travels through internal IONet switches, which enables separation of the IONet and PROFINET external networks.

No re-wiring or configuration change is required during an upgrade from an older Embedded PPNG version (prior to ControlST V07.04). The I/O and configuration compatibility codes for the Embedded PPNG have changed, which drives an offline download to the system. Additionally, the variable name **PROFI_BACKUP_ PPNG_R** has been changed to **PRIMARY_PPNG_R/PRIMARY_PPNG_S** to indicate the Primary Embedded PPNG in a Hot Backup configuration. Therefore, any variable connected to **PROFI_BACKUP_PPNG_R** is intentionally dropped.

After upgrade, users can separate the IONet and PROFINET networks if needed, but it is not required to maintain existing functionality.

PROFINET Device Support in Hot Backup Configuration

The Hot Backup configuration provides the ability to have both Embedded PPNG redundancy (via two Embedded PPNGs working together) and network redundancy (via MRP ring). This is achieved by implementing the PROFINET system redundancy feature of the standard PROFINET version. The Mark VIe Embedded PPNG implements and supports S2 system redundancy in Legacy mode and supports the PROFINET scanner devices listed in the following table.

Supported PROFINET Scanner Devices in Hot Backup Configuration

PROFINET Slave Device	Part Number
RX3i CEP PROFINET Scanner	IC695CEP001
RX3i PROFINET Scanner	IC695PNS001
PAC8000 PROFINET Scanner	8515-BI-PN
VersaMax PROFINET Scanner	IC200PNS001
GLM064 MRP Switch	IC695GLM064
The latest GSDML files for these devices are distributed with the ControlST Software Suite.	

1.1.9.2 Dataflow

The UCSCH1A Embedded PPNG exchanges data with the control system at standard Mark VIe controller frame rates (10 ms, 20 ms, 40 ms and so forth). Actual PROFINET data size depends on the data transmitted by the PROFINET I/O devices. The Embedded PPNG limits this to a maximum of 8 KB of data in either direction. The ToolboxST application has rules in place to check for the maximum allowable amount of PROFINET data in terms of Ethernet packets.

The exchange of data between the PROFINET I/O device and the UCSC controller is a configurable I/O device data update rate (refer to the applicable *Embedded PPNG Specifications* table for these values). The frame rate of the Mark VIe controller is also a configurable scan rate. Be aware that the transfer of data occurs asynchronously.

IONet communication between the Embedded PPNG and the Mark VIe firmware is routed through internal IONet switches on the UCSCH1A controller(s). Thus, the Embedded PPNG and the Mark VIe firmware share the internal R and S IONet ports in the UCSCH1A controller.

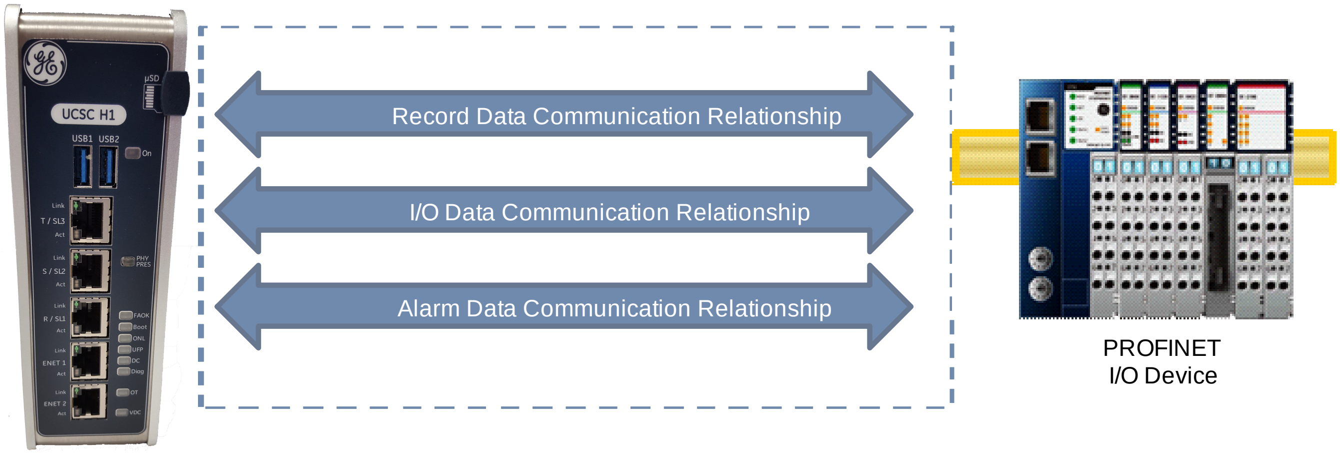
1.1.9.3 PROFINET Network Communication

A typical PROFINET network incudes the following components:

- **PROFINET I/O controller** is the UCSC Embedded PPNG virtual machine that acts as a PROFINET I/O controller. It controls one or more PROFINET I/O devices through Read/Write of the associated data.
- **Ethernet switch** is either the GE-qualified, general-purpose, unmanaged Ethernet switch or the GE-qualified MRP managed Ethernet switch. Either switch is used to route data from multiple PROFINET I/O devices to the Embedded PPNG.
- **PROFINET I/O devices** are distributed I/O devices hosting various data types that communicate with the Embedded PPNG.

Before the UCSC controller can exchange data with a PROFINET I/O device, an application relationship (connection) must be established between the devices. The UCSC controller automatically sets up the correct number and types of Communication Relationships (CRs) based on its ControlST configuration. The following CR types are established between the UCSC controller and I/O devices:

- **Record Data CRs** are always the first to be established within an application relationship. They are used for non real-time transfers of data records such as startup parameters, diagnostics, identifications, and configurations.
- **IO CRs** are used for real-time, cyclic transfer of I/O data.
- **Alarm CR** is used for real-time, acyclic transfer of alarms and events.


UCSC H1
USB1
USB2
Record Data Communication Relationship
I/O Data Communication Relationship
Alarm Data Communication Relationship
PROFINET
I/O Device

Typical PROFINET Network Communication

1.1.9.4 Embedded PPNG Specifications

Simplex Embedded PPNG Specifications

Item	**Specification**
Conformance class version	PROFINET IO-RT V2.2 Class A I/O controller
Ethernet cabling supported	Cat 5e STP for PROFINET
I/O device data update rates	Configurable: 1 ms, 2 ms, 4 ms, 8 ms, 16 ms, 32 ms, 64 ms, 128 ms, 256 ms, and 512 ms
Number of PROFINET MAC addresses	One
Maximum I/O memory	8 KB of input and 8 KB of output memory
Max number of PROFINET I/O devices attached to UCSC	Limited to eight devices with update rates of 1 ms
Network topology supported	Star (typical), Line (daisy-chain with UCSC at one end of the bus), or a combination
Maximum PROFINET data rate	6 KB per millisecond
PROFINET Network Speed	100 Mbps full duplex on dedicated PROFINET network
Media Redundancy Protocol (MRP)	Not supported

Simplex Embedded PPNG with MRP Specifications

Item	**Specification**
Conformance class version	PROFINET IO-RT V2.2 Class A I/O controller
Ethernet cabling supported	Cat 5e STP for PROFINET
I/O device data update rates	Configurable: 8 ms, 16 ms, 32 ms, 64 ms, 128 ms, 256 ms, and 512 ms
Number of PROFINET MAC addresses	One
Maximum I/O memory	8 KB of input and 8 KB of output memory
Max number of PROFINET I/O devices attached to UCSC	Refer to the table in the section *Device Update Rate versus Number of Devices*
Network topology supported	Ring
Maximum PROFINET data rate	6 KB per millisecond
PROFINET Network Speed	100 Mbps full duplex on dedicated PROFINET network
Media Redundancy Protocol (MRP)	Supported using the GE-qualified MRP switch serving as the Media Redundancy Manager (MRM)

Hot Backup Embedded PPNG with MRP Specifications

Item	**Specification**
Conformance class version	PROFINET IO-RT V2.2 Class A I/O controller
Ethernet cabling supported	Cat 5e STP for PROFINET
I/O device data update rates	Configurable: 8 ms, 16 ms, 32 ms, 64 ms, 128 ms, 256 ms, and 512 ms
Number of PROFINET MAC addresses	One
Maximum I/O memory	8 KB of input and 8 KB of output memory
Max number of PROFINET I/O devices attached to UCSC	Refer to the table in the section *Device Update Rate versus Number of Devices*
Network topology supported	Ring using MRP
Maximum PROFINET data rate	6 KB per millisecond
PROFINET Network Speed	100 Mbps full duplex on dedicated PROFINET network

Hot Backup Embedded PPNG with MRP Specifications (continued)

Item	Specification
Media Redundancy Protocol (MRP)	Supported using the GE-qualified MRP switches, with one serving as the Media Redundancy Manager (MRM)
Maximum Primary Switch-over time (time it takes to switch Embedded PPNG Master)	Refer to the section *Primary Switch-over Time in Hot Backup Configuration*

1.1.9.5 Embedded PPNG Network Configuration

The Embedded PPNG UCSCH1A controller communicates with a PROFINET scanner (also commonly known as a bus coupler or head module, depending on the manufacturer), which then enables PROFINET communication to I/O devices. By default, the ToolboxST application supports the configuration of several GE PROFINET scanners. For third-party or new PROFINET scanners, users can import the vendor-supplied PROFINET device configuration file (GSDML) into their ToolboxST configuration. For further details on supported PROFINET devices in a Hot Backup configuration, refer to the *Compatibility* section *PROFINET Device Support in Hot Backup Configuration*.

Simplex Embedded PPNG without MRP Configuration

➢ **To set up the Simplex Embedded PPNG without MRP**

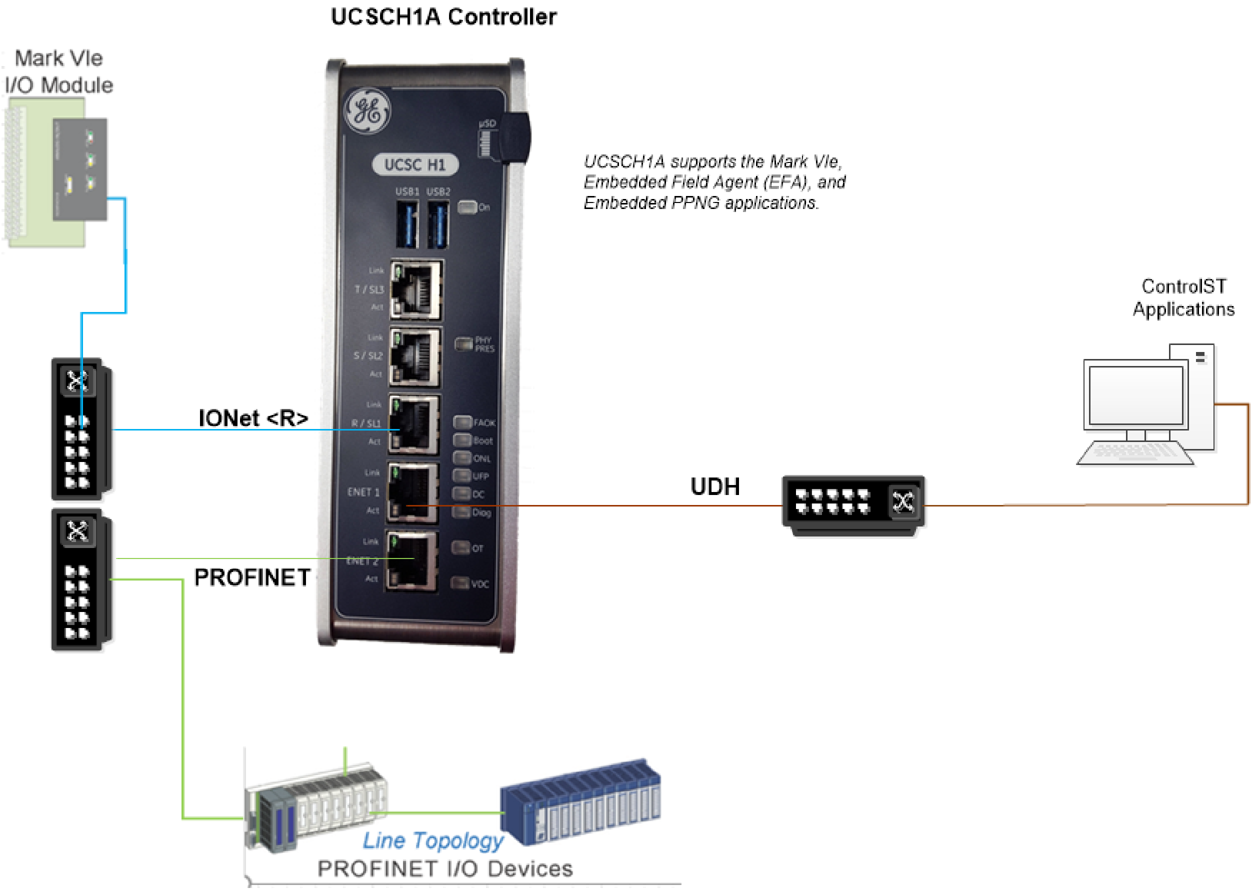
1. Connect a Cat 5e shielded-twisted pair Ethernet cable to a GE-qualified unmanaged switch and the other end of the Ethernet cable to the UCSCH1A *ENET 2 port*. Refer to the PROFINET device-specific technical manuals for more information on requirements for connecting those devices to the GE-qualified unmanaged switch.
2. From the ToolboxST application, configure the embedded Embedded PPNG. For instructions, refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6700), the section *PPNG PROFINET Module Configuration*.
   - **a.** Configure the PROFINET network data rate.
   - **b.** Attach and configure the PROFINET I/O devices.

Note The I/O device host names must match the names in the ToolboxST configuration. The ToolboxST DCP configuration feature can be used to set the I/O device host names. Right-click the PPNGE1A module and select **Identify PROFINET Devices**.

3. From the ToolboxST application, perform a series of Builds and Downloads (similar to a standard I/O pack).

Attention

Versions prior to ControlST V07.04 / PPNG V05.11 required that the IONet and PROFINET networks be combined. Beginning with ControlST V07.04 / PPNG V05.11, the UCSCH1A controller supports network separation between the R IONet and PROFINET networks (through internal IONet switches). Combining the IONet and PROFINET networks should only be used in Legacy installed systems. All new designs should separate the networks as illustrated in the following figure.



Simplex Embedded PPNG Network Topology without MRP

Simplex Embedded PPNG with MRP Configuration

➢ To set up the Simplex Embedded PPNG with MRP

1. Connect a Cat 5e shielded-twisted pair Ethernet cable to a GE-qualified MRP switch (non-Ring port in accordance with MRP switch configuration) and the other end of the Ethernet cable to the UCSCH1A *ENET 2 port*. Refer to the PROFINET device-specific technical manuals for more information on requirements for connecting those devices to the GE-qualified MRP switch.
2. Configure the MRP switch as a Media Redundancy Manager (MRM). In the MRM configuration, two ports are configured as Ring ports. The PROFINET devices are connected to the Ring ports as illustrated in the following figure, *Simplex Embedded PPNG Network Topology with MRP*.

Note The MRP ring should be kept open (do not close the loop) until the MRM switch has been configured to avoid a situation where there is no ring manager present to prevent a network storm. Once the MRM switch has been configured in its role as ring manager, the ring can be closed to provide the expected network redundancy.

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3. From the ToolboxST application, configure the Embedded PPNG module. For instructions, refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6700), the section *PPNG PROFINET Module Configuration*.
    - **a.** Add the MRP switch as a PROFINET device to the Embedded PPNG configuration. Configure the MRP switch as an MRM.
    - **b.** Attach and configure the PROFINET I/O devices.
    - **c.** Configure the Media Redundancy Client (MRC) parameters for the PROFINET devices.

Note The I/O device host names must match the names in the ToolboxST configuration. The ToolboxST DCP configuration feature can be used to set the I/O device host names. Right-click the **PPNG-E21CR** module and select **Identify PROFINET Devices**.

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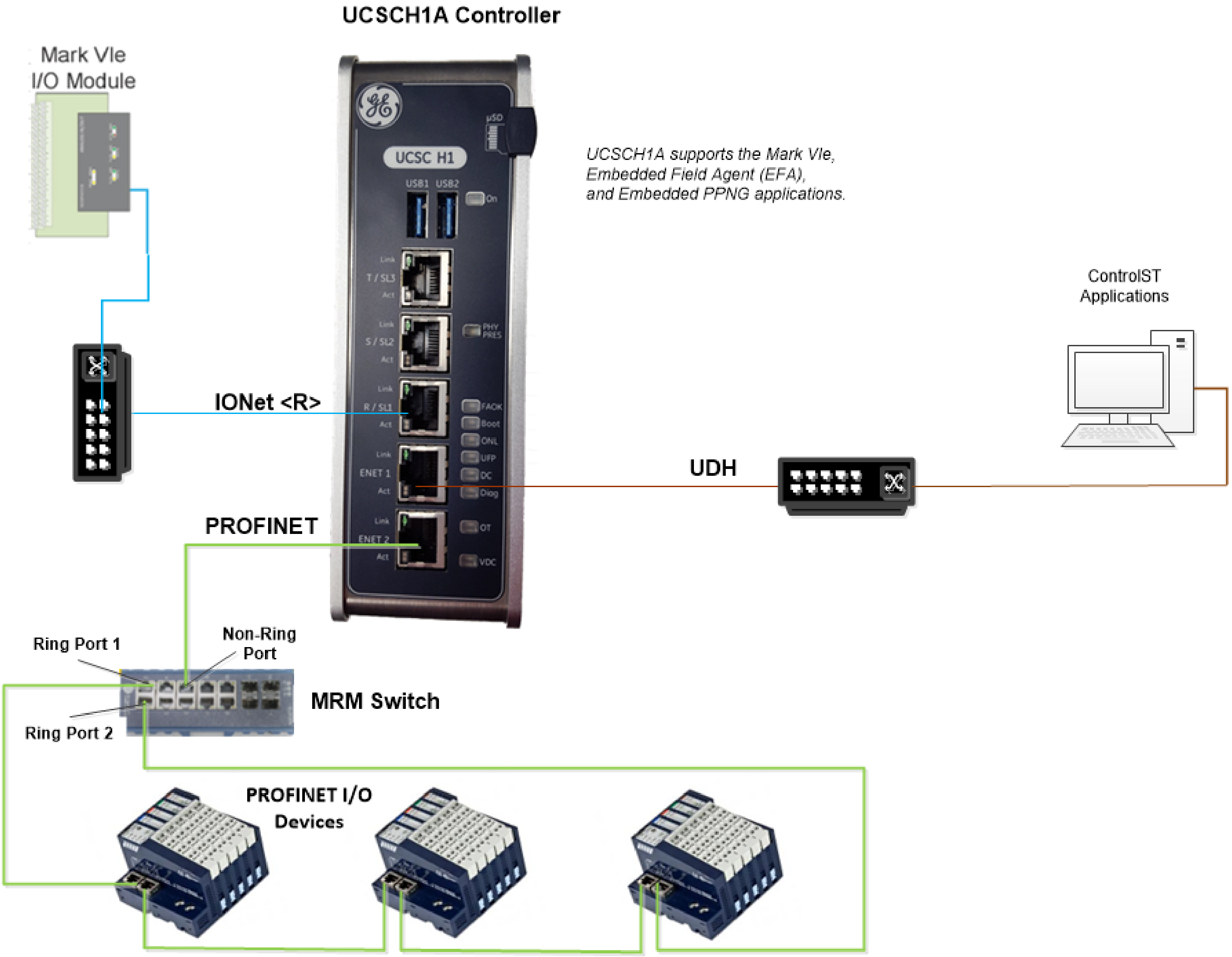
4. From the ToolboxST application, perform a series of Builds and Downloads (similar to a standard I/O pack).



Simplex Embedded PPNG Network Topology with MRP

Hot Backup Embedded PPNG with MRP Configuration

➢ To set up the Hot Backup Embedded PPNG

1. Connect a Cat 5e shielded-twisted pair Ethernet cable to a GE-qualified MRP switch (non-Ring port in accordance with MRP switch configuration) and the other end of the Ethernet cable to the UCSCH1A *ENET 2 port*. Refer to the PROFINET device-specific technical manuals for more information on requirements for connecting those devices to the GE-qualified MRP switch.
2. For a Hot Backup configuration, two MRP switches are used. In all PROFINET devices (including MRP switches), two ports are configured as Ring ports and the PROFINET devices are connected to the Ring ports as illustrated in the figure *Hot Backup Embedded PPNG with MRP Network Topology*.
   Also, the Media Redundancy Manager (MRM) switch and the Media Redundancy Client (MRC) switch are looped through the other ring port as illustrated in the figure.

   Note The MRP ring should be kept open (do not close the loop) until the MRM switch has been configured to avoid a situation where there is no ring manager present to prevent a network storm. Once the MRM switch has been configured in its role as ring manager, the ring can be closed to provide the expected network redundancy.

3. From the ToolboxST application, configure the Embedded PPNG module. For instructions, refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6700), the section *PPNG PROFINET Module Configuration*.
   a. Add the MRP switch as a PROFINET device to the Embedded PPNG configuration. Configure the MRP switch as an MRM and configure the other MRP switch as an MRC.
   b. Attach and configure the PROFINET I/O devices.
   c. Configure the MRC parameters for the PROFINET devices.

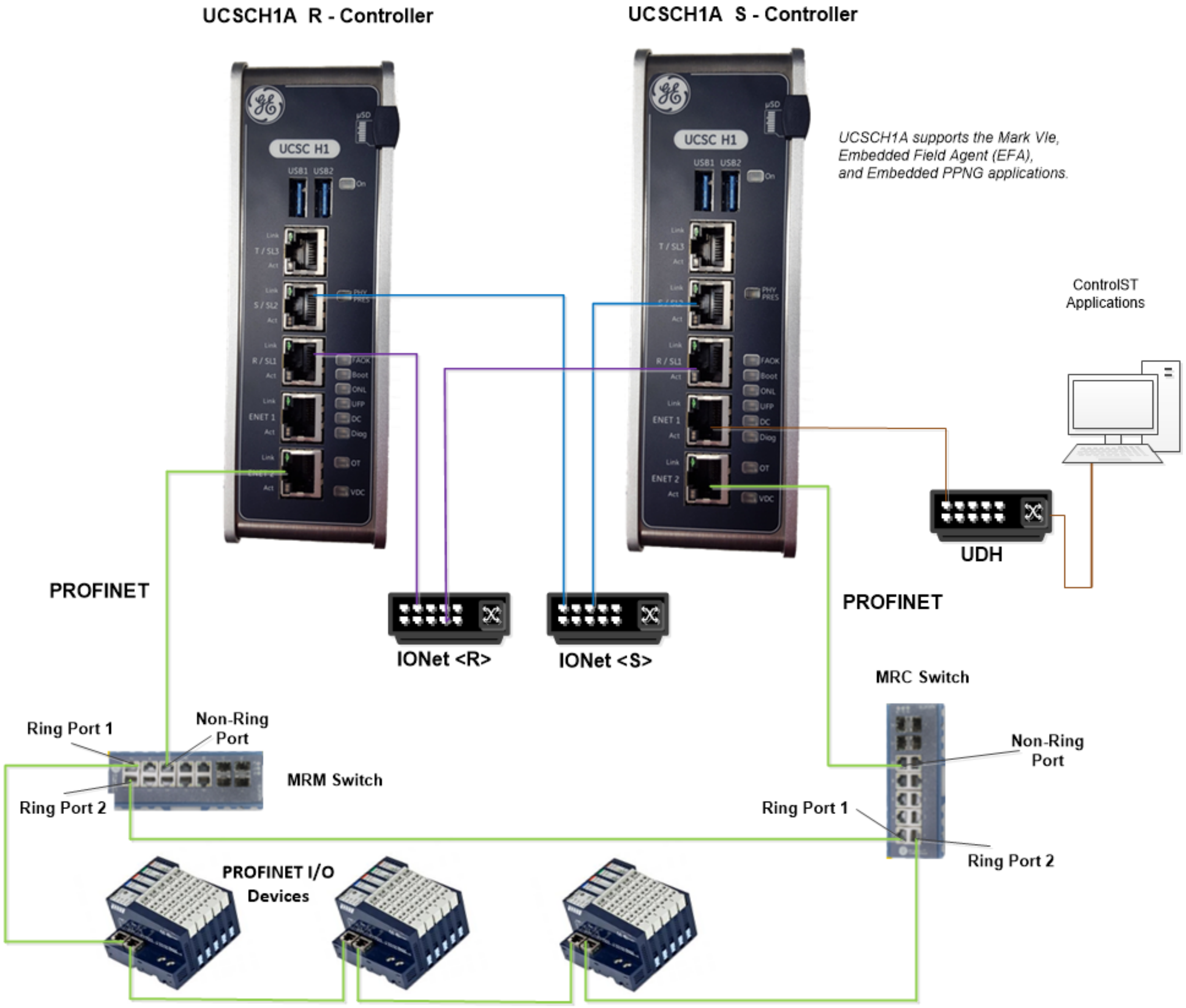
Note The I/O device host names must match the names in the ToolboxST configuration. The ToolboxST DCP configuration feature can be used to set the I/O device host names. Right-click the **PPNG-E21CR** module and select **Identify PROFINET Devices**.

4. From the ToolboxST application, perform a series of Builds and Downloads (similar to a standard I/O pack).

Additional configuration details:

- The MRM switch or the MRC switch can be connected to either the R or S Embedded PPNGs in the configuration. (The T Embedded PPNG is not used.)
- The UCSC ENET2 port can be connected to any of the available non-Ring ports in the MRP switch.
- Ring ports are configured using the ToolboxST application.
- The MRM and MRC switches can be looped through Ring Port 1 and Ring Port 2.

Note The network configuration represented in the following figure is the only GE-qualified network configuration for Hot Backup. You must use the GE-qualified PROFINET MRP switch as specified in this illustration.



UCSCH1A supports the Mark VIe, Embedded Field Agent (EFA), and Embedded PPNG applications.

Hot Backup Embedded PPNG with MRP Network Topology

Device Update Rate versus Number of Devices

The following table provides the device update rate per number of PROFINET devices depending on the configuration.

In order to have an MRP configuration, you must use either one (Simplex with MRP) or two (Hot Backup with MRP) GLM switches in the system. In order to configure and monitor these switches, you must add them to your configuration as PROFINET devices themselves. Therefore, they must be included in the count when assessing the number of PROFINET devices supported per cyclic rate when MRP is used.

Cyclic Rate (ms)	Number of PROFINET Devices		
	Simplex	Simplex with MRP	Hot Backup with MRP
1	8	0	0
2	16	0	0
4	32	0	0
8	64	18	18
16	64	34	34
32	64	64	64
64	64	64	64
128	64	64	64
256	64	64	64
512	64	64	64

Primary Switch-over Time in Hot Backup Configuration

The following table lists the supported device cyclic rates and respective primary switch-over time in a Hot Backup configuration.

Note The switch-over time in the following table is applicable to the Embedded PPNG. If you are performing a primary switch-over from a ToolboxST command, the primary switch-over time will vary in accordance with the controller frame rate. This allows time for the I/O pack to receive the command from the controller and for the response to be sent back to controller (these two parameters are related to the controller frame rate).

Cyclic Rate (ms)	Switch-over Time (ms)
8	60
16	80
32	140
64	200
128	250-350
256	350-550
512	900-1000

GE-qualified PROFINET Switches (for Simplex Use in non-MRP Networks)

GE has qualified the following unmanaged switches for use on the PROFINET communication network, between the UCSC and the Slave devices:

- ESWA 8–port industrial unmanaged switch
- ESWB 16–port industrial unmanaged switch

GE-qualified PROFINET MRP Switches

GE has qualified the following managed switch for use as MRP switches on the PROFINET communication network between the Slave devices: IC086GLM064 (Rev -AB or later).

An older version of the GLM064 switch may be used, but the firmware for the switch must be upgraded to V00.00.06 or later. Refer to the *PACSystems PROFINET Managed Industrial Ethernet Switches User Manual* (GFK-3030) for the procedures to update the GLM switch firmware.

Network Cabling

Users should order green-colored Ethernet cables for connections between the UCSC and all PROFINET devices on the PROFINET network (cable color distinguishes this network from the IONet). The following table lists the available green network cables.

Green-colored PROFINET Ethernet Cables

GE Part #	Length
336A4940DTP3GN	0.91 m (3 ft)
336A4940DTP5GN	1.52 m (5 ft)
336A4940DTP8GN	2.44 m (8 ft)
336A4940DTP10GN	3.05 m (10 ft)
336A4940DTP12GN	3.66 m (12 ft)
336A4940DTP15GN	4.57 m (15 ft)
336A4940DTP18GN	5.49 m (18 ft)

1.1.9.6 Embedded PPNG Variables

Variable Name	Type	Description
L3DIAG_PPNG_R	Input BOOL	True indicates at least one diagnostic alarm is in the queue (active or normal state)
LINK_OK_PPNG_R	Input BOOL	True indicates the IONet communication link is okay
ATTN_PPNG_R	Input BOOL	True indicates at least one active diagnostic alarm
PRIMARY_PPNG_R	Input BOOL	This signal should be True for a Simplex Embedded PPNG configuration. In a Hot Backup configuration, if R Embedded PPNG is Primary, this variable remains True. If R is Backup Embedded PPNG, this variable remains False.
PRIMARY_PPNG_S	Input BOOL	This signal should be False in a Simplex Embedded PPNG configuration. In a Hot Backup configuration, if S Embedded PPNG is Primary, this variable remains True. If S is Backup Embedded PPNG, this variable remains False.
CPU_HOT_PPNG_R	Input BOOL	This signal is True if the processor temperature has exceeded 97°C (207 °F).
BoardTmpr_PPNG_R	AnalogInput REAL	Thermal sensors are not available in the Embedded PPNG, therefore value this will always be zero.
AuxTmpr_PPNG_R	AnalogInput REAL	Thermal sensors are not available in the Embedded PPNG, therefore this value will always be zero.
PrimarySwitchCmd	Output BOOL	User Primary switch-over command. On the rising edge of this variable going to True, the Primary Embedded PPNG is changed to Backup Embedded PPNG.

1.1.9.7 Hot Backup Configuration (PROFINET System Redundancy)

In a Hot Backup configuration, two UCSCH1A controllers are used, which results in two Embedded PPNGs. These two Embedded PPNGs communicate with each other (Peer-to-Peer Communication, P2P) through the R and S IONets.

P2P communication can fail due to the following reasons:

1. Either one of the Embedded PPNGs is not booted up or has not passed the SEQUENCING state.

2. The Embedded PPNGs are not communicating on both R and S IONets due to IONet failure.

If P2P communication fails, the Embedded PPNG diagnostic alarm 165, *Redundant PPNG Peer-to-Peer Communication Timeout*, is generated. (For more information, refer to alarm 165 in the section *PPNG Specific Alarms*).

Of the two Embedded PPNGs, one Embedded PPNG is designated as the Primary and the other is designated as the Backup.

During Primary and Backup switch-over, MRP switch devices are not considered.

During primary switch-over, the PROFINET Device Status in ToolboxST may indicate *Primary Not Available* for the devices.

For an Embedded PPNG to be designated as Primary, one of the following conditions must be met:

- The Embedded PPNG is in CONTROLLING state, P2P is healthy, and at least one PROFINET device is connected to it.
- The Embedded PPNG is in CONTROLLING state, P2P is un-healthy, and all configured PROFINET devices are connected to it.

For an Embedded PPNG to be designated as Backup, one of the following conditions must be met:

- The Embedded PPNG has no PROFINET devices connected to it.
- The Peer Embedded PPNG is in Primary state.

For an Embedded PPNG to be designated as Primary Switch-over, one of the following conditions must be met:

- The Embedded PPNG has received the Primary Switch-over command from the user through ToolboxST.

Note Prior to issuing a Primary Switch-over command, the user must ensure that the Backup Embedded PPNG has devices connected to it.

- The Embedded PPNG has lost all PROFINET devices and the Peer Embedded PPNG has PROFINET devices connected to it.
- The Embedded PPNG has lost all PROFINET devices and P2P is un-healthy.

1.1.9.8 PROFINET I/O Device Diagnostics

PROFINET I/O devices (Slaves) provide alarm and event messages to the Embedded PPNG. After they are viewed, these Slave device messages can be reset from the ToolboxST application. However, PROFINET Slave device alarms and events are not forwarded to the Mark VIe controller or the WorkstationST Alarm Viewer. The following table defines the Slave device message types supported by the Embedded PPNG.

Supported Slave Device Alarm Types

Alarm	Type
0x0001	Diagnosis
0x0003	Pull
0x0004	Plug
0x0005	Status
0x0006	Update
0x0008	Controlled by Supervisor (Logical Pull)
0x0009	Released (Logical Plug)
0x000A	Plug Wrong Sub-module
0x000B	Return of Sub-module
0x000C	Diagnosis Disappears
0x000E	Port data change notification
0x0011	Network component problem notification
0x0013	Dynamic frame packing problem indication
0x0016	Multiple Interface mismatch notification

1.1.9.9 Embedded PPNG Diagnostics

Ring Break Diagnostic Alarm

In a Ring configuration (with MRP), the ring may be broken due to PROFINET device failures or Ethernet cable faults. However, there is no specific diagnostic generated for this event. To receive notification of a Ring Break status, the user can attach an application variable to the Ring Break status enabled for alarm.

➢ To attach an alarm variable to the Ring Break status

1. From the Embedded PPNG configuration, navigate to the GLM PROFINET device configured as Media Redundancy Manager (MRM).
2. Click Slot 4 (MRP Group 1) for the GLM PROFINET device.
3. Attach an application variable to the variable **Input-0001_3**. If the ring is broken, this variable value becomes False. If the ring is connected, the variable value is True.
4. Set the application variable property to *Alarmed* and set the property **Alarm On Zero** to *True*.

Hot Backup Embedded PPNG Diagnostic Alarm

When the Embedded PPNG in a Hot Backup configuration is unable to communicate with the Peer Embedded PPNG, diagnostic alarm 165, *Redundant PPNG Peer-to-Peer Communication Timeout*, is generated. For possible causes and solutions to resolve this issue, refer to alarm 165 in the section *PPNG Specific Alarms*.

Common Diagnostic Alarms

For diagnostic alarms that are shared between the Embedded PPNG module and the PPNG module, refer to the section *PPNG Specific Alarms*.

1.1.10 UCSC Embedded EtherCAT Controller

The UCSCH1C contains an embedded EtherCAT Master, which maps I/O from EtherCAT Slave devices to the Mark VIe controller. It connects to an EtherCAT device network, enabling communication with EtherCAT I/O devices. It provides a mechanism to import EtherCAT Network Information (ENI) files to configure and operate an EtherCAT I/O device network in either Line or Ring topologies.

EtherCAT features include:

- One or two RJ-45 shielded-twisted pair 100 Mbps port(s) for EtherCAT communication
- Support for Line (only one connection to UCSCH1C), Ring (closed loop with two connections to UCSCH1C), or mixed EtherCAT network topologies
- EtherCAT I/O device configuration by importing an existing ENI file
- Cyclic exchange of input and output data from EtherCAT I/O devices, synchronous with Mark VIe controller frame
- I/O values are displayed and modified in the ToolboxST application

TwinCAT®, or another EtherCAT network configuration tool, is required to generate an ENI file. Using the ToolboxST application, this ENI file is imported to create the Mark VIe configuration. Any change made to the configuration of attached EtherCAT devices requires a new configuration file to be imported into ToolboxST. (Refer to the *ToolboxST User Guide for Mark Controls Platform*, GEH-6703, the section *EtherCAT Tab*, for ToolboxST configuration details.) After initial configuration, a local variable can be connected to a particular I/O point from EtherCAT device I/O and used in the Mark VIe controller application logic.

1.1.10.1 Embedded EtherCAT Controller Specifications

Attention

The UCSCH1C controller and the EtherCAT Master operate at a fixed period of 10 ms. Adjust device timeouts, watchdogs, and state transitions within your EtherCAT network configuration tool accordingly.

Item	EtherCAT Specification
Conformance class version	EtherCAT Class B I/O controller
Supported Ethernet cabling	Cat 5e STP
I/O device data update rates	Synchronous updates once per Mark VIe frame (10 ms)
Maximum I/O memory	16 KB
Max number of EtherCAT I/O devices attached to UCSC	Limited to 512 devices
Supported network topology	Line (daisy-chain with UCSC at one end of the bus), Ring (daisy-chain with UCSC at both ends of the bus), or a combination through junction devices
Network speed	100 Mbps full-duplex on dedicated EtherCAT network
Media redundancy	Supported with ports ENET2 and T/SL3

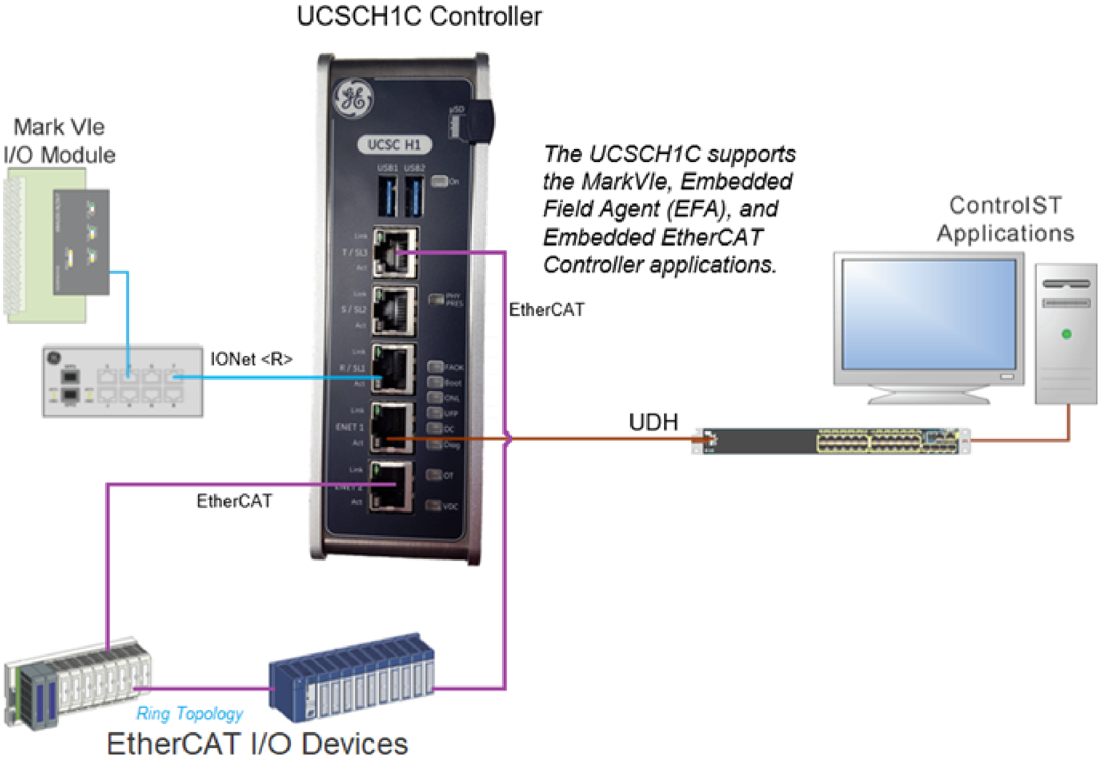
1.1.10.2 EtherCAT Network Configuration

The UCSCH1C EtherCAT controller communicates with EtherCAT I/O devices connected through an Cat 5e shielded-twisted pair Ethernet cable. Devices are configured with TwinCAT or a comparable EtherCAT network configuration utility capable of exporting ENI files. The ENI file contains the information required to establish communication with EtherCAT I/O devices, perform configuration and startup, and exchange cyclic data.

➢ **To set up the EtherCAT network**

1. Open TwinCAT, or a comparable EtherCAT network configuration utility.
2. Add all EtherCAT I/O devices that will be connected to this network.
3. Configure the appropriate I/O types, scaling, and sample period for this control application.
4. When the network configuration is complete, export the ENI file.
5. From the ToolboxST application, configure the EtherCAT network. Refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703), the section *EtherCAT Tab* for configuration procedures.
   a. Import the ENI file into ToolboxST configuration by right-clicking on the EtherCAT Master node and selecting **Import ENI File**. This imports the network configuration and creates the Mark VIe signal space map required to exchange data with the EtherCAT I/O devices.
   b. Configure Cable Redundancy and Frame Loss Limit for this network.
   c. Perform a Build and Download the configuration to the Mark VIe controller.

Network Topology



Typical Embedded EtherCAT Network Topology (Ring)

1.1.10.3 Dataflow

The UCSCH1C EtherCAT controller exchanges data with the control system at standard Mark VIe controller frame rates in synchronization with the control frame. EtherCAT data exchanges with EtherCAT I/O devices is determined by the ENI file created with the EtherCAT network configuration tool (such as TwinCAT). Refer to the section *EtherCAT Network Configuration* for details.

Note EtherCAT network performance is determined by the cyclic data exchanges defined by the EtherCAT network configuration tool. To achieve the highest performance, users should minimize the quantity of packets required to exchange process data.

1.1.10.4 EtherCAT Network Communication

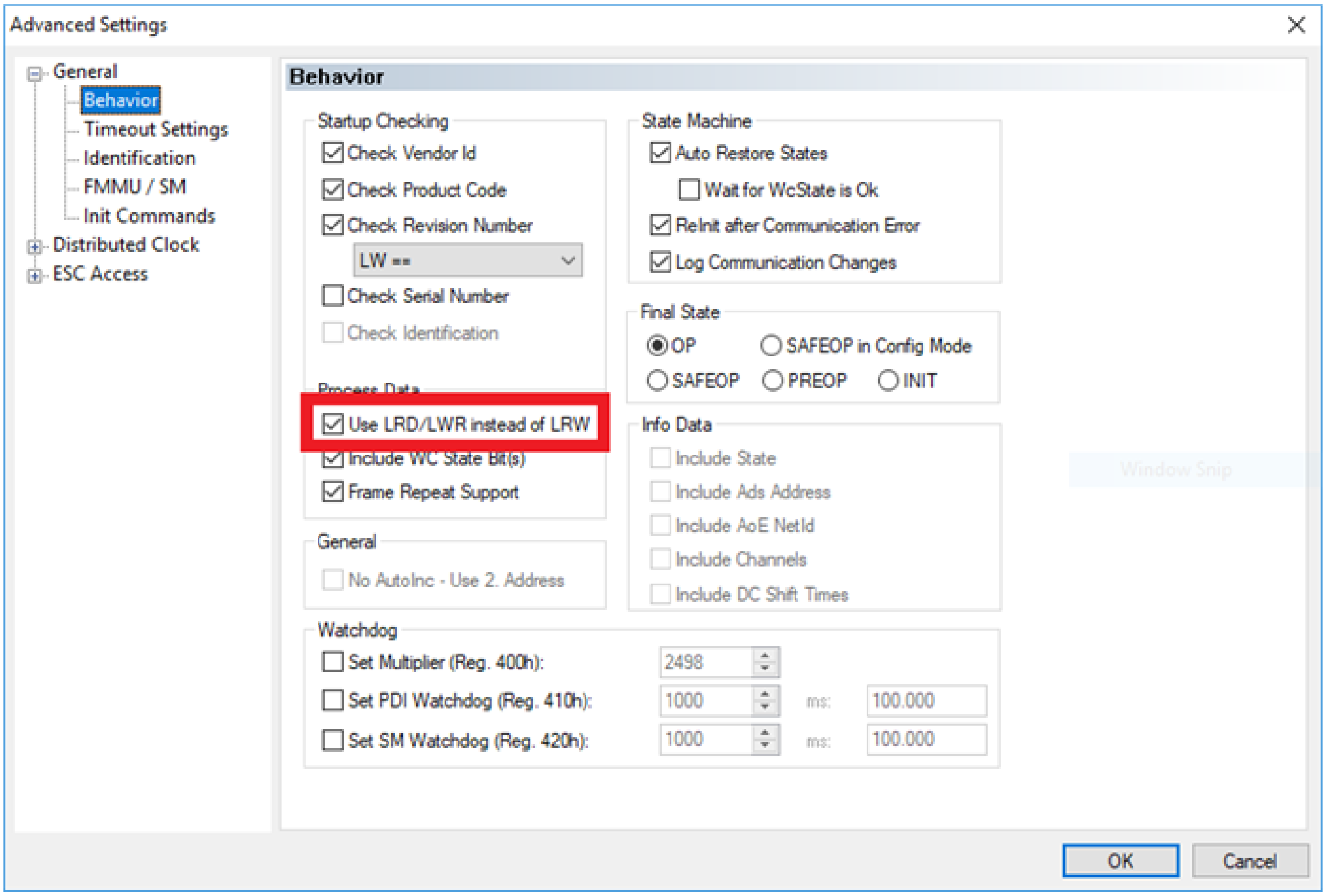
A typical EtherCAT network has the following components:

- **EtherCAT I/O controller** – the UCSCH1C controller establishes communication with EtherCAT I/O devices according to the configured network layout in the ENI file.
- **EtherCAT I/O devices** – are distributed I/O devices hosting various data types that communicate with the Mark VIe controller.

Switches (managed or unmanaged) are not recommended on EtherCAT networks. EtherCAT I/O devices will be advanced from Init (power-on) state to Operational state according to the commands in the ENI file. The EtherCAT I/O devices maintain a current Operating state, which can be read using the OpState variable type. An OpState variable is automatically created for each EtherCAT Slave device and can be read by the Mark VIe application.

The EtherCAT network configuration tool defines the cyclic data exchanges according to customer parameters. Under some conditions, such as utilizing devices with large process data maps, data exchanges can grow larger than standard Ethernet frames or generate a large volume of Ethernet packets. In systems with large applications, users should attempt to minimize the number and size of cyclic data exchanges. This can be accomplished by removing devices, removing unused variables from the process data map, and utilizing Read/Write commands (LRW) if the network topology supports it.

Redundant operation requires that Logical Read/Write (LRW) commands not be used by multiple devices on the same sync unit. It is strongly advised that users that have configurations using cable redundancy replace LRW commands with Logical Read/Logical Write (LRD/LWR). This is accomplished in the Advanced Settings menu for devices in many EtherCAT network configuration tools.



Behavior

Startup Checking
☑ Check Vendor Id
☑ Check Product Code
☑ Check Revision Number
LW ==
☐ Check Serial Number
☐ Check Identification

Process Data
☑ Use LRD/LWR instead of LRW
☑ Include WC State Bit(s)
☑ Frame Repeat Support

General
☐ No AutoInc - Use 2. Address

State Machine
☑ Auto Restore States
☐ Wait for WcState is Ok
☑ ReInit after Communication Error
☑ Log Communication Changes

Final State
● OP ○ SAFEOP in Config Mode
○ SAFEOP ○ PREOP ○ INIT

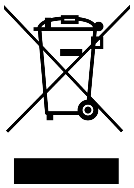
Info Data
☐ Include State
☐ Include Ads Address
☐ Include AoE NetId
☐ Include Channels
☐ Include DC Shift Times

Watchdog
☐ Set Multiplier (Reg. 400h): 2498
☐ Set PDI Watchdog (Reg. 410h): 1000 ms: 100.000
☐ Set SM Watchdog (Reg. 420h): 1000 ms: 100.000

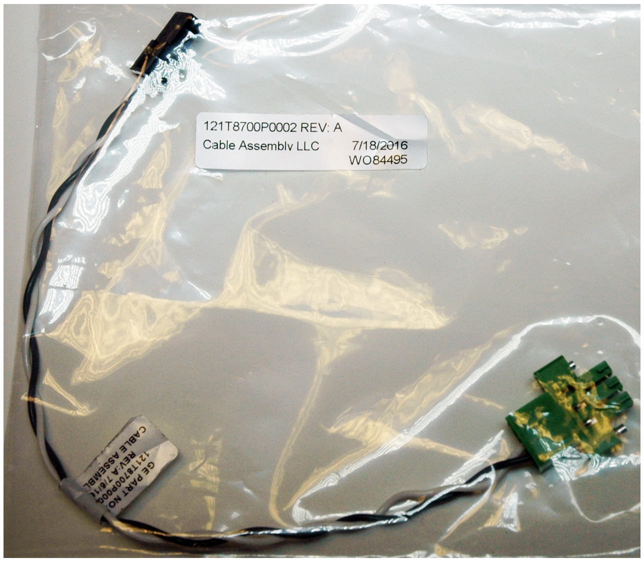
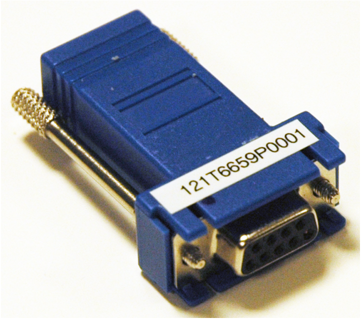
LRW Command Replacement in Advanced Settings

1.1.11 UCSC and UCEC Agency Certifications and Standards

Refer to the *UCSC Installation and Maintenance Requirements (IMR)* (GFK-3006) for conformance to these standards.

Description	Marking	Comments
North America Safety for Programmable Controller for use in Hazardous locations	c UL US LISTED	ISA 12.12.01: 2015, Class I Div. 2 Groups ABCD, UL 60079-0 Ed 6.0 (2013), Class I, Zone 2 Gas Group ABCD, UL 60079-15 Edition 4.0 (2013), [Ex nA] CSA C22.2 No. 213-15, CAN/CSA-C22.2 NO. 60079-0:15, Class I, Zone 2, CAN/CSA-C22.2 NO. 60079-15:12
EMC Directive European Restriction of Hazardous Substances (RoHS)	CE	IEC/EN 61131-2: 2007(sections 8-10, Zone B), IEC/EN 61000-6-2: 2005 Ed 2.0, IEC/EN 61000-6-4: 2006 Ed 2.0, CISPR 11:2009 +A1: 2010 / EN 55011: 2009 +A1: 2010, CISPR 22: 2010 / EN55022: 2010/AC:2011 (Class A), CISPR 24: 2010 / EN55024: 2010, IEC/EN 61131-2: 2007 (sections 4 & 6), IEC 61000-4-18: 2006 / EN 61000-4-18: 2007 (refer to IEC61131-2: 2007 Annex D for levels)
European Safety for Explosive Atmosphere, ATEX Directive	Ex	Category 3 equipment - [II 3 G], EN 60079-0: 2012 A+11:2013, EN 60079-7: 2015 [Type of Protection Ex ec]
European Waste & Collection		Compliance with European WEEE Directive 2012/19/EU
China Restriction of Hazardous Substances	25	Compliance with "Management Methods for the Restriction of the Use of Hazardous Substances in Electrical and Electronic Products". (Jan 21, 2016) Declaration Table provided with equipment.
Environmental	No Marking	IEC/EN 61131-2: 2007 (sections 5 & 6) Storage: Dry Heat - IEC 60068-2-2: 1974 test Bb (70°C at 16hrs, unpowered), Cold Temp - IEC 60068-2-1: 2007 test Ab (-40°C at 16hrs, unpowered Sinusoidal Vibration: DIN EN 60068-2-6: (Edition 10/08) (test Fc) Shock: DIN EN 60068-2-27: (Edition 2/10) (test Ea)

1.1.12 Accessories

Part Number	Description
121T8700P0002	UCSB to UCSC Power Cable Adapter 
127T2669P0001	UCSB/CSLA (151X1235BC01SA##) to UCEC Module Power Cable Adapter
121T6659P0001	UCSC COM Port Adapter (RJ-45 to DB9F) 

1.1.13 UCSC Hardware Replacement

Replacement parts may contain static-sensitive components. Therefore, GE ships replacement parts in anti-static bags. When handling electronics, make sure to store them in anti-static bags or boxes and use a grounding strap.

Caution

To prevent component damage caused by static electricity, treat all boards with static-sensitive handling techniques. Wear a wrist grounding strap when handling boards or components, but only after boards or components have been removed from potentially energized equipment and are at a normally grounded workstation.

Warning

In addition to information provided here, always follow all wiring and safety codes that apply to your area or your type of equipment. For example, in the United States, most areas have adopted the National Electrical Code standard and specify that all wiring conform to its requirements. In other countries, different codes will apply. For maximum safety to personnel and property you must follow these codes. Failure to do so can lead to personal injury or death, property damage or destruction, or both.

➢ To replace the UCSC with another UCSC

1. Loosen the screws holding the power connector in place.
2. Disconnect the power connector from the controller.
3. Disconnect all Ethernet cables (note which cable is connected to which port).
4. Loosen the screws holding the controller in place. The mounting is a keyhole design.
5. Remove the controller by lifting to align the large portion of the keyhole with the mounting screws and pull forward.
6. Verify that the hardware revision of the old UCSC is the same or compatible with the new UCSC for its particular application.
7. Reinstall the new controller by reversing steps 2 through 4. Do not apply power yet.
8. Perform the UCSC Restore procedure to initialize the new controller.
9. If restore was not successful, configure the new controller’s UDH network address.
10. Use the ToolboxST application to Build and Download to the controller as needed. Refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703), the section *Download to Controller* for instructions.

1.1.14 UCSC Restore

After installing a replacement controller, perform the following procedure to apply the configuration to the UCSC controller and allow communication between the UCSC and the ToolboxST application. The Physical Presence (PHY PRES) button located on the front of the controller is used to initiate the procedure.

Note The UCSC, as shipped from the factory, does not include the software on the controller to support communication from the PHY PRES button to the EFA. The user needs to download to the controller at least once (using ToolboxST) to enable this.

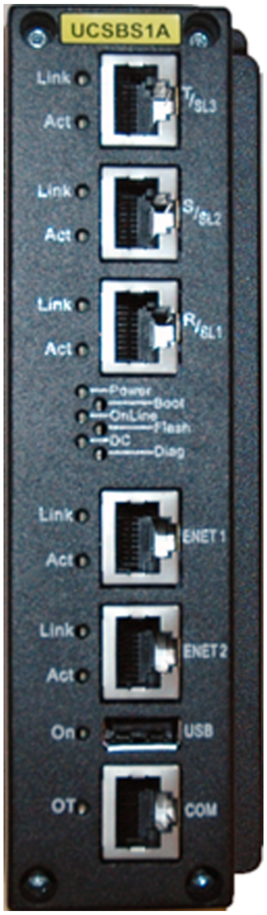
➢ **To perform UCSC restore**

1. From the ToolboxST Component Editor **Device** menu, select **Download**, then select **Controller Setup**.
2. When the Controller Setup Wizard *Welcome* window displays, click **Next**.
3. Select **Initialize USB Flash Device**, then click **Next**.
4. Insert a non-encrypted USB 2.0 (only) flash device with a 4 GB minimum capacity into the HMI computer USB port.
5. Click **Scan** and select the listed flash drive.
6. Select the correct **Channel** (R, S, or T if using redundant controllers).
7. Click **Write**, then click **Next**.
8. Complete the controller restore process using the instructions provided on the *Controller Setup Wizard* window or using the remaining steps in this procedure.
9. Remove the USB flash device from the HMI computer.
10. Remove power from the controller.
11. Insert the USB flash device into either USB port of the controller.
12. Press and hold in the **PHY PRES** button, and apply power to the controller. Continue to hold in the PHY PRES button until the USB **On LED** is lit (~ 15 seconds).
13. Release the PHY PRES button and wait for the process to complete. (The USB On LED remains lit to indicate the restore is in progress. The procedure takes one to two minutes.) When the LED turns off, the restore has completed successfully.

   Note If the LED flashes at a 1 Hz rate, a failure has occurred. Retry or remove the USB flash device.

14. Remove the USB flash device from the controller.
15. Cycle power on the controller.
16. From the ToolboxST *Controller Setup Wizard* window, click **Finish**.
17. Perform a **Download** to bring the controller back online and in the controlling state.

1.2 UCSB Controllers



The UCSB controllers are stand-alone computers that run the application code. The controller mounts in a panel, and communicates with the I/O packs through on-board I/O network (IONet) interfaces. IONet is a private special-purpose Ethernet that only supports Mark* controls I/O modules and controllers. The controller operating system (OS) is QNX Neutrino, a real time, multitasking OS designed for high-speed, high-reliability industrial applications. Unlike traditional controllers where I/O is on a backplane, the UCSB controller does not host any application I/O. Also, all I/O networks are attached to each controller providing them with all input data. The hardware and software architecture guarantees that no single point of application input is lost if a controller is powered down for maintenance or repair.

The Mark VIeS UCSBS1A Safety controller and Safety I/O modules are used for functional safety loops to achieve SIL 2 and 3 capabilities. Mark VIeS Safety equipment is used by operators knowledgeable in safety-instrumented system (SIS) applications to reduce risk in critical safety functions. Safety controllers and distributed I/O modules are programmed specifically for safety control use, and this specific control hardware and software has IEC 61508 certification.

The UCSB controllers offer the following advantages:

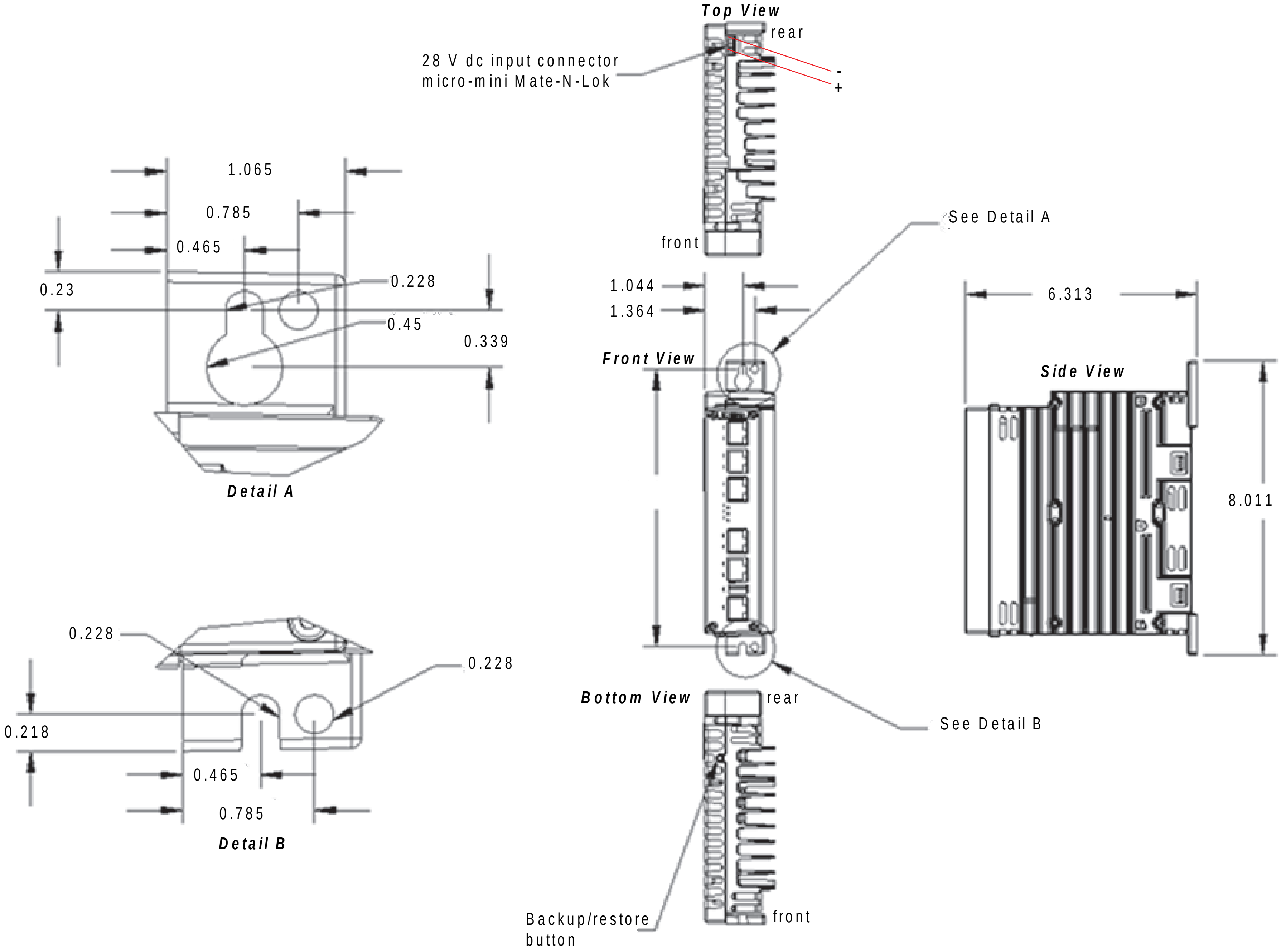
- Single module
- Built-in power supply
- No jumper settings required
- No battery
- No fan (UCSBS1A, UCSBH1A, UCSBH4A)
- Dual-redundant fans with IS420UCSBH3A
- Smaller panel footprint
- Flash memory can be conveniently updated

1.2.1 UCSB Specifications

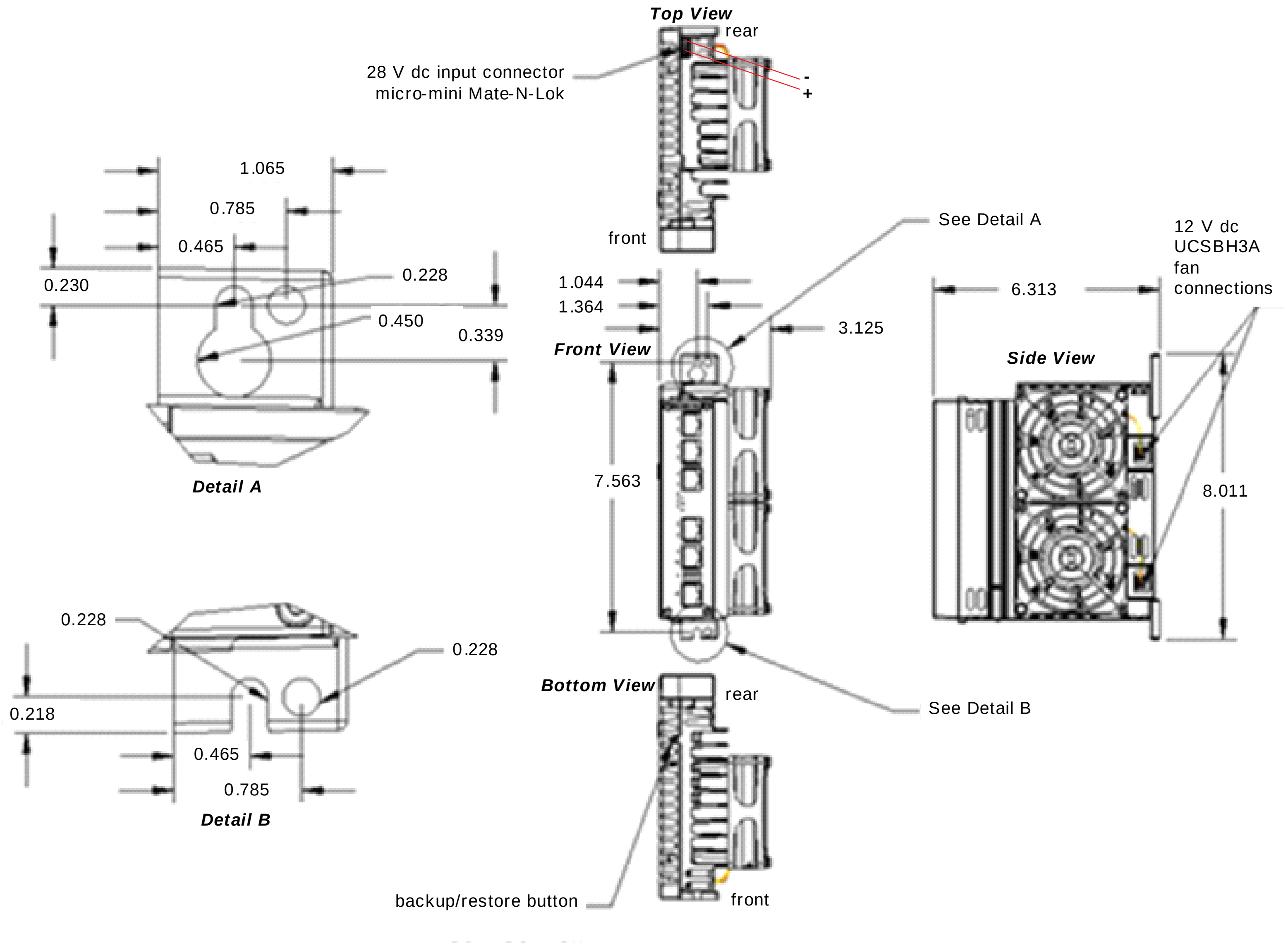
Item	UCSB Specification
Microprocessor	UCSBH1A and UCSBS1A: 600 MHz Intel EP80579
	UCSBH3A: 1200 MHz Intel EP80579
	UCSBH4A: 1066 MHz Intel EP80579
Memory	256 MB DDR2 SDRAM with error-correcting code (ECC) Flash-backed SRAM 8K allocated as NVRAM for controller functions (*Mark VIe control only*) NAND flash size is 2 gigabytes
Operating System	QNX Neutrino
Programming	Control block language with analog and discrete blocks; Boolean logic represented in relay ladder diagram format. Supported data types include: • Boolean • 16-bit signed integer • 16-bit unsigned integer • 32-bit signed integer • 32-bit unsigned integer • 32-bit floating point • 64-bit long floating point
Primary Ethernet Interface, ENET1	Twisted pair 10Base-TX/100Base-TX, RJ-45 connector TCP/IP protocol used for communication between controller and the ToolboxST application TCP/IP protocol used for alarm communication to HMIs EGD protocol for application variable communication with CIMPLICITY HMI and Series 90-70 PLCs
Secondary Ethernet Interface, ENET2 (***not supported for Mark VIeS control***)	Twisted pair 10Base-TX/100Base-TX, RJ-45 connector Ethernet Modbus, OPC UA, or CDH
IONet Ethernet Interface (3 ports)	Twisted pair 10Base-TX/100Base-TX, RJ-45 connectors: • TCP/IP protocols used to communicate between controllers and I/O modules • IONet redundancy is equal to controller redundancy • Red, black, and blue Ethernet cables connect from controllers to IONet switches
COM1	This is an optional setup for the controller IP address, instead of using the flash drive. For cabling use GE-provided Ethernet cables, which are specifically designed for use in the Mark controller product family (GE part #342A4944P1).
Power Requirements	UCSBH1A and UCSBS1A: 26.7 W peak, 15.6 W nominal
	UCSBH3A: 28.7 W peak, 17.3 W nominal
	UCSBH4A: 28.7 W peak, 17.3 W nominal
Weight	UCSBH1A and UCSBS1A: 2.4 lbs (1 Kg)
	UCSBH3A: 2.9 lbs (1.3 Kg)
	UCSBH4A: 2.4 lb (1 Kg)
† Ambient rating for enclosure design	UCSBHIA and UCSBS1A: -30 to 65°C (-22 to 149 °F)
	UCSBH3A: 0 to 65°C (32 to 149 °F)
	UCSBH4A: -30 to 65°C (-22 to 149 °F)
† Refer to GEH-6721_Vol_I, the chapter Technical Regulations, Standards, and Environments for additional equipment rating information depending on application requirements.	

1.2.2 UCSB Installation

The controller is contained in a single module that mounts directly to the panel sheet metal. The following diagrams display the module envelope and mounting dimensions. All dimensions are in inches. The UCSB is to be mounted to the panel as shown with vertical air flow through the fins to be unobstructed.

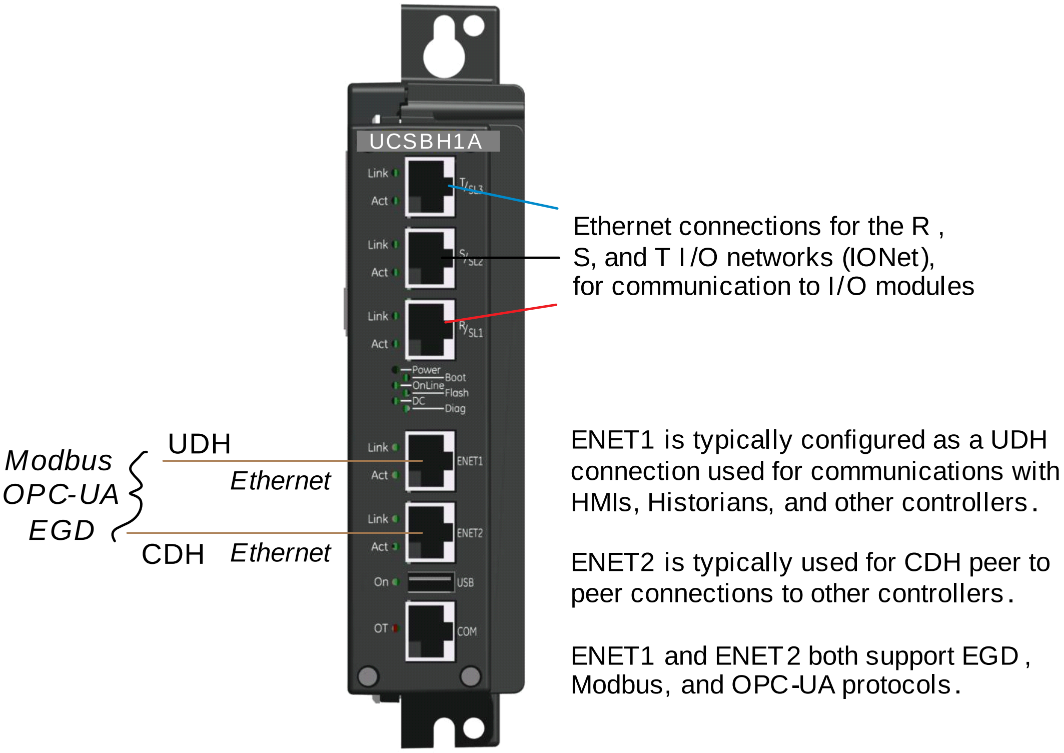


Mark VIeS UCSBS1A, Mark VIe UCSBH1A, H4A Envelope & Mounting Dimensions



Mark VIe UCSBH3A Envelope and Mounting Dimensions

The following communication ports provide links to I/O, operator, and engineering interfaces from the Mark VIe controller:



Ethernet connections for the R, S, and T I/O networks (IONet), for communication to I/O modules

ENET1 is typically configured as a UDH connection used for communications with HMIs, Historians, and other controllers.

ENET2 is typically used for CDH peer to peer connections to other controllers.

ENET1 and ENET2 both support EGD, Modbus, and OPC-UA protocols.

Typical Ethernet Connections

Note The Mark VIeS Safety controller does not use any CDH network, nor does it allow for OPC-UA.

OPC-UA from the Mark VIe controller requires firmware version 5.01 or later.

1.2.3 UCSB Software and Communications

The controller is loaded with software specific to its application. It can run rungs or blocks. Minor modifications to the control software may be made online without requiring a restart. The IEEE 1588 protocol is used through the R, S, and T IONets to synchronize the clock of the I/O packs and controllers to within ±100 microseconds. External data is transferred to and from the control system database in the controller over the R, S, and T IONets. This includes process inputs/outputs to the I/O modules.

In a dual system, this also includes:

- Internal state values and initialization information from the designated controller
- Status and synchronization information from both controllers

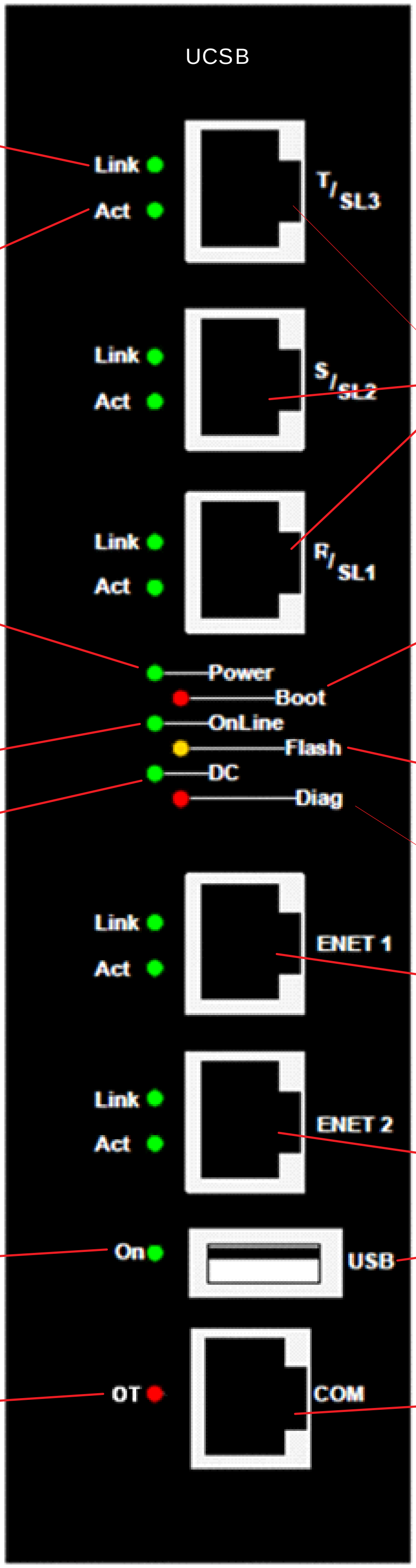
In a triple modular redundant (TMR) system, this also includes:

- Internal state values for voting and status, and synchronization information from all three controllers
- Initialization information from the designated controller

1.2.3.1 Mark VIeS Safety Controller Software Branding

If the Mark VIeS Safety controller application code is changed and downloaded, then a Branding of the new code is required. Changes that are not downloaded may cause a Brand change. Refer to *GEH-6723, Mark VIeS Safety Control Safety Instruction Guide*, the section, *Application Code Branding*. This feature is a requirement for functional safety.

1.2.4 UCSB LEDs and Connections



Link
solid green = Ethernet link has been established with the IONet switch

Act
solid green = IONet packet traffic
Flashing green = traffic is low

Power
solid green = internal 5 V supply is on and regulating The UCSB converts the incoming 28 V dc to 5 V dc. All other internal power planes are derived from 5 V.

OnLine
solid green = controller is online and running application code

DC
solid green = this is the designated controller

On
solid green = USB is active

OT over-temperature
Yellow = alarm is present
Red = trip has occurred

Ethernet connections for R, S, and T I/O networks (IONet)

Boot
solid red = startup in process
off = startup has completed
flashing red = an error is detected
flashes red once every 3 seconds = Baseload signature verification has failed

Flash
flashing **amber** = a flash device is being accessed

Diag flashing red = Active diagnostic alarm

Ethernet connection to (UDH for communication with HMI)

Provides optional CDH, OPC UA, or Modbus TCP/IP (***not supported for Mark VIeS control***)

USB connection used during initial setup of controller UDH IP address and for the backup/restore function

Used by GE during development process or for alternate IP address setup

1.2.5 UCSB Boot LED

The boot LED is lit continuously during the boot process unless an error is detected. If an error is detected, the LED flashes at a 1 Hz frequency. The LED, when flashing, is on for 500 ms and off for 500 ms. After the flashing state, the LED turns off for three seconds. The number of flashes indicates the failed state.

If the flash image is valid but the runtime firmware has not been loaded, the boot LED flashes continuously at a 1 Hz rate. Once the firmware is loaded, the boot LED turns off. If the controller does not go *online*, use the ToolboxST application to determine why the controller is blocked. Once an IP address has been assigned, ToolboxST application uses the Ethernet for configuration.

UCSB Boot LED Flashing Codes

State	Description	# of Flashes
Executing BIOS	Normally booting BIOS	On
Failed SPD	SPD has bad data	1
Failed DRAM	DRAM memory test has failed in the BIOS	2
Failed BIOS SPI	BIOS was unable to validate the BIOS SPI checksum	3
Failed CPLD	BIOS was unable to communicate with the complex programmable logic device (CPLD)	4
Failed APP SPI	BIOS was unable to communicate with the APP SPI	5
Failed QNX IFS	BIOS was unable to read or verify the QNX IFS image	6
Fully Booted	Fully Booted	Off

1.2.6 Transfer IP Address to UCSB Controller

For the software configuration procedure, refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703), the chapter *Controller Setup*, the section *Configure and Transfer IP Address to UCSB / UCSC Controller*.

1.2.7 UCSB Controller Replacement

Warning

To prevent personal injury or equipment damage caused by equipment malfunction, only adequately trained personnel should modify the following equipment.

Caution

Verify the controller being replaced has a RED LED. A RED LED indicates the controller is in a fault condition and is the one that needs to be replaced. Ensure the remaining two control loops are free of faults or alarms before proceeding. A failure on one of the remaining loops could cause a turbine trip.

Attention

If the Mark* VIe controller interfaces with a SecurityST* platform and Secure Mode is implemented on the controller, then the controller cores should be taken out of Secure Mode prior to executing this maintenance procedure. Once maintenance has been completed, the Mark VIe controller cores should be placed back into Secure Mode.

Note Maintenance of this component may cause loss of communication, loss of power, and a small change in valve position. When the portion of the null bias for the PSVO or PSVP I/O pack is lost, the valve might move slightly in the direction of the spring bias.

Note Refer to the Mark VIe site-specific wiring documentation for the UCSB power and communication connections. Main unit applications use three JPDCs, and feed pump turbine applications only use one JPDC in their power distributions.

Note Before performing this procedure, obtain the controller connector (serial port to Ethernet adapter, GE Part Number 342A4944P1) and an Ethernet cable long enough to connect from the controllers to a Mark VIe engineering workstation with access to the turbine controller software.

➢ To replace the Mark VIe UCSBHxx or Mark VIeS UCSBS1A

1. If possible, back up the old UCSB’s NAND flash.
2. Disconnect the power plug JCR on the associated JPDC for the controller being replaced:
   a. For <R> controller, plug JCR.
   b. For <S> controller, plug JCS.
   c. For <T> controller, plug JCT.
3. Disconnect the IONet cables.
4. Disconnect the VLAN cable.
5. Loosen the screws holding the controller in place. The mounting is a keyhole design.
6. Remove the controller by lifting to align the large portion of the keyhole with the mounting screws and pull forward.
7. Install the replacement controller by lining up the large open portion of the keyhole with the mounting screws and pushing it flush with the mounting backplane. Slide the replacement controller down so that the smaller portion of the

keyhole holds the controller in place. Tighten the mounting screws to firmly hold the controller in place. Do not apply power yet.

8. Connect the VLAN cable per its wire label or in accordance with the Mark VIe site wiring documentation.
9. Connect the IONet cables per their wire labels or in accordance with the Mark VIe site wiring documentation. Connect the power to the replacement controller per the controller power wire label or the Mark VIe site wiring documentation.
10. Connect the controller connector to one end of the Ethernet cable. Connect the controller connector to the engineering workstation.
11. Connect the opposite end of the Ethernet cable to the COM port on the replacement controller.
12. Update the replacement UCSB's NAND flash with the backup from step 1.
13. If backup/restore was not successful, configure the new controller’s TCP/IP address. Refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703), the section *Controller Setup*.

1.2.8 UCSB Backup and Restore

If the UCSB controller fails, back up the UCSB configuration (including the UDH IP address), install a replacement controller, and restore the configuration to the replacement UCSB to allow for communication to the ToolboxST application. A software recovery push-button located on the bottom of the controller is used to update the NAND flash. A 2.0-compliant, non-encrypted USB with a minimum capacity of 4 GB must be used.

➢ **To perform a UCSB backup**

Note If a serial terminal is connected to the UCSB, open the Microsoft Hyperterminal program to display backup and restore status.

1. Insert a FAT32 DOS-formatted USB drive into the front USB port on the UCSB. The USB device must be USB 2.0-compliant, non-encrypted, with a minimum capacity of 4 GB.
2. From the bottom of the UCSB, press and hold in the backup/restore button until the USB *On* LED is lit.
3. Release the button and wait while the LED remains lit and the backup is in progress. The LED turns off when the backup completes successfully.
4. Remove the USB drive.
5. If the LED flashes at a 1 Hz rate, a failure has occurred. Remove the USB drive or retry.

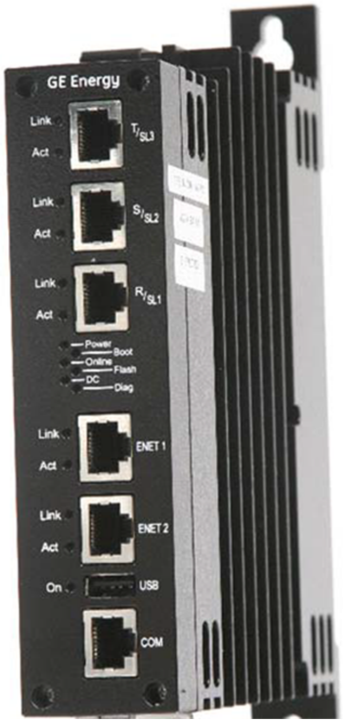
➢ **To perform a UCSB restore**

1. Remove power from the UCSB.
2. Insert the backed-up USB drive into the USB port.
3. Press and continue to hold in the backup/restore button, apply power to the UCSB, and continue to hold in the backup/restore button until the USB *On* LED is lit.
4. Release the button and wait while the LED remains lit and the restore is in progress. The LED turns off when the restore completes successfully.
5. Remove the USB drive.

Note If the LED flashes at a 1 Hz rate, a failure has occurred. Remove the USB drive or retry.

6. After a restore, a download from ToolboxST may be required to bring the controller back online and in the controlling state.

1.3 UCSA Controller

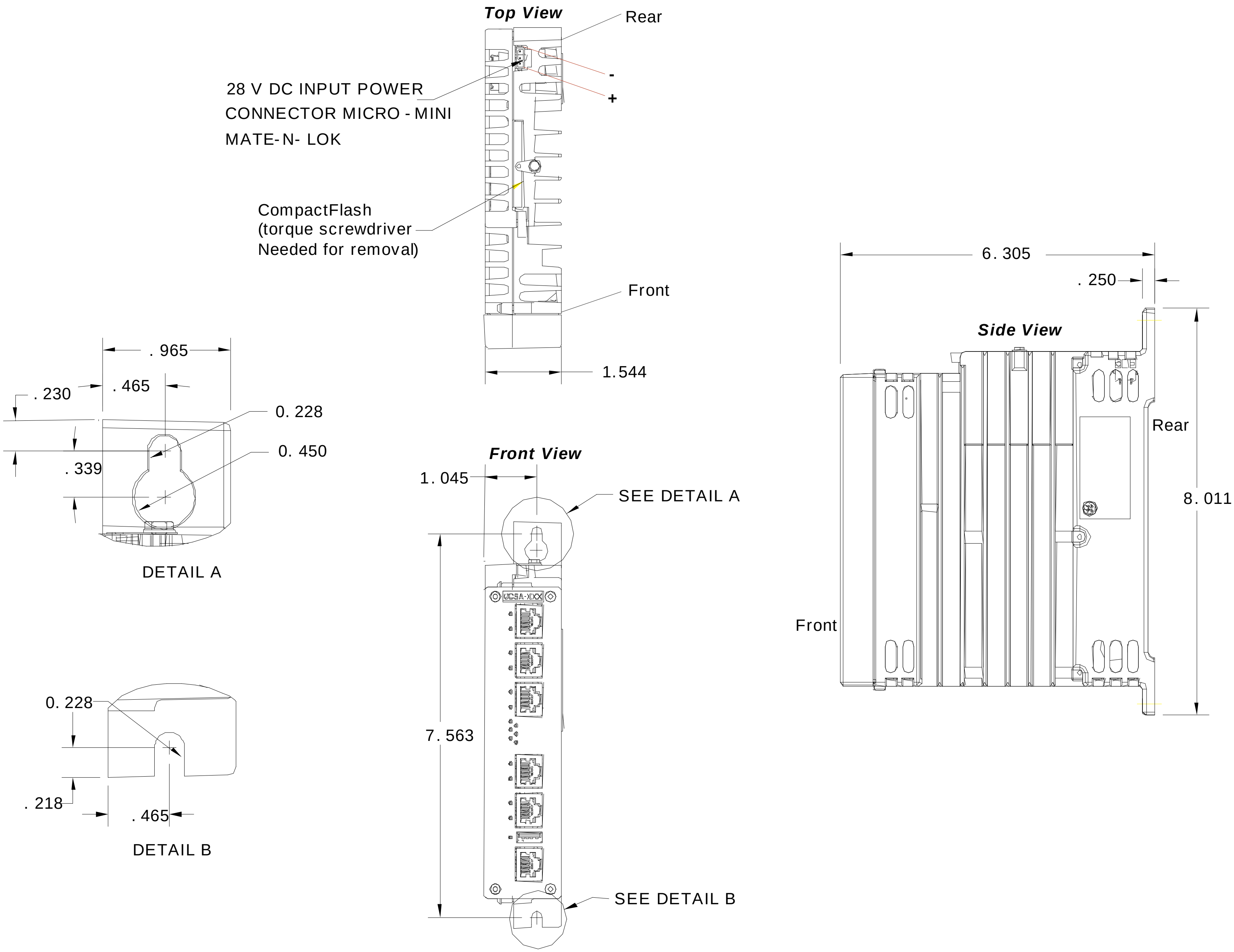


The UCSA controllers are stand-alone computers that run the application code. The controller mounts in a panel and communicates with the I/O packs through on-board I/O network (IONet) interfaces. The I/O networks are private special-purpose Ethernet that support only the I/O modules and the controllers. The controller operating system (OS) is QNX Neutrino, a real-time multitasking OS designed for high-speed, high-reliability industrial applications.

Unlike traditional controllers where I/O is on a backplane, the UCSA controller does not host any application I/O. Also, all I/O networks are attached to each controller providing them with all input data. The hardware and software architecture guarantees that no single point of application input is lost if a controller is powered down for maintenance or repair. The UCSA controller uses CompactFlash.

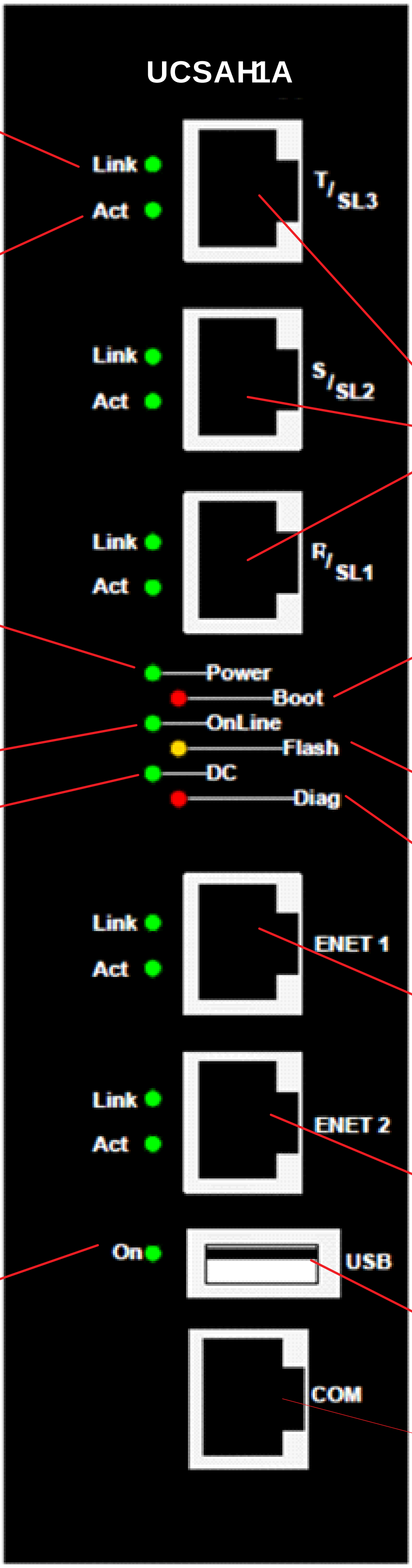
The UCSA controller platform is available for use in many Mark VIe control system applications, including balance of plant controls and some retrofits. It does not have enough processing power, however, for some advanced model-based controls application. The UCSA controller not certified for IEC 61508 Safety Loop usage.

The following figure displays the installation envelope and mounting dimensions for the UCSA controller.



Mark VIe UCSA Controller Envelope and Mounting Dimensions

1.3.1 UCSA LEDs and Connections



Link solid green =
Ethernet PHY has established a link with an Ethernet switch port

Act solid green =
there is packet traffic on an Ethernet interface
Flashing green = traffic is low

Power solid green =
Internal 5 V supply is up and regulating
The UCSA converts the incoming 28 V dc to 5 V dc. All other internal power planes are derived from 5 V.

OnLine solid green =
controller is online and running application code

DC solid green =
this is the designated controller

On solid green =
USB is active

Ethernet connections for R, S, and T I/O networks (IONet)

Boot solid red = startup in process
off = startup has completed
flashing red = an error is detected
flashes red once every 3 seconds = Baseload signature verification has failed

Flash flashes **amber** =
a flash device is being accessed

Diag flashing red =
active diagnostic alarm

Ethernet connection to UDH for communication with HMI

Optional **CDH**

USB connection

COM1 RS-232C
used during initial controller setup

1.3.2 UCSA Boot LED Flash Codes

# of Flashes	Description
1	Failed Serial Presence Detect (SPD) EEPROM
2	Failed to initialize DRAM or DRAM tests failed
3	Failed NOR flash file system check
4	Failed to load FPGA or PCI failed
5	CompactFlash device not found
6	Failed to start IDE driver
7	CompactFlash image not valid

1.3.3 UCSA Specifications

Item	UCSA Specification
Microprocessor	Freescale Power (Power QUICC II PRO 667 MHz)
Memory	256 MB DDR SDRAM Flash-backed SRAM - 8K allocated as NVRAM for controller functions
Flash	128 MB CompactFlash module (GE part #336A5196AAP8) 2 GB CompactFlash module (GE part #336A5196AAP9)
Operating System	QNX Neutrino
Programming	Control block language with analog and discrete blocks; Boolean logic represented in relay ladder diagram format. Supported data types include: • Boolean • 16-bit signed integer • 16-bit unsigned integer • 32-bit signed integer • 32-bit unsigned integer • 32-bit floating point • 64-bit long floating point
Primary Ethernet Interface (2)	Twisted pair 10Base-TX/100Base-TX, RJ-45 connectors: TCP/IP protocol used for communication between controller and the ToolboxST application TCP/IP protocol used for alarm communication to HMIs EGD protocol for application variable communication with CIMPLICITY HMI and Series 90-70 PLCs Ethernet Modbus protocol supported for communication between controller and third-party DCS
IONet Ethernet Interface (3 ports)	Twisted pair 10Base-TX/100Base-TX, RJ-45 connectors: TCP/IP protocols used to communicate between controllers and I/O modules
COM port	One accessible through RJ-45 connector on front panel For cabling use GE-provided Ethernet cables, which are specifically designed for use in the Mark* controller product family (GE part #342A4944P1)
Power Requirements	32 V dc to 18 V dc (12.5 W typical preliminary)
Weight	2 lbs (0.9 Kg)
† Ambient rating for enclosure design	0 to 65°C (32 to 149 °F)
Technical Regulations, Standards, and Environments	† Refer to GEH-6721_Vol_I, the chapter Technical Regulations, Standards, and Environments for additional equipment rating information depending on application requirements.

1.3.4 UCSA Controller Replacement

Warning

To prevent personal injury or equipment damage caused by equipment malfunction, only adequately trained personnel should modify the following equipment.

Caution

Verify the controller being replaced has a RED LED. A RED LED indicates the controller is in a fault condition and is the one that needs to be replaced. Ensure the remaining two control loops are free of faults or alarms before proceeding. A failure on one of the remaining loops could cause a turbine trip.

Attention

If the Mark* VIe controller interfaces with a SecurityST* platform and Secure Mode is implemented on the controller, then the controller cores should be taken out of Secure Mode prior to executing this maintenance procedure. Once maintenance has been completed, the Mark VIe controller cores should be placed back into Secure Mode.

Note Maintenance of this component may cause loss of communication, loss of power, and a small change in valve position. When the portion of the null bias for the PSVO or PSVP I/O pack is lost, the valve might move slightly in the direction of the spring bias.

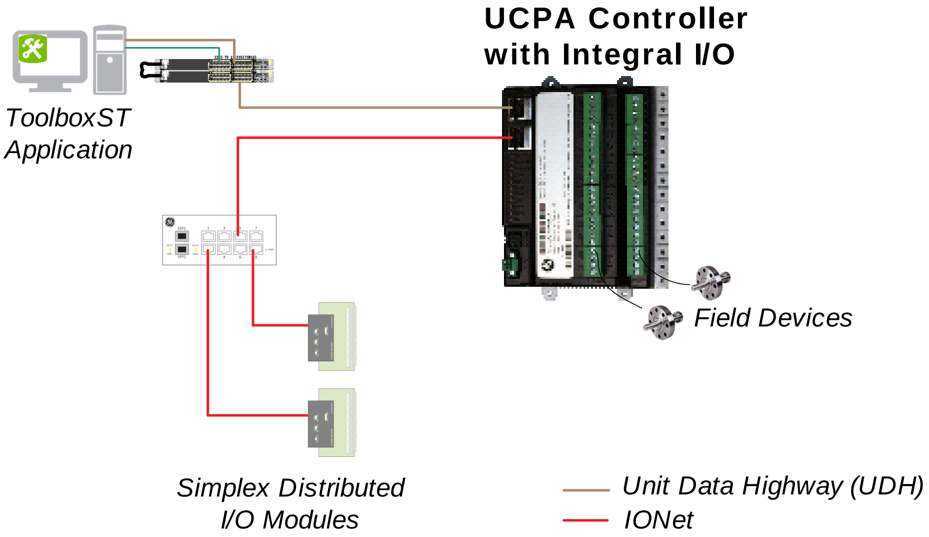
➢ To replace the Mark VIe UCSA Controller

1. Disconnect the power plug JCR on the associated JPDC (or other power distribution board) (for example, UCSA R/JPDC/JCR).
2. Disconnect the IONet cables.
3. Disconnect the VLAN cable.
4. Loosen the screws holding the controller in place. The mounting is a keyhole design. Refer to *Detail A* on the UCSA drawing.
5. Remove the UCSA by lifting to align the large portion of the keyhole with the mounting screws and pull forward.
6. If still functional, remove the CompactFlash® from the old UCSA, and install it into the new UCSA.
7. Reinstall the new UCSA by reversing steps 1 through 5.
8. If using new flash memory, configure the new controller’s TCP/IP address for use as a Mark VIe controller. For instructions, refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703), the section *Configure and Transfer IP Address to UCCA / UCCC / UCSA Controller.*
9. From the ToolboxST application, verify the status of the controller. It should be in the controlling state with no warnings or errors and online.
10. From the ToolboxST application, if the controller does not go online or the controller is not in the controlling state, download to the controller using the Download Wizard.

1.4 UCPA Controller with Integral I/O

The UCPA is a Mark* VIe controller platform that runs application code (control logic). The controller has both integral I/O capabilities and can communicate with external I/O packs through a Simplex IONet. The UCPA controller is commercial in design and not intended for use at any time in a residential environment. The UCPA controller is panel-mounted and includes the following features:

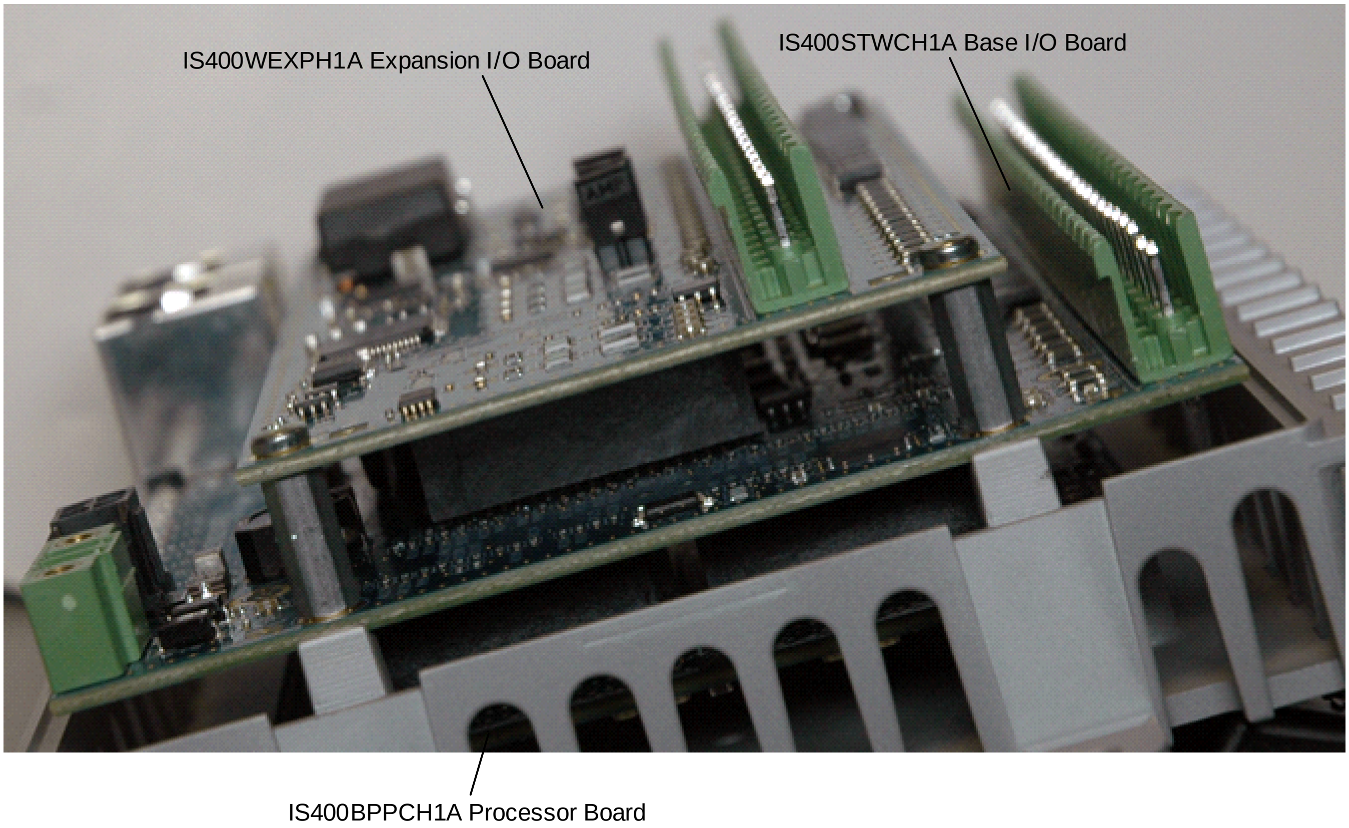
- Controller and I/O in a single module
  - Smaller panel footprint with integral I/O
  - IONet port for simplex I/O module expansion
- Single 12 V dc power supply, runs at 4 W (low power)
- Can operate in -40 to 70°C ambient temperate range
- No battery or fan
- Cost-effective platform for simplex control and I/O
- Uses ControlST* V05.04 or later with the same ToolboxST* configuration tools across the Mark Controls platform



1.4.1 UCPA Controller Versions

The Mark VIe UCPA controller contains the following components:

- IS400BPPCH2A processor board
- IS400STWCH1A base I/O board
- IS400WEXPH1A expansion I/O board (included with UCPAH2A)


IS400WEXPH1A Expansion I/O Board
IS400STWCH1A Base I/O Board
IS400BPPCH1A Processor Board

The IS420UCPAH1A includes the IS400STWCH1A (base I/O board) and the BPPCH2A processor board. It provides the following inputs and outputs:

- Two Hall Effect *Pulse Inputs*
- Two *Analog Inputs (AI)*
- Four *Digital Inputs or Outputs with feedback (DIO)*

The IS420UCPAH2A also includes the IS400WEXPH1A expansion I/O board. The WEXP provides the following additional I/O:

- Six AIs (for a total of 8)
- Two Analog Outputs
- Four DIOs (for a total of 8)

Note Some I/O points are configurable on a per point basis. Refer to the section, *Configuration* for more information.

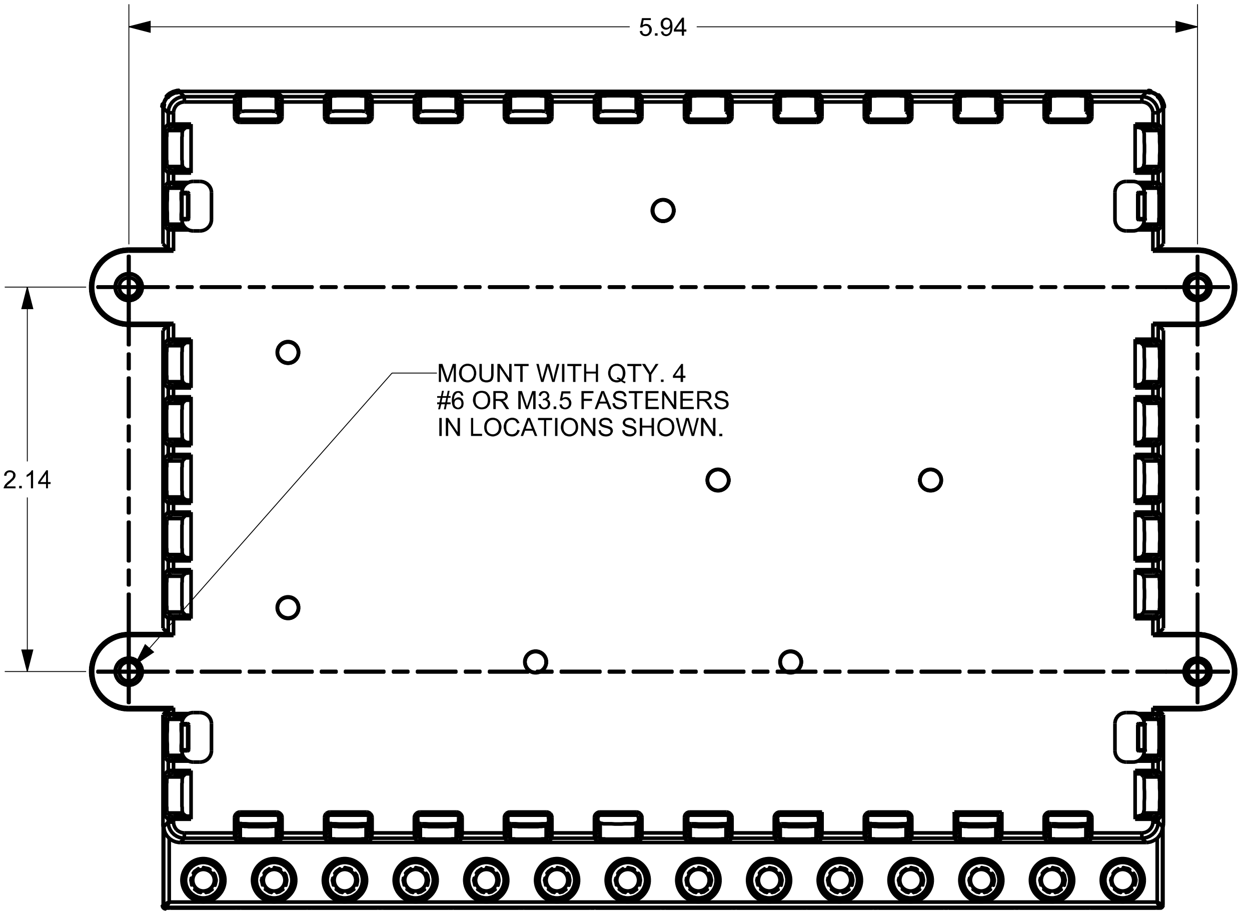
1.4.2 UCPA Specifications

Item	**UCPA Specfication**
Processor	Freescale 3308 processor, 332 MHz, (BPPC-based)
Memory	64 MB RAM 256 MB onboard flash 32 KB NOVRAM
Temperature/Humidity rating	-40 to +70°C (-40 to 158 °F), 5 to 95% relative humidity non-condensing
Ethernet ports	2 Ethernet ports, 10/100 Mbps, ENET1 for UDH, ENET2 for IONet to (maximum 6) distributed I/O modules
Ethernet protocols supported	Modbus TCP slave, NTP, and other GE proprietary protocols
Shared IONet	Not supported
10 ms frame period	Only supported if not using any distributed I/O packs over IONet
COM serial port	Used to set the network IP address or for maintenance by qualified GE engineer
Controller and I/O module Redundancy	Simplex
Configuration software	ToolboxST application
Internal operating system	QNX
Operating voltage	9 V to 16 V dc, nominal 12 V dc
Power consumption	4 W
Dimensions	162 mm X 115 mm X 72 mm
Mounting	Base-mounted
Terminal blocks	Wire sizes: 22 to 12 AWG Screw torque: 4.5 in-lb Temperature rating for copper wire: 80°C
2-pin Euro style power plug *Included with the UCPA part kit*	Wire sizes: 22 to 14 AWG Screw torque: 2.2 in-lb Temperature rating for copper wire: 80°C Wiring to power input terminals shall be limited to 30 meters in length
Expansion I/O pack capability	A maximum 6 simplex Mark VIe I/O packs over IONet with a minimum frame period of 20 milliseconds can connect to one UCPA. For a list of available simplex I/O modules, refer to *GEH-6721_Vol_I, Mark VIe and Mark VIeS Control System Guide,* the section *I/O Types*.
Internal I/O Types	
Discrete inputs or outputs (DIO) *Each point can be either a discrete input or a discrete output with feedback*	12 V dc, 4 DIOs on STWC and 4 additional DIOs with WEXP 2.2 V min for input high, 0.6 V max for input low, 16 V dc max input Accumulates counts, frequency up to 500 Hz Up to 500 mA sink on digital outputs for resistive and lamp loads. Up to 100 mA sink for inductive loads. Refer to the section, *Discrete Output Derating*

Item	**UCPA Specfication**
Analog Inputs	Two analog inputs on STWC Gains used in scaling: 1, 64, 128 Voltage In: Refer to the section, *Analog Input Modes*. Current (option channel 2): 4 to 20 mA Accuracy: 0.1% of full range
	Six analog inputs on WEXP Voltage In: 0 V to 5 V, fixed gain 1 (option channels 6, 7, and 8) Current: 4 to 20 mA (all channels 3–8) Accuracy : 0.1% of full range
Analog outputs	Two analog outputs on WEXP
	Voltage : 0 to 10 V
	Current : 0 to 20 mA
	Accuracy: 0.3% of full range
Pulse Inputs	Two Hall Effect *Pulse Inputs* on STWC
	20 mA sink current required, 5 V dc source provided (for Hall Effect sensor)
	Accumulates counts and measures time between pulses, frequency up to 5 kHz
Sequence of Events (SOEs)	Not available with internal I/O Supported with distributed I/O packs

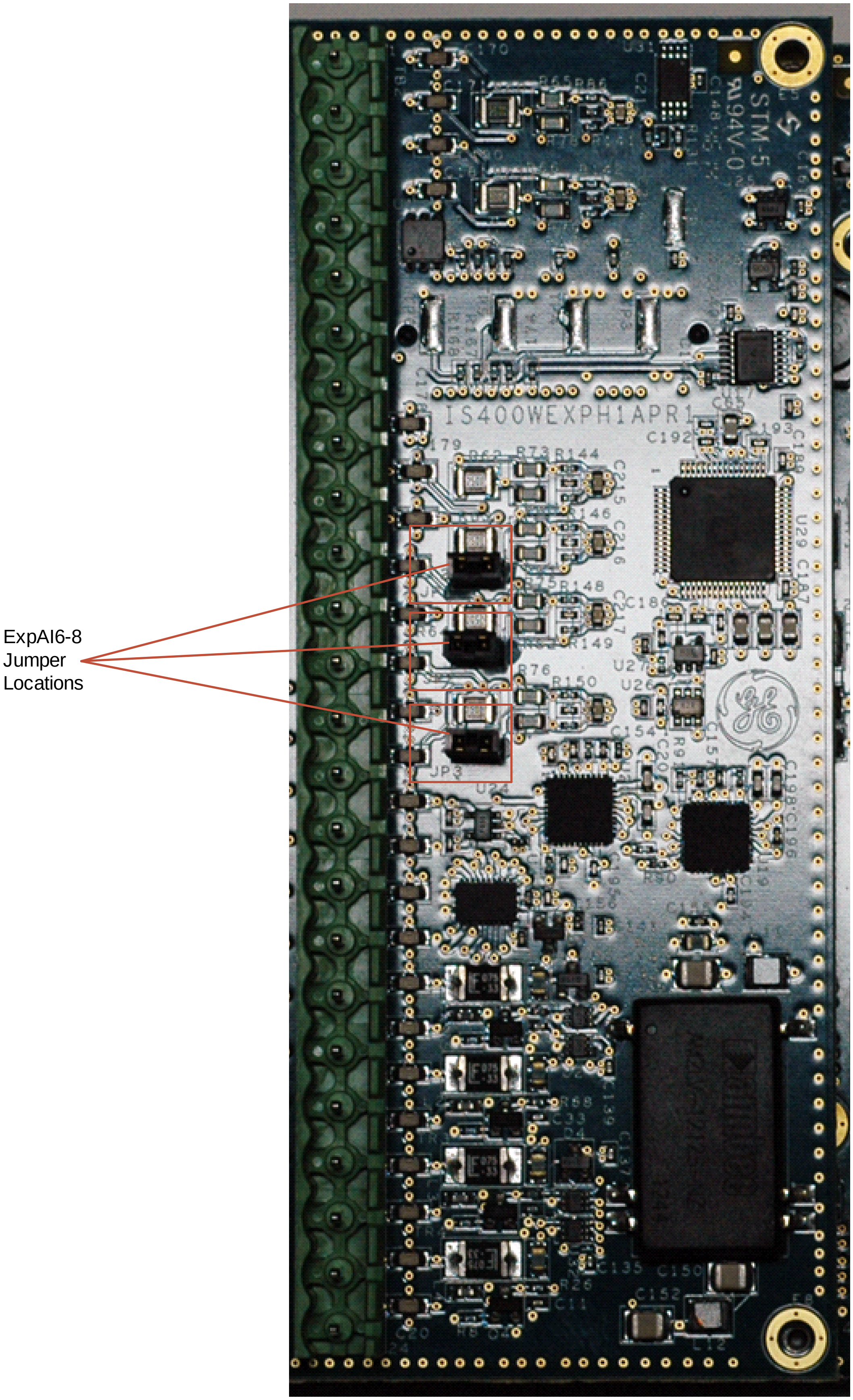
1.4.3 UCPA Installation

The controller is contained in a single module that mounts directly to the panel sheet metal. It is base-mounted and has integrated shield ties. Use #6_32 screws for mounting. The bottom part of the module is cast aluminum and the top portion is plastic. Provide approximately one inch of space around the UCPA within the panel for airflow and connection to shield ties.



UCPA Mounting, Dimensions are Inches

The WEXP has three jumpers (JP1, JP2, and JP3) that correspond to I/O points *ExpAI6* to ExpAI8 (analog inputs 6, 7, and 8) respectively. By default, these jumpers are installed to support the 4–20 mA input mode. Remove the jumpers to set these analog inputs to the 0–5 V input mode. For the removal of these jumpers, the removal of the UCPA cover is required (to expose the WEXP). The following figure displays the location of these jumpers.

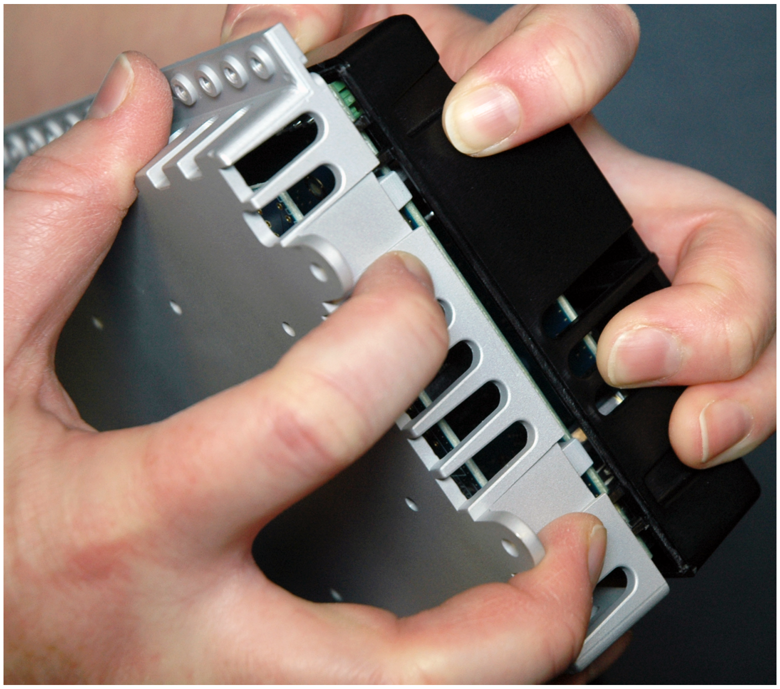

ExpAI6-8
Jumper
Locations

1.4.3.1 Remove UCPA Cover

The UCPAH2A requires partial disassembly to remove the WEXP jumpers. This sets the expansion analog inputs 6–8 to 0–5 V mode (default with jumpers is 4–20 mA mode).

➢ **To remove the UCPA cover**

1. Use a small flat-head screwdriver to unscrew the retaining screws on the power connector and remove it.
2. Remove the field wiring portion of both terminal blocks.
3. Locate the two indented sections of the cover (as shown in the following photo) and press firmly inward while pulling the cover away from the base.



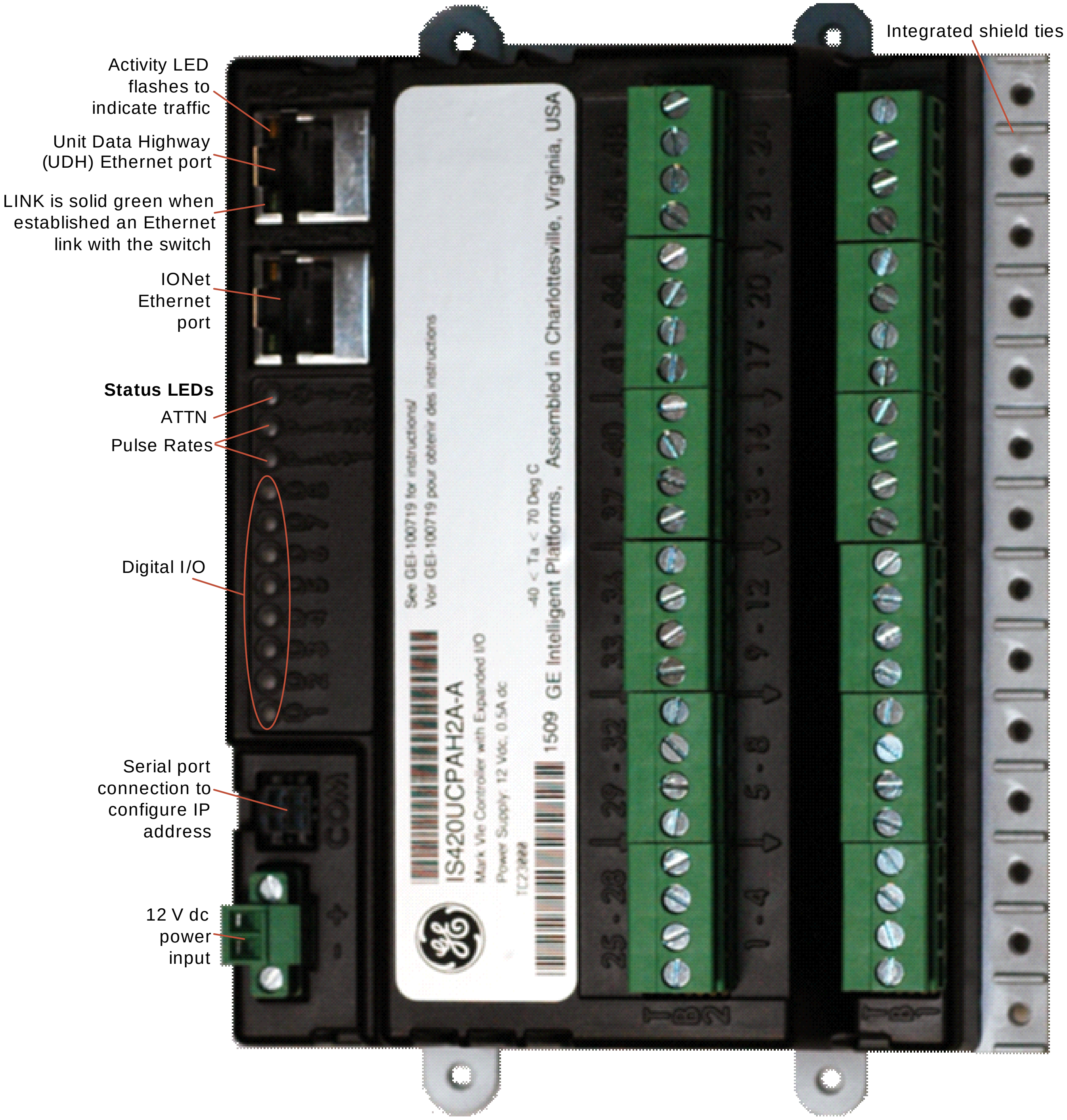
1.4.3.2 Wiring and Cabling

Analog inputs, analog outputs, pulse rate inputs, and any associated field power should use shielded signal cables with shield wires terminated on the provided chassis terminals. Discrete I/O may use non-shielded wiring. Ethernet cables should also be the shielded type. Shielded cables provide additional surge suppression for signals exposed to transients. For field wiring, refer to the terminal block pin definition tables for the STWC and WEXP.

The UCPA runs on a nominal 12 V dc power supply (9 to 16 V dc). The correct power connector is included with the UCPA controller part kit (it is not the one used with the UCSB). The 12 V dc power input is intended to be powered from a supply with Class II protection level. Wiring to the controller power input terminals shall be no more than 30 meters in length.

Caution

More than 16 V dc to the UCPA can cause damage to the components.


Activity LED flashes to indicate traffic
Unit Data Highway (UDH) Ethernet port
LINK is solid green when established an Ethernet link with the switch
IONet Ethernet port
Status LEDs
ATTN
Pulse Rates
Digital I/O
Serial port connection to configure IP address
12 V dc power input
Integrated shield ties
IS420UCPAH2A-A
COM
TB2
TB1

UCPA Ports and LEDs

1.4.4 UCPA Performance and Limitations

The UCPA is designed for simplex unit controls with integral I/O capability, a smaller footprint, and can operate in -40 to 70° C ambient temperature range. BPPC processor speed and amount of RAM are the limiting factors. UCPA has approximately 25% the memory of UCSB. Be aware, however, that the internal UCPA processor and memory do have the following limitations as compared to the UCSB controller:

- UCPA performance as relative to the UCSBH4A (1066MHz Intel® processor) is approximately 15% capability.
- UCPA performance as relative to the UCSBH1A (600 MHz Intel processor) is approximately 25% capability.
- UCPA cannot be part of a Shared IONet system.
- UCPA does not support OPC UA direct from the controller.
- UCPA can only support a maximum of six simplex distributed I/O packs over IONet with a minimum frame period of 20 ms.
- UCPA does not have a real-time clock, which is needed to fully support the SecurityST server.
- FOUNDATION fieldbus is not supported with UCPA.

1.4.5 BPPC Processor in the UCPA

The UCPA uses the IS400BPPCH2A processor version, which passes all connections through the internal STWC I/O board. It runs at nominal 12 V dc (9 to 16), and accepts a serial interface.

The BPPC processor board provides the following features:

- High-speed processor with RAM and flash memory
- Two fully independent 10/100 Ethernet ports with connectors
- Hardware watchdog timer and reset circuit
- Internal temperature sensor
- Status-indication LEDs
- Electronic ID and the ability to read IDs on other boards
- Local CPU power supplies

At startup, the processor reads board ID information to ensure the correct matching of UCPA internal circuit boards. With a good match, the processor attempts to establish Ethernet communications, starting with request of a network address. The address request uses the industry standard dynamic host configuration protocol (DHCP).

After Ethernet initialization, the processor programs the on-board logic, runs the application, and enables the acquisition board to begin operation. The processor application code contains all the logic necessary to allow the UCPA controller and I/O module to operate with or without IONet to external I/O packs. The Ethernet ports on the processor auto-negotiate between 10 and 100 Mbps speed, and between half-duplex and full-duplex operation.

1.4.5.1 Controller Application Logic

The controller runs software specific to its application. The application code (control logic) is made up of function blocks configured with the ToolboxST application. From the ToolboxST Block Diagram Editor, right-click the block diagram and select Block Help for more information. Minor modifications to the control software may be made online. Variables are connected to block diagrams. The logic is then downloaded to the controller from the ToolboxST application.

1.4.5.2 IONet Communications

The UCPA controller can communicate over IONet to simplex distributed I/O packs (maximum of six) through an unmanaged ESWA or ESWB switch. Refer to the figure, *UCPA Control and Communications*. IEEE 1588 protocol is used through the IONet to synchronize the clock of the distributed I/O packs and the UCPA to within ±100 microseconds. External data is also transferred to the controller over the IONet, including process inputs from and outputs to the I/O modules. Sequence of Events (SOEs) are supported with distributed I/O packs, but not with the UCPA integral I/O.

1.4.6 UCPA Diagnostics

The I/O functions integral to the UCPA do not provide any diagnostics that are available to the user as variables or from the ToolboxST application as alarms. There are diagnostics common to Mark VIe controllers, which are supported, with possible causes and solutions that are viewable from the ToolboxST application. In addition, diagnostic messages from distributed I/O packs are also supported by the UCPA controller. Refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703) for more information on how to view diagnostics.

1.4.6.1 UCPA Status LEDs

The internal UCPA processor (BPPC) provides the following diagnostics as status LEDs. Refer to the figure, UCPA Ports and LEDs. There are two LEDs (Yellow/Green) for each Ethernet connector (ENET1 and ENET2), which are embedded in the RJ-45 connectors. The green LED indicates an Ethernet connection has been established. The yellow LED indicates packet traffic.

UCPA LEDs

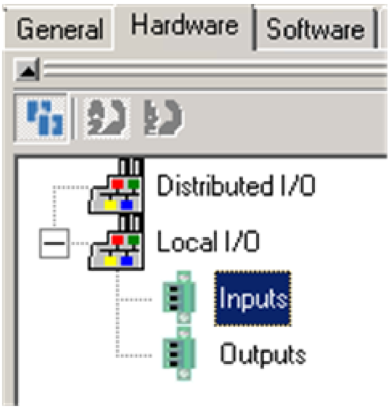
Label	Color	Description
DIO1 to DIO8	Yellow	ON indicates discrete input/output is active low
PULSE1 PULSE2		ON indicates pulse input is active low
ATTN	Red and Green	Bi-color LED, red for Attention, green for Sync — displays processor status

ATTN LED Flash Codes

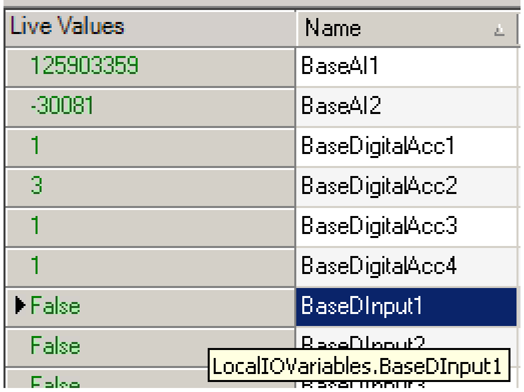
LED	Flashing Pattern	Description
Red ATTN	Solid	Booting - prior to reading board ID
	4 Hz 50%	Diagnostic alarm active
	2 Hz 50%	Awaiting an IP address
	1 Hz 50%	No firmware to load (Program mode)
	0.5 Hz 50%	Application code not loaded
	LED out	Initializing, no problems detected
Green ATTN	Solid	BIOS (at power on), but if it remains in this state, the component is not functioning properly and should be replaced
	1 or 2 Hz at 50%	Component has completed power up, and is progressing through the state machine, no problems detected
	Two 4 Hz flashes every 4 sec	Online and controlling

1.4.7 UCPA Configuration

Configure the integral UCPA I/O points from the ToolboxST Component Editor **Hardware** tab.



The inputs and outputs are global variables that can be modified by double-clicking **Live Values**. These variables can be used directly in the controller application logic without connection to a different local variable.



Live Values	Name
125903359	BaseAI1
-30081	BaseAI2
1	BaseDigitalAcc1
3	BaseDigitalAcc2
1	BaseDigitalAcc3
1	BaseDigitalAcc4
False	BaseDInput1
False	BaseDInput2

Note Refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703) for instructions for configuring Modbus.

1.4.7.1 Inputs

Name	Description	Type	Mode or Notes
BaseAI1	Base Analog Input 1 (screws 1–4)	DINT	± 39 mV, ± 78 mV, ± 5 V differential, 0-5 V single-ended
BaseAI2	Base Analog Input 2 (screws 5–10)	DINT	± 39 mV, ± 78 mV, ± 5 V differential, 0-5 V single-ended, 4-20 mA (with a jumper placed between screws 9 and 10)
BaseDigitalAcc1	Base Digital Accumulator 1	UDINT	Increments on the falling edge of the digital input or output (counts up by 1)
BaseDigitalAcc2	Base Digital Accumulator 2	UDINT	
BaseDigitalAcc3	Base Digital Accumulator 3	UDINT	
BaseDigitalAcc4	Base Digital Accumulator 4	UDINT	
BaseDInput1	Base Discrete Input 1 (screws 11–12)	BOOL	‡ Low level equals True
BaseDInput2	Base Discrete Input 2 (screws 13–14)	BOOL	
BaseDInput3	Base Discrete Input 3 (screws 15–16)	BOOL	
BaseDInput4	Base Discrete Input 4 (screws 17–18)	BOOL	
BaseDOReadBack1	Base Discrete Output Read Back 1 (screws 11–12)	BOOL	‡ Low level equals True Active Low
BaseDOReadBack2	Base Discrete Output Read Back 2 (screws 13–14)	BOOL	
BaseDOReadBack3	Base Discrete Output Read Back 3 (screws 15–16)	BOOL	
BaseDOReadBack4	Base Discrete Output Read Back 4 (screws 17–18)	BOOL	
‡ Refer to the section, *Discrete Input and Output, Non-isolated* for more information on the hardware functions and options for field wiring.			
BasePulse1	Base Pulse 1 (screws 19–21)	BOOL	Low level equals True
BasePulse2	Base Pulse 2 (screws 22–24)	BOOL	Low level equals True
BasePulseAcc1	Base Pulse Accumulator 1	UDINT	Increments on the falling edge of the pulse inputs (counts up by 1)
BasePulseAcc2	Base Pulse Accumulator 2	UDINT	
DeltaTimePulse1	Base Delta Time for Pulse Input 1	UDINT	Time between falling edges in microseconds
DeltaTimePulse2	Base Delta Time for Pulse Input 2	UDINT	
ExpAI3	Expansion Analog Input 3 (screws 25–26)	DINT	4-20 mA
ExpAI4	Expansion Analog Input 4 (screws 27–28)	DINT	4-20 mA
ExpAI5	Expansion Analog Input 5 (screws 29–30)	DINT	4-20 mA
ExpAI6	Expansion Analog Input 6 (screws 31–32)	DINT	0-5 V without *jumper* 4-20 mA with jumper
ExpAI7	Expansion Analog Input 7 (screws 33–34)	DINT	
ExpAI8	Expansion Analog Input 8 (screws 35–36)	DINT	

Name	Description	Type	Mode or Notes
ExpDigitalAcc5	Expansion Digital Accumulator 5	UDINT	Increments on the falling edge of the digital input or output (counts up by 1)
ExpDigitalAcc6	Expansion Digital Accumulator 6	UDINT	
ExpDigitalAcc7	Expansion Digital Accumulator 7	UDINT	
ExpDigitalAcc8	Expansion Digital Accumulator 8	UDINT	
ExpDInput5	Expansion Discrete Input 5 (screws 41–42)	BOOL	‡ Low level equals True
ExpDInput6	Expansion Discrete Input 6 (screws 43–44)	BOOL	
ExpDInput7	Expansion Discrete Input 7 (screws 45–46)	BOOL	
ExpDInput8	Expansion Discrete Input 8 (screws 47–48)	BOOL	
ExpDOReadBack5	Expansion Discrete Output Read Back 5 (screws 41–42)	BOOL	‡ Low level equals True Active Low
ExpDOReadBack6	Expansion Discrete Output Read Back 6 (screws 43–44)	BOOL	
ExpDOReadBack7	Expansion Discrete Output Read Back 7 (screws 45–46)	BOOL	
ExpDOReadBack8	Expansion Discrete Output Read Back 8 (screws 47–48)	BOOL	
ExpIoEnabled	Expansion I/O Enabled	BOOL	WEXP installed if True
LatchedPulseAcc1AtPulse2	Latches Pulse Accumulator 1 (rpm pulse count) as captured on the falling edge of Pulse Input 2 (crank), not synced to any interrupt	UDINT	Does not function on LatchMode event
LatchedBaseAI1	Latched Load Value	DINT	† A cohesive sample set based on *LatchMode Event*
LatchedBaseAI2	Latched Position Value	DINT	
LatchedDeltaTimePulse1	Latched Delta Time for Pulse 1, in microseconds	UDINT	
LatchedBasePulseAcc1	Latched Pulse Accumulator 1	UDINT	
LatchedSampleCount	Latched Sample Count	UDINT	

‡ Refer to the section, *Discrete Input and Output, Non-isolated* for more information on the hardware functions and options for field wiring.

1.4.7.2 LatchedMode Event

Five *local input variables* are sampled at regular intervals and latched to a cohesive set of inputs. These values are sampled together as close as possible for application-specific use. The fastest sample rate for these signals is 2048 microseconds.

The two modes used to configure the data latching are as follows:

- By writing the value **0** (default value) to the *LatchMode* output variable, the UCPA latches the variable set on every falling edge of BasePulse1.
- By writing the value **1** to the **LatchMode** variable and setting a value into the *LatchTime* variable, the UCPA latches the variable set when the latch timer expires. Set the LatchTime variable to a value greater than or equal to the minimum of 2048 microseconds, and then set LatchMode to a value of 1 to engage the timer to trigger the data latching.

Note With either LatchMode, this function generates an interrupt and subsequent move of the values into signal space.

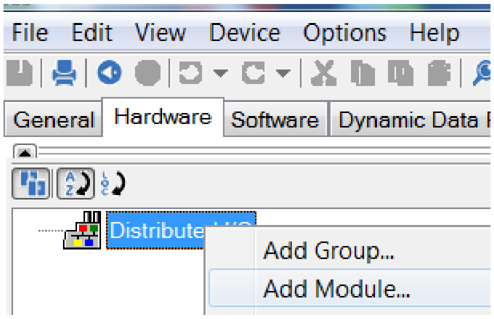
1.4.7.3 Outputs

Name	Description	Type	Mode
‡ BaseDOutput1	Discrete Output 1, True drives output Active Low (screws 11–12)	BOOL	
‡ BaseDOutput2	Discrete Output 2, True drives output Active Low (screws 13–14)	BOOL	
‡ BaseDOutput3	Discrete Output 3, True drives output Active Low (screws 15–16)	BOOL	
‡ BaseDOutput4	Discrete Output 4, True drives output Active Low (screws 17–18)	BOOL	
ExpAO1	Expansion Analog Output 1 (screws 37–38)	UDINT	0–10 V 0–20 mA
ExpAO2	Expansion Analog Output 2 (screws 39–40)	UDINT	0–10 V 0–20 mA
‡ ExpDOutput5	Expansion Discrete Output 5, True drives output Active Low (screws 41–42)	BOOL	
‡ ExpDOutput6	Expansion Discrete Output 6, True drives output Active Low (screws 43–44)	BOOL	
‡ ExpDOutput7	Expansion Discrete Output 7, True drives output Active Low (screws 45–46)	BOOL	
‡ ExpDOutput8	Expansion Discrete Output 8, True drives output Active Low (screws 47–48)	BOOL	
† LatchMode	Latch Mode Select, 0 = edge-triggered, 1 = timer-triggered	UDINT	
† LatchTime	32-Bit countdown timer in microseconds, used for latching Analog Input 1 and 2 as well as Pulse Accumulator 1 Used when LatchMode = 1	UDINT	
† Refer to the section *LatchedMode Event* for more information.			

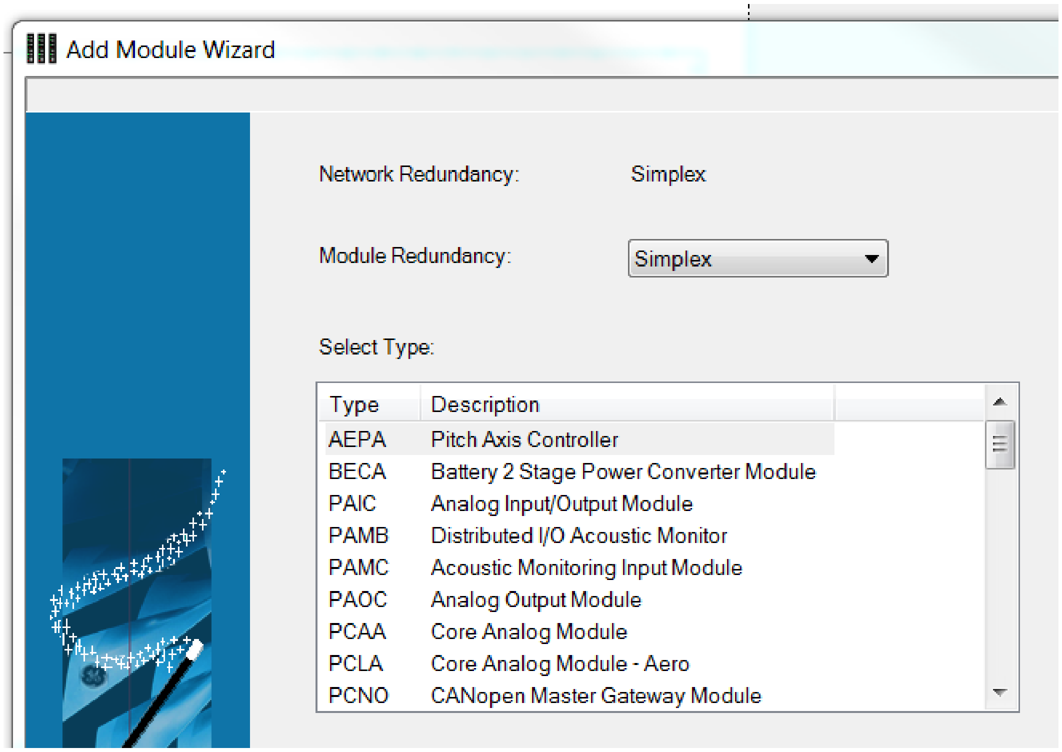
Note ‡ Refer to the section, *Discrete Input and Output, Non-isolated* for more information on the hardware functions and field wiring.

1.4.7.4 Distributed I/O Types

Connecting to distributed I/O modules is accomplished from the Component Editor Hardware tab, using the typical procedure for adding a new simplex module. The figure, *UCPA Control and Communications*, displays an example of the UCPA connected to distributed I/O packs.



Module Redundancy must be **Simplex**.



Network Redundancy: Simplex

Module Redundancy: Simplex

Select Type:

Type	Description
AEPA	Pitch Axis Controller
BECA	Battery 2 Stage Power Converter Module
PAIC	Analog Input/Output Module
PAMB	Distributed I/O Acoustic Monitor
PAMC	Acoustic Monitoring Input Module
PAOC	Analog Output Module
PCAA	Core Analog Module
PCLA	Core Analog Module - Aero
PCNO	CANopen Master Gateway Module

1.4.8 STWC I/O Board

The STWC is the base internal I/O board for the UCPAH1A and UCPAH2A controllers. It provides the following inputs and outputs:

- Two Hall Effect *Pulse Inputs*
- Two Analog Inputs (AI)
- Four Digital Inputs or Outputs with feedback (DIO)

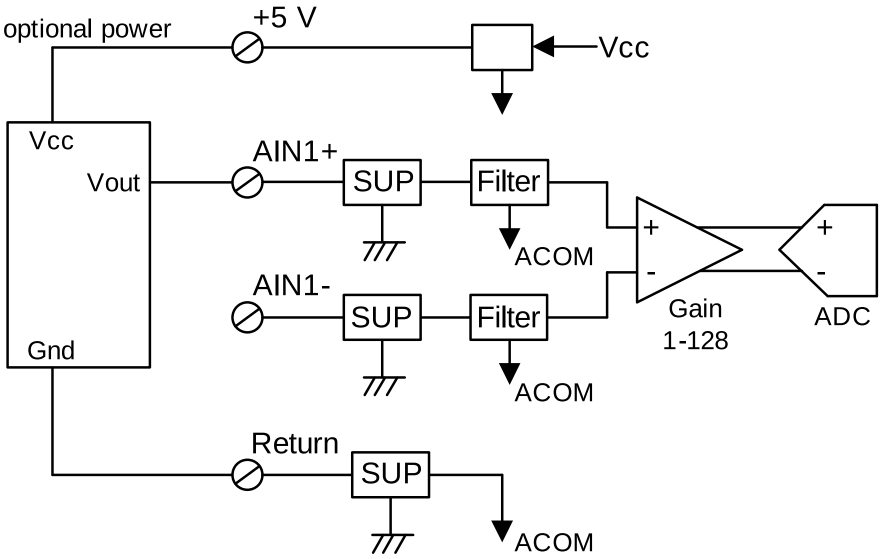
TB1 Terminal Block Pin Definitions

Screw #	Screw Name	Global Variable	Description
1	AIN1_5V	BaseAI1	Analog Input 1, 5 V field power, 15 mA max
2	AIN1_P		Analog Input 1 Positive
3	AIN1_N		Analog Input 1 Negative
4	AIN1_RET		Analog Input 1 Return
5	AIN2_5V	BaseAI2	Analog Input 2, 5 V field power, 15 mA max
6	AIN2_P		Analog Input 2 Positive
7	AIN2_N		Analog Input 2 Negative
8	AIN2_RET		Analog Input 2 Return
9	AIN2_JPR		Analog input 2 has a 4-20 mA option. Apply a terminal jumper between pins 9 and 10. This applies the 250 ohm burden across the AIN2 differential input.
10	AIN2_JPR		
11	DIO1	BaseDInput1 or BaseDOReadBack1 BaseDOutput1	Digital Input or Output 1
12	DIO1_RET		DIO Return 1
13	DIO2	BaseDInput2 or BaseDOReadBack2 BaseDOutput2	Digital Input or Output 2
14	DIO2_RET		DIO Return 2
15	DIO3	BaseDInput3 or BaseDOReadBack3 BaseDOutput3	Digital Input or Output 3
16	DIO3_RET		DIO Return 3
17	DIO4	BaseDInput4 or BaseDOReadBack4 BaseDOutput4	Digital Input or Output 4
18	DIO4_RET		DIO Return 4
19	PULSE_P5		Pulse Rate 1, 5 V Power Output for Hall Effect Sensor, 10 mA
20	PULSE1	BasePulse1	Pulse Rate 1 Input Signal
21	PULSE_COM		Pulse Rate 1 Ground
22	PULSE_P5		Pulse Rate 2, 5 V Power Output for Hall Effect Sensor, 10 mA
23	PULSE2	BasePulse2	Pulse Rate 2 Input Signal
24	PULSE_COM		Pulse Rate 2 Ground

1.4.9 STWC Analog Differential Voltage Inputs, Group-Isolated

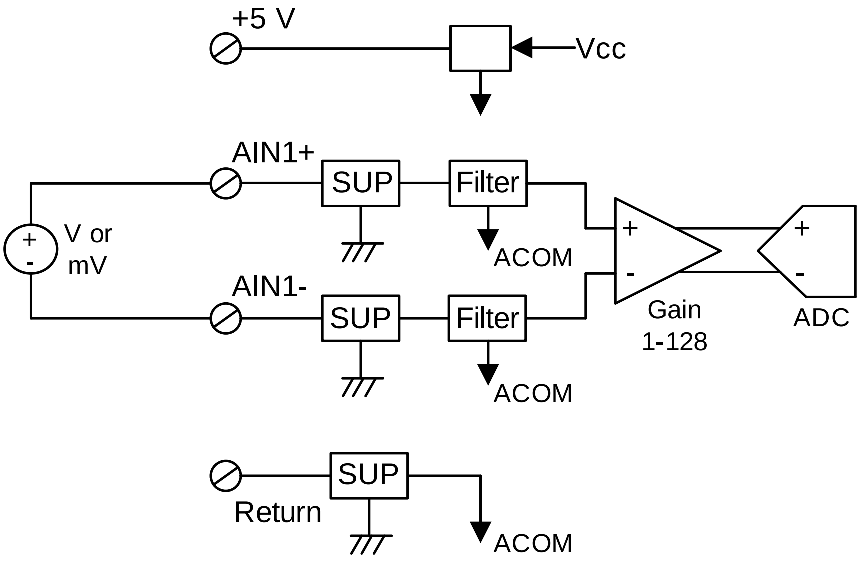
These analog inputs are group isolated. Power is supplied by 12 V dc-dc isolated power supply. The digital signal interface is isolated with a capacitive coupled isolator. The primary application is differential voltage inputs for a LOAD bridge (+/-10mV) and POSITION Inclinometer (0-5V).

The analog inputs are single-ended inputs when using terminals 2 and 4 for analog input 1 or terminals 6 and 8 for analog input 2, and setting the appropriate ToolboxST configuration for *BaseAI1* or BaseAI2. This is the case for most 5 V field devices.



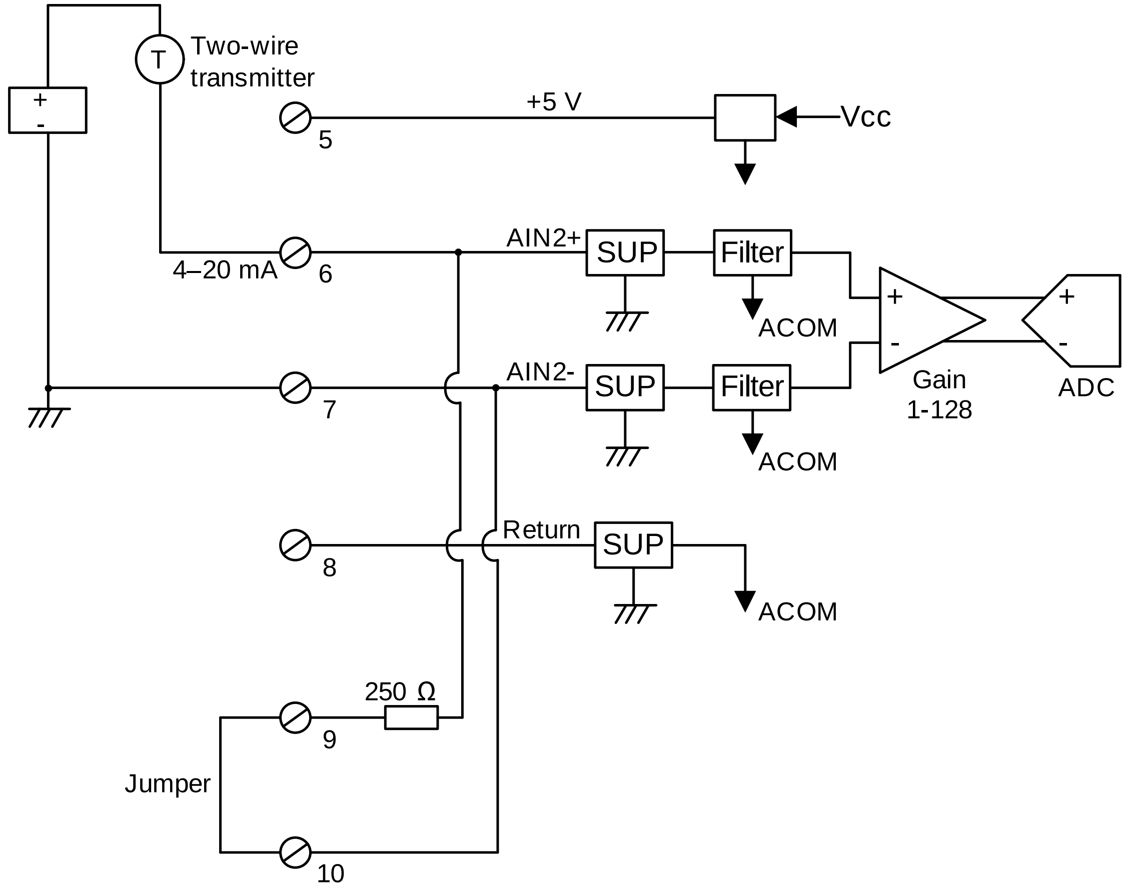
0–5 V Single-ended with Analog Input 1 or 2

From the ToolboxST configuration, *± 5 V differential* is also the selection for 0 to 5 V differential. The analog inputs are differential inputs when using terminals 2 and 3 for analog input 1 or terminals 6 and 7 for analog input 2, and setting the appropriate ToolboxST configuration for *BaseAI1* or BaseAI2.



0–5 V Differential with Analog Input 1 or 2

Analog input 2 can also be a 4-20 mA input. When configured for 4-20 mA, a differential connection should be made to terminals 6 and 7, install a wire or jumper between TB1 pins 9 and 10 (which inserts the 250 Ohm 0.1% load resistor), and select the AI_Mode from the ToolboxST application.



Analog Input 2 4–20 mA Connection Example

1.4.9.1 Analog Input Modes

The ADS1220 A/D converter supports differential and single-ended inputs, with a gain from 1 to 128. The programmable gain amplifier (PGA) may be bypassed for rail-to-rail 5 Volt signals.

AI	Signal Level	Input Connections	Common Mode Voltage	Signal Type Mux Mode	ADC Gain	PGA Mode
1, 2	0 to +5 V	+in, ACOM	0 V	Single-ended	1	Bypassed
1, 2	0 to +5 V	+in, -in	0 V	Differential	1	Bypassed
1, 2	±5 V	+in, -in	2.5 V	Differential	1	Bypassed
1, 2	±39mV	+in, -in	2.5 V	Differential	128	Enabled
1, 2	±78mV	+in, -in	2.5 V	Differential	64	Enabled
2	4 to 20 mA	+in, -in	0 to 5 V	Differential	1	Bypassed

1.4.9.2 Scaling of Analog Inputs 1–2

Analog Input	Gains	Voltage	Current
1	1, 64, or 128 depending on the Input Mode (5V, 78mV, or 39 mV)	$\text{Vin} = \frac{5\ (\text{BaseAI1})}{2^{31}(\text{GAIN})}$	n/a
2	1, 64, or 128 depending on the Input Mode (5V, 78mV, or 39 mV)	$\text{Vin} = \frac{5\ (\text{BaseAI2})}{2^{31}(\text{GAIN})}$	$\underset{(mA)}{\text{Ain}} = \frac{5\ (\text{BaseAI2})}{2^{31}(250)} \text{ X } 1000$

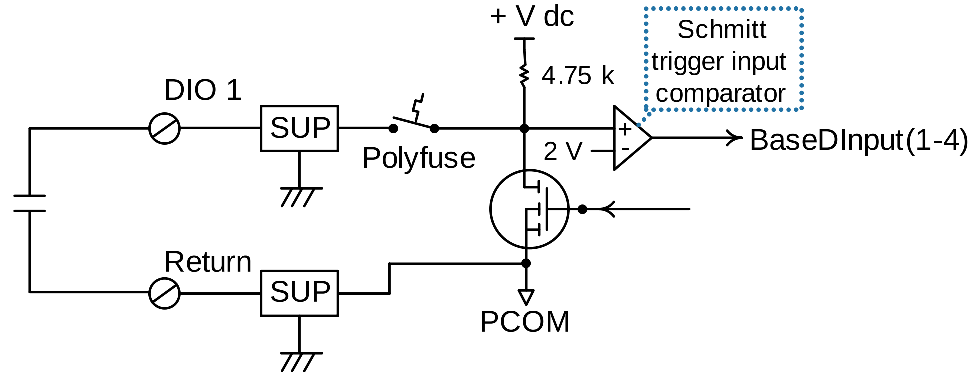
Analog Input	Volts to Counts (+/-39mv)	Volts to Counts (+/-78mv)	Volts to Counts (+/-5v)	Milliamps to Counts (4-20ma)
1	0v = 0	0v = 0	5v = 2,147,483,647	n/a
	25mv = 1374389535	25mv = 687194767	2.5v = 1,073,741,824	
		50mv = 1374389535	0v = 0	
			-2.5v = -1,073,741,824	
			-5v = -2,147,483,648	
2	0v = 0	0v = 0	5v = 2,147,483,647	20ma = 2,147,483,647
	25mv = 1374389535	25mv = 687194767	2.5v = 1,073,741,824	16ma = 1,717,986,918
		50mv = 1374389535	0v = 0	12ma = 1,288,490,189
			-2.5v = -1,073,741,824	8ma = 858,993,459
			-5v = -2,147,483,648	4ma = 429,496,730
				0ma = 0

1.4.10 STWC Discrete Input or Output with feedback, Non-isolated

Four non-isolated digital I/O points are individually configurable in the ToolboxST application for either 12 V input or open drain output with feedback. When an I/O point is configured as an output, the input circuitry functions as a feedback signal. The signal is pulled-up with 4.75k Ohms to the 12 V supply.

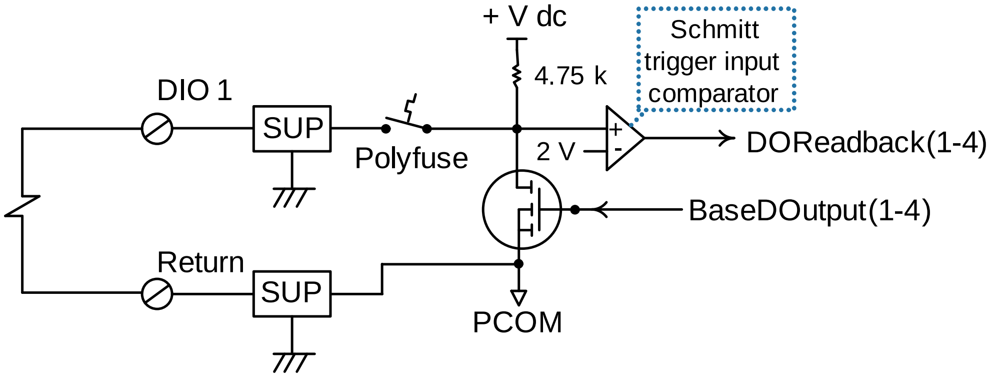
The discrete input or output (DIO) terminals are compatible with 12 V I/O (9 V to 16 V). The terminals are bidirectional. When configured by ToolboxST as an output, a Boolean state of True drives the open-drain terminal low. When the Boolean state is False, the terminal is pulled high by the resistance. Output loads such as relay coils may be driven by switching the low side and connecting the high side to the 12 V dc external power supply. Inductive loads should have fly-back suppression installed on the relay. Input signals must be less than 0.6 V to indicate that the Boolean state is True, and should be greater than 2.2 V to indicate a Boolean state of False.

The input is RC filtered by 20k Ohm and 10nF for bandwidth of 800 Hz (allowable bandwidth is specified lower than this as 500 Hz). The input is sensed by a Schmitt trigger IC powered from 3.3 V supply with threshold of about 2 Volts.



Discrete In

This is an open drain style output. It uses an Si2308BDS MOSFET with 500 mA current sink capability for resistive or lamps load types and 100 mA for inductive load types. Wetting power is provided from external 12 V supply, which can be the same supply that powers the board 12 V input.

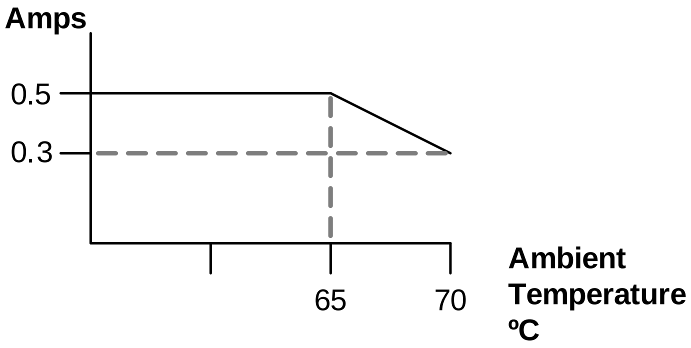


Discrete Out

1.4.10.1 Discrete Output Derating

Attention

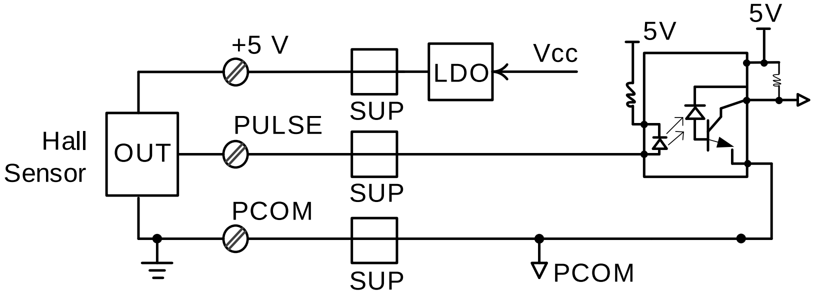
The discrete output sink current should be derated for elevated ambient temperatures using the following graph.



1.4.11 STWC Pulse Accumulator Inputs

The pulse inputs are 5 V open-collector inputs that source 20 mA when driven low by the sensor. The bandwidth is 5 kHz. The inputs are not galvanically isolated. The sensor ground is AC-coupled to chassis and ferrite-coupled to board ground. For low frequency signals (including up to the pulse rate input bandwidth), sensor ground is the same as board ground.

2 Pulse Rate (Hall Effect) Inputs



Designed for open-collector output devices

Nominal 20 mA input current

1.4.12 WEXP Expansion I/O Board

The WEXP expansion I/O board is part of the IS420UCPAH2A. There are three jumpers on the WEXP that are removed to allow for 0–5 V Analog Inputs on channels 6–8. These inputs are 4–20 mA with the JP1, JP2, or JP3 jumpers installed. The WEXP provides the following I/O types:

- 6 Analog Inputs
- 2 Analog Outputs
- 4 Discrete Inputs and Outputs

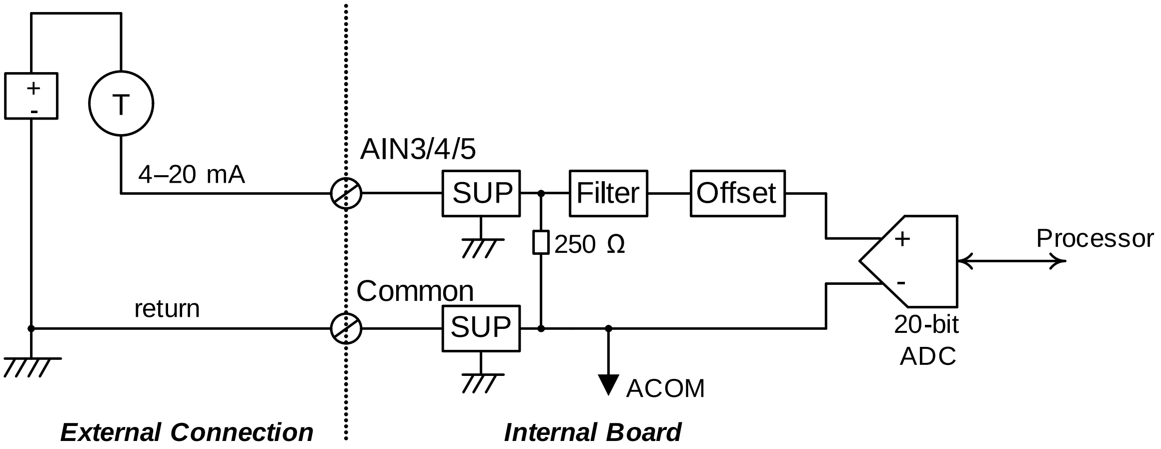
TB2 Terminal Block Pin Definitions

Screw #	Screw Name	Global Variable	Description
25	AIN3	ExpAI3	Expansion Analog Input 3, 4-20 mA
26	AIN3_RET		Expansion Analog Input 3 Return
27	AIN4	ExpAI4	Expansion Analog Input 4, 4-20 mA
28	AIN4_RET		Expansion Analog Input 4 Return
29	AIN5	ExpAI5	Expansion Analog Input 5, 4-20 mA
30	AIN5_RET		Expansion Analog Input 5 Return
31	AIN6	ExpAI6	Expansion Analog Input 6, 0-5 V without jumper 4-20 mA with jumper
32	AIN6_RET		Expansion Analog Input 6 Return
33	AIN7	ExpAI7	Expansion Analog Input 7, 0-5 V without jumper 4-20 mA with jumper
34	AIN7_RET		Expansion Analog Input 7 Return
35	AIN8	ExpAI8	Expansion Analog Input 8, 0-5 V without jumper 4-20 mA with jumper
36	AIN8_RET		Expansion Analog Input 8 Return
37	AOUT1	ExpAO1	Expansion Analog Output 1
38	AOUT1_RET		Expansion Analog Output 1 Return
39	AOUT2	ExpAO2	Expansion Analog Output 2
40	AOUT2_RET		Expansion Analog Output 2 Return
41	DIO5	ExpDInput5 or ExpDOReadBack5 ExpDOutput5	Expansion Discrete Input or Output 5
42	DIO5_RET		Expansion DIO Return 5
43	DIO6	ExpDInput6 or ExpDOReadBack6 ExpDOutput6	Expansion Discrete Input or Output 6
44	DIO6_RET		Expansion DIO Return 6
45	DIO7	ExpDInput7 or ExpDOReadBack7 ExpDOutput7	Expansion Discrete Input or Output 7
46	DIO7_RET		Expansion DIO Return 7
47	DIO8	ExpDInput8 or ExpDOReadBack8 ExpDOutput8	Expansion Discrete Input or Output 8
48	DIO8_RET		Expansion DIO Return 8

1.4.13 WEXP Analog Inputs, Single-Ended, Group-Isolated

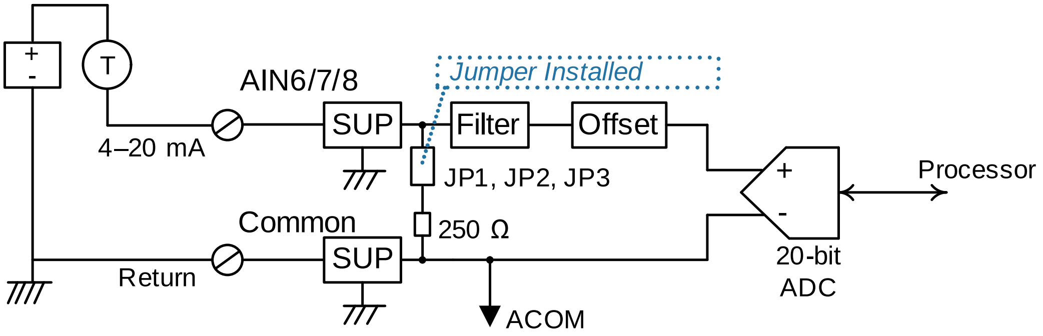
AIN 3 – 8 connections are made on TB2 pins in +/- pairs. Provide a signal and return path for single-ended analog inputs. These inputs are group isolated. Power is supplied by 12 V DC-DC ISO supply. AIN 3, 4, and 5 are 4–20 mA only.

Analog Inputs 3 through 5

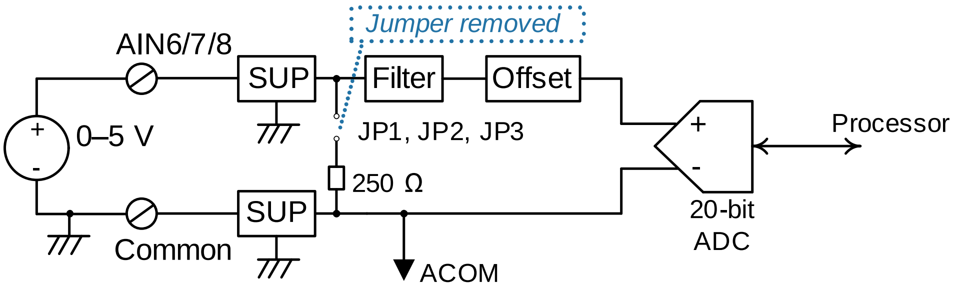


AIN 6, 7, and 8 are configurable by removing the *jumper* for 0–5 V input. The jumper may be left installed (factory default) for 4–20 mA input mode. No software configuration changes are necessary in either mode.

4–20 mA Option, Analog Inputs 6 through 8



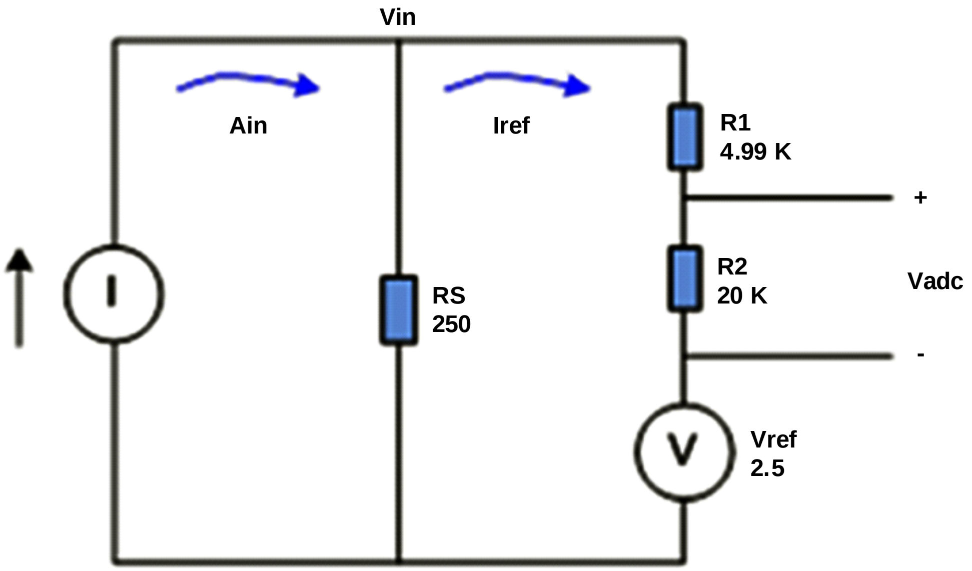
5 V Input Option for Analog Inputs 6 through 8



1.4.13.1 Scaling of Analog Inputs 3–8

Analog Input	Gains	Voltage	Current
3–5	1	n/a	$\text{Ain (mA)} = \frac{3.155 \left[\frac{\text{(ExpAI6)}}{2^{31}} \right] + 2.5}{250} \times 1000$
6–8	1	$\text{Vin} = \frac{3.12375 \text{ (ExpAI6)}}{2^{31}} + 2.5$	

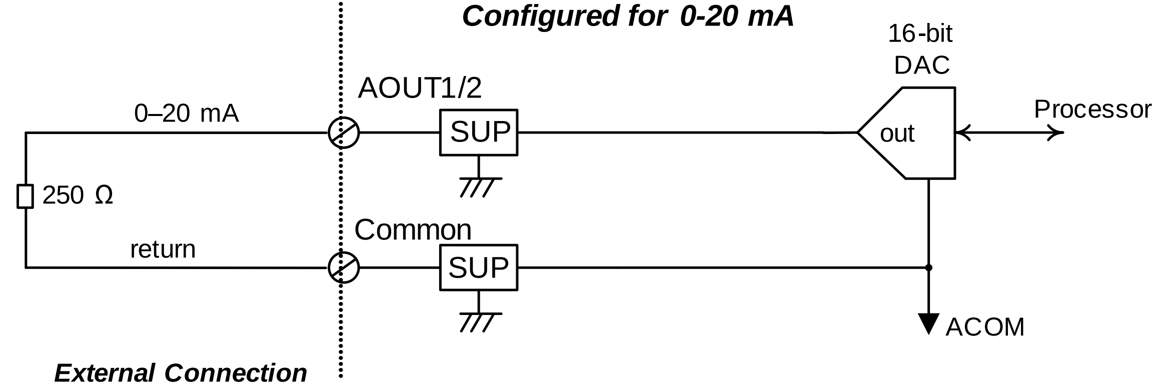
Analog Input	Volts to Counts (0-5v)	Milliamps to Counts (4-20ma)
3–5	n/a	20ma = 1,701,651,068
		16ma = 1,020,990,641
		12ma = 340,330,214
		8ma = -340,330,214
		4ma = -1,020,990,641
		0ma = -1,701,651,068
6–8	5v = 1,718,674,388	20ma = 1,701,651,068
	4v = 1,031,204,633	16ma = 1,020,990,641
	3v = 343,734,878	12ma = 340,330,214
	2v = -343,734,878	8ma = -340,330,214
	1v = -1,031,204,633	4ma = -1,020,990,641
	0v = -1,718,674,388	0ma = -1,701,651,068



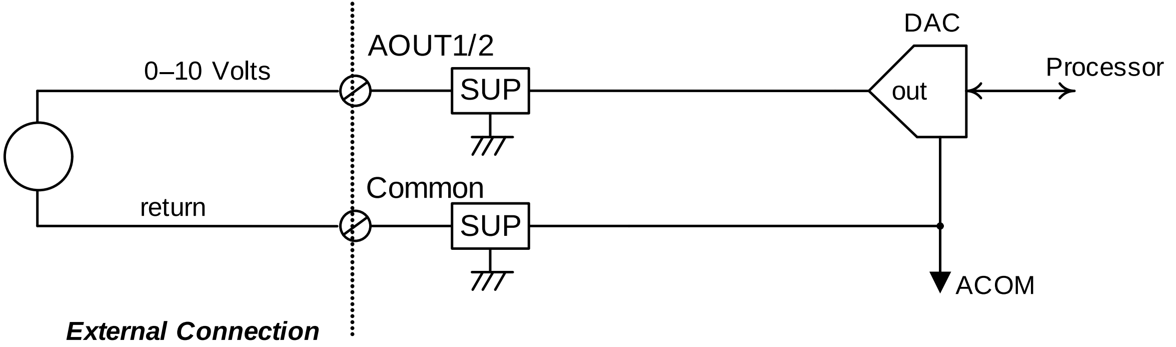
1.4.14 WEXP Analog Outputs

These outputs are referenced to module ACOM. Each analog output is configured for 0–10 V or 0–20 mA output in the ToolboxST application.

Analog Outputs 1 & 2
Configured for 0-20 mA



Analog Outputs 1 & 2
Configured for 0-10V



$$\text{ExpAO1} = \frac{\text{Iref (Amps)}}{0.020} \text{ X } 2^{32}$$

Current

$$\text{ExpAO1} = \frac{\text{Vref (Volts)}}{10} \text{ X } 2^{32}$$

Voltage

Counts

Analog Output	Counts to Volts (0-10v)	Counts to Milliamps (0-20ma)
1–2	4,294,967,295 = 10v	4,294,967,295 = 20ma
	3,435,973,837 = 8v	3,435,973,837 = 16ma
	2,576,980,378 = 6v	2,576,980,378 = 12ma
	1,717,986,918 = 4v	1,717,986,918 = 8ma
	858,993,459 = 2v	858,993,459 = 4ma
	0 = 0v	0 = 0ma

1.4.15 WEXP Discrete I/O, Non-isolated

These DIOs are identical to those described in the Discrete Input and Output, Non-isolated *STWC* board.

UCPA for Hazardous Locations (HazLoc)

This equipment is suitable for use in Class I Division 2 Groups ABCD, Class I Zone 2, and ATEX Zone 2 locations.

Warning

Refer to *Mark VIe UCPA Controller Instructions for Safe Use (GFK-2951)* for requirements.

UCPA and Federal Communications Commission (FCC) Compliance

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.

   and

2. This device must accept any interference received, including interference that may cause undesired operation.

Caution

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

1.4.16 UCPA Controller Replacement

➢ **To replace the UCPA**

1. Lock out and tag out the equipment.
2. Disconnect the incoming 12 V dc power plug.
3. Disconnect the Ethernet cables.
4. Remove the terminal wiring.
5. Remove the screws holding the controller in place.
6. Remove the old controller from the panel.
7. If installing a new UCPAH2A that has the WEXP, remove the plastic cover to set the jumpers if needed. Refer to the controller *Installation* section for more information.
8. Reinstall the new controller by reversing steps 6 through 1.
9. Transfer the UDH network IP address to the new UCPA controller. Refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703), the section *Configure and Transfer IP Address to UCPA Controller.*
10. Download the firmware and application to the new controller.
11. From the ToolboxST application, verify the status of the controller. It should be in the controlling state with no warnings or errors.

1.5 Password Protection

Beginning with Mark VIe controller firmware V06.00.00C, password protection can be applied as a security measure to restrict access to the controller. The password has an eight-character limit and other requirements. For the instructions to set password protection, change the password, and other details, refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703), the section *System Password Protection* for your component.

1.6 Shared IONet

The Shared IONet function (with ControlST* V04.06 or higher) enables the sharing of Mark VIeS Safety inputs or Mark Stat Wind Converter inputs with another basic process Mark VIe controller set, saving the cost of redundant sensors and I/O. Refer to GEH-6812, Mark Controllers Shared IONet User Guide for more information. Specific configurations supported include:

- One Mark VIeS UCSB Safety controller set and one Mark VIe UCSB controller set
- One Mark Stat Wind power conversion controller UCSB set and one Mark VIe UCSB controller set
- Two Mark VIe UCSB controller sets

Note The UCPA does not support Shared IONet.

The UCSA does not support Shared IONet.

1.7 Auto-Reconfiguration

Note Auto-reconfiguration is not available for the Mark VIeS Safety controller.

The Auto-Reconfiguration feature of the Mark VIe controller allows Mark VIe I/O modules to be replaced without operator configuration. Auto-Reconfiguration is available with the ControlST* software suite V 03.05.00C or later. If Auto-Reconfiguration is enabled, when the controller detects a new I/O module starting with a different configuration, a reconfiguration file is automatically downloaded from the controller to the I/O module. This reconfiguration includes the bootload, baseload, firmware, and parameters. Each I/O module is updated with the current configuration that matches the configuration used by the controller, unless it already contains the latest version.

While an Auto-Reconfiguration is in progress, the Mark VIe controller will not allow a restart until the Auto-Reconfiguration has completed. Other downloads to the I/O module cannot be initiated while it is being auto-reconfigured. If the I/O module is already running the correct configuration, Auto-Reconfiguration only performs diagnostics.

Auto-Reconfiguration is enabled or disabled in the ToolboxST application through the Component Editor. This allows the operator to manually reconfigure each I/O module if needed. If a terminal board is replaced, the I/O module must be manually reconfigured. From the Component Editor, press F1 for help.

When power is applied, the I/O module starts and, if enabled, the Auto-Reconfiguration process starts. It generates a signal to the Mark* VIe controller, requesting an IP address and configuration. The Mark VIe controller queries the I/O module, identifies existing files to determine if a reconfiguration is needed, downloads the IP address and reconfiguration files, then signals the I/O module when the download is complete. The I/O module restarts, performs a self-diagnostic test, and goes online.

When replacing an I/O module with one that already has the proper baseload and firmware, the Auto-Reconfiguration process takes a relatively short time (less than a minute). When the baseload and/or firmware needs to be reloaded, the Auto-Reconfiguration process may take a few minutes to complete.

1.8 Controller Interoperability

Beginning with ControlST V07.04, Mark VIe redundant configurations can support interoperable controllers, with different platform types interoperating in a redundant set. Each controller in the redundant set displays as a separate Platform entry in the Property Editor. If the <R> controller Platform is set to a controller type that is not interoperable then only a single platform entry is provided for all controllers. If one controller in an interoperable set fails, operators can replace it with the same or a different supported controller type while the process being controlled is still running, without losing plant control. (ToolboxST supports online replacement.)

Examples of interoperable controllers are:

- UCSBH1A, UCSCH2A
- UCSBH4A, UCSCH2A

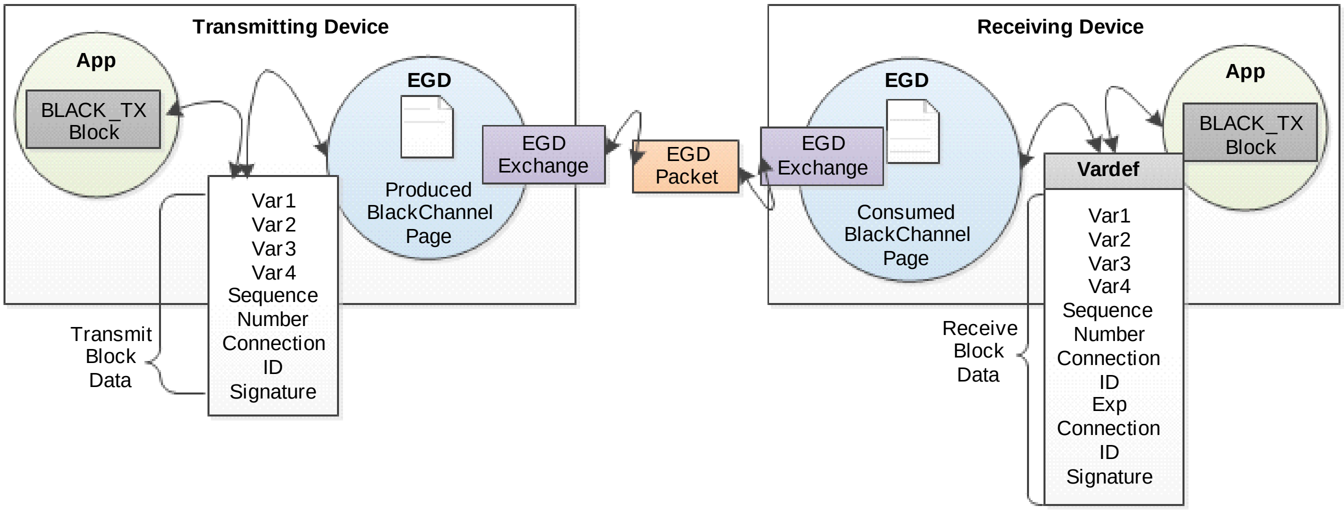
For instructions to replace a controller in a redundant set with an interoperable controller, refer to the *ToolboxST User Guide for Mark Controls Platforms* (GEH-6703), the section *Controller Interoperability.*

For upgrade instructions, refer to *Mark VIe Interoperable Controller Upgrade Instruction Guide* (GEI-100871).

1.9 Black Channel Safety Communication

Black channel is a safety communications approach in which the new safety functionality is built over existing protocol without impact to existing safety applications. The black channel feature provides the transfer of safety control data between two Mark VIeS Safety control devices without using the standard UDH network (providing a safer, less congested network). A matching pair of transmitter and receiver blocks, *BLACK_TX* and *BLACK_RX*, are configured for the two Mark VIeS Safety control devices in the application. The data is passed through Ethernet (similar to UDH EGD), and the BLACK_TX and BLACK_RX blocks run a data integrity check on each respective side of the Black Channel.

Note Refer to GEI-100691, Mark VIeS Safety Control Block Library, Black Channel Transmitter (BLACK_TX) and Black Channel Receiver (BLACK_RX) blocks.



1.10 Controller Setup and Download

After a controller and associated I/O modules have been added to the system, prepare the controller for use by configuring the IP address and redundancy information using the ToolboxST application. For further instructions and procedures, refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703), the sections *Controller Setup* and *Build and Download to Controller.*

1.11 Initial Download to I/O Modules

1.11.1 Update Terminal Boards

Prerequisites

- Successfully online with the associated controller set
- All I/O modules have been correctly added to the ToolboxST system
- Correctly connected IONet cables to all the I/O modules
- I/O modules are powered on

Complete this procedure to detect the terminal board barcodes.

➢ To update terminal boards online

1. If not already online, then from the Component Editor toolbar click the **Go On/Offline** icon to go online with the ToolboxST application.
2. Have available or create a written record of all installed terminal boards.
3. Enable the I/O modules for configuration.
    a. From the Component Editor Hardware tab, select all the I/O modules.
    b. From the Property Editor, under **Configuration**, **Required**, select **True**.
4. From the **Tree View**, double-click the I/O module icon to display the **Modify** dialog box.
5. From the **Bar Code** text box, click the ellipsis button to display the **Select Unassigned Terminal Board** dialog box with the available terminal boards.
6. From the dialog box, select the correct **Bar Code** and click **OK**.
7. Read the warning message, then click **Yes**.
8. Click **OK**.
9. Repeat this procedure for the remaining I/O modules.
10. Verify using the written record that all terminal boards have been identified by the ToolboxST application.

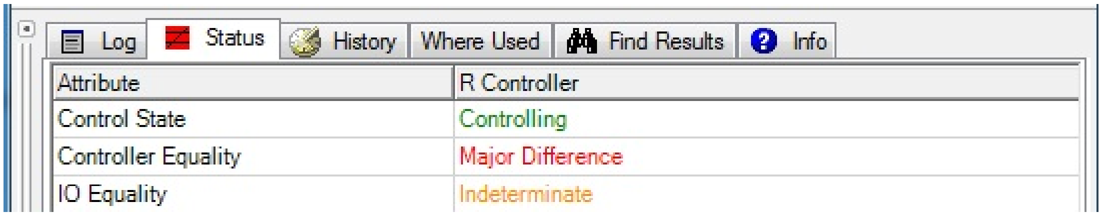
1.11.2 Initial Download to I/O Modules

➢ To perform an initial download

1. If using Shared IONet, save and close both Component Editors. From the System Editor **Tree View**, select the Shared IONet Group. Right-click and select **Download Shared IONet**, then complete the wizard. Go to step 4.
2. From the Component Editor, click **Build**.
3. Click **Download** and complete the wizard using the default settings.
4. Cycle power to the panel. Wait for all equipment to power on with correct status LEDs.
5. Click to go online.
6. Wait and reset any alarms, if needed.
7. Build and Download again, if needed.
8. Wait and reset any alarms, if needed.
9. Select the **Component InfoView Status** tab.

The color of the Status tab indicates overall health and equality status of the controller, including its associated I/O hardware. A major difference in controller equality means that the configuration in the ToolboxST application is different from the controller configuration.

- *Green* indicates that the ToolboxST configuration and the controller configuration are equal.
- *Orange* indicates the presence of inequalities or diagnostic warnings.
- *Red* indicates that the configuration in the ToolboxST system, which includes base load, firmware, application code, and I/O module configuration, is significantly different from the component configuration (a *Download* will correct this).

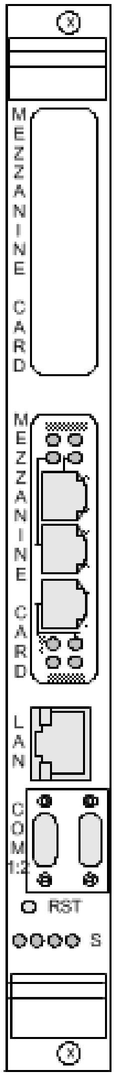


Attribute	R Controller
Control State	Controlling
Controller Equality	Major Difference
IO Equality	Indeterminate

Note Refer to GEH-6721_Vol_I, the chapter *Troubleshooting* for further assistance. For example, if a particular download fails, this may be fixed by selecting the pack individually from the download wizard and trying again.

1.12 UCCx Controllers

Note Mark VIeS Safety Controller V05.03 is the most current firmware version that still supports the UCCx platform. Beginning with ConstrolST V07.02, the UCCx is installed from the ControlST Software Suite DVD by selecting the ControlST Supplement Package installation option. Refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703), the section *Installation* for more information.



The UCCx controller is a single-board computer that runs the application code. The controller mounts in a CompactPCI (CPCI) enclosure and communicates with the I/O packs through on-board I/O network interfaces. The CPCI enclosure typically consists of a 6U high rack, one or two 3U high power supplies, a 6U high single board, and a cooling fan. The rack backplane is CPCI compliant, but is used only to provide power from the power supply(s) to the controller and cooling fan. The CPCI power supply converts the bulk incoming power to ±12 V dc, 5 V dc, and 3.3 V dc. These voltages are distributed to the controller(s) and fan through the backplane.

The CPCI power supply takes the incoming bulk power from the CPCI backplane and creates ±12, 5, and 3.3 V dc. This power is provided to the backplane through one or two Mate-N-Lok® connectors, for use by the power supply(s), controller(s) and cooling fan. The power supply is a CPCI hot swap compliant 3U power supply using the standard CPCI 47-pin connector. Two power supplies can be used to provide power supply redundancy in an optional rack.

The controller operating system (OS) is QNX® Neutrino®, a real-time, multitasking OS designed for high-speed, high-reliability industrial applications. The following communication ports provide links to I/O modules, operator, and engineering interfaces:

- Ethernet connection for the Unit Data Highway (UDH) for communication with HMIs, and other control equipment. The UCCC controller has an additional Ethernet connection for the Control Data Highway (CDH).
- RS-232C connection for setup using the COM1 port
- Ethernet connection for the R, S, and T I/O network

The I/O networks are private, special-purpose Ethernet that support only the I/O modules and the controllers.

1.12.1 Installation

The enclosure contains (at a minimum) a controller and a four-slot CPCI rack with either one or two power supplies. The primary controller must be placed in the left-most slot (slot 1). A second, third, and fourth controller can be placed in a single rack. If the slot 1 controller is removed, the other controllers will stop operating.

The CMOS battery is disconnected using a processor board jumper during storage to extend the life of the battery. When installing the board, the battery jumper must be reinstalled. Refer to the specific UCCx module drawing for jumper location. The battery supplies power to the CMOS RAM settings and the internal date and real-time clock. There is no need to set CMOS settings since the settings are defaulted to the proper values through the BIOS. Only the real-time clock must be reset. The initial date and time can be set using a system NTP server or ToolboxST* application.

If the board is the system board (slot 1 board) and other boards are in the rack, ejection of the system board will cause the other boards to stop operating. It is recommended that power be removed from the rack when replacing any board in the rack. Rack power can be removed by one of the following methods:

- In a single power supply unit, a switch is provided to disable the power supply outputs.
- In a dual power supply unit, both power supplies can be safely ejected to remove power.
- Unplug the bulk power input Mate-N-Lok connector(s) on the bottom of the CPCI enclosure.
- Use a remote disconnect switch.

Note Unlike the Mark VI control VME boards that provided only ejectors, the UCCC has injectors/ejectors at the bottom and top of the module.

Before sliding the board in the rack, the top ejector should be tilted up and the bottom ejector should be tilted down. When the connector on the backside of the board connects with the backplane connector, the injectors should be used to fully insert the board. This is done by pushing down on the top injector and pulling up on the bottom ejector. Remember to finish the installation by tightening the top and bottom injector/ejector screws. This provides mechanical security as well as a chassis ground connection.

Note Failing to lock the injectors will prevent the controller from booting. When extracting the board, perform the insertion process in reverse. See the next section on configuration before connecting the Ethernet cables. If a previous application is loaded in the module, mis-operation can occur if the Ethernet addresses collide with other operating equipment.

1.12.2 Operation

With the Mark VIeS Safety controller, if controller application code is changed and downloaded, a Branding of the new code will be required. Changes that are not downloaded may cause a Brand change. Refer to GEH-6723, Mark VIeS Safety Control Safety Instruction Guide, the section Application Code Branding. Minor modifications to the control software may be made online without requiring a restart.

The controller is loaded with software specific to its application, which includes but is not limited to steam, gas, and land-marine aeroderivative (LM), or balance-of-plant (BOP) products. It can run rungs or blocks. The IEEE® 1588 protocol is used through the R, S, and T IONets to synchronize the clock of the I/O packs and controllers to within ±100 micro seconds.

External data is transferred to and from the control system database in the controller over the R, S, and T IONets.

In a simplex system, this includes process inputs/outputs to the I/O packs.

In a dual system:

- Process inputs/outputs to the I/O packs
- Internal state values and initialization information from the designated controller
- Status and synchronization information from both controllers

In a triple modular redundant (TMR) system:

- Process inputs/outputs to the I/O packs
- Internal state values from for voting and status and synchronization information from all three controllers
- Initialization information from the designated controller

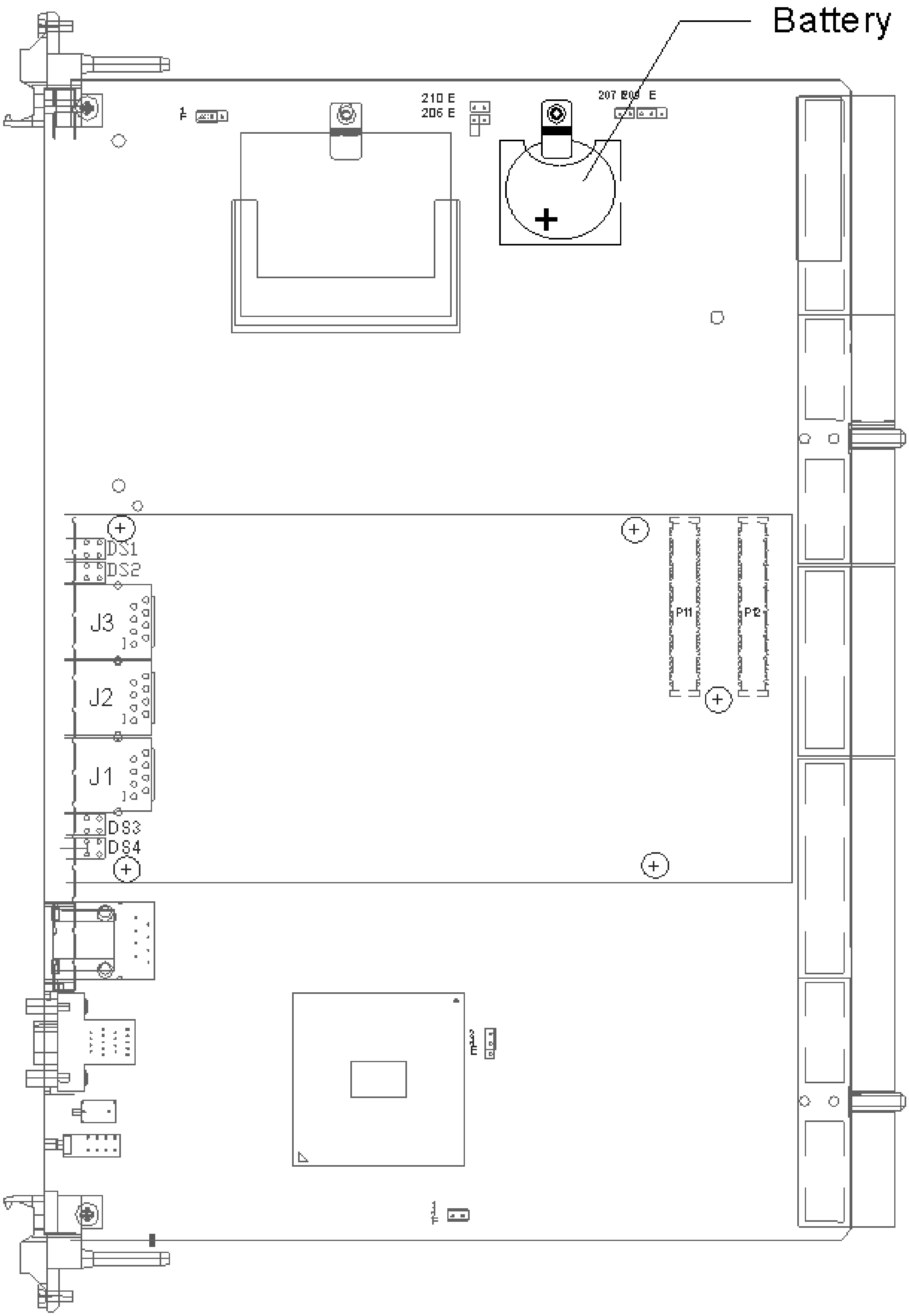
1.12.2.1 Controller Battery

The UCCC uses a lithium battery to supply power to the CMOS (which contains the BIOS settings for the CPU board) and the real-time clock when the controller is not on. Default CMOS settings are also stored in flash memory, so when the battery reaches end-of-life, only the real-time clock functions are lost.

The lithium battery for the UCCC has a service life of 10 years. The battery is disabled in stock and can be disabled when storing a controller. If the controller is stored with the battery disabled, its life expectancy is 10 years, minus the time the controller has been in service. If the controller is stored with the battery enabled, the life expectancy drops to seven years minus the time the controller has been in service. An expired battery can be replaced on the controller board.

➢ **To replace the controller battery**

1. Power down the CPCI rack. If the rack has a single power supply (version P1), turn off the power switch located on the panel above the power supply.
2. Loosen the screws at the top and bottom of the controller.
3. Press down on the top ejector tab and pull up on the bottom ejector tab to disconnect the controller from the backplane. Carefully pull the controller out of the CPCI rack.
4. Locate the battery near the top, inboard side of the controller.
5. Loosen the screw on the tab holding the battery and move it out of the way.
6. Slide the expired battery out of its enclosure, making note that the positive (+) side faces away from the controller.
7. Insert the new battery. Reposition the holding tab and tighten the screw.
8. Slide the controller back into the CPCI rack and secure it in place.
9. From the ToolboxST application, reset the real-time clock.


Battery
210 E
206 E
207 209 E
DS1
DS2
J3
J2
J1
DS3
DS4
P11
P12

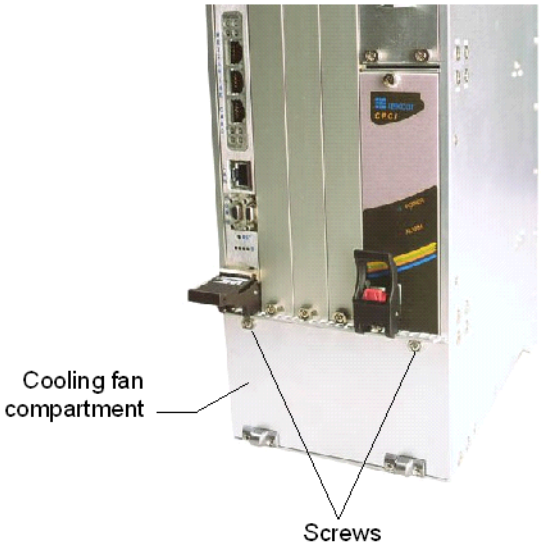
1.12.2.2 Cooling Fan

A cooling fan is located in a tray at the bottom of the CPCI rack. The cooling fan can fail, causing temperatures to rise to a level that will damage the controllers and power supplies. The cooling fan can be replaced without removing power to the rack.

Note The controller automatically monitors the CPU core temperature and can be configured to continue to run, or to reboot the controller into a low power failure state. Refer to the *Mark VIe Controller Standard Block Library* (GEI-100682), the section *Temperature Status (TEMP_STATUS)*.

➢ **To replace the cooling fan**

1. Loosen the two screws at the top of the door located at the bottom of CPCI rack.
2. Open the door and slide the old cooling fan out of the rack. There are no cables to remove. The fan assembly plugs directly into the backplane.
3. Insert a new cooling fan into the guides in the compartment and push in firmly. If the fan is not completely in place, the compartment door will not close.
4. Close the door and tighten the two screws at the top.



Replacing CPCI Cooling Fan

1.12.2.3 EPMC

The CPCI controllers support a single PCI Mezzanine Card (PMC) daughterboard called the IS200EPMC.

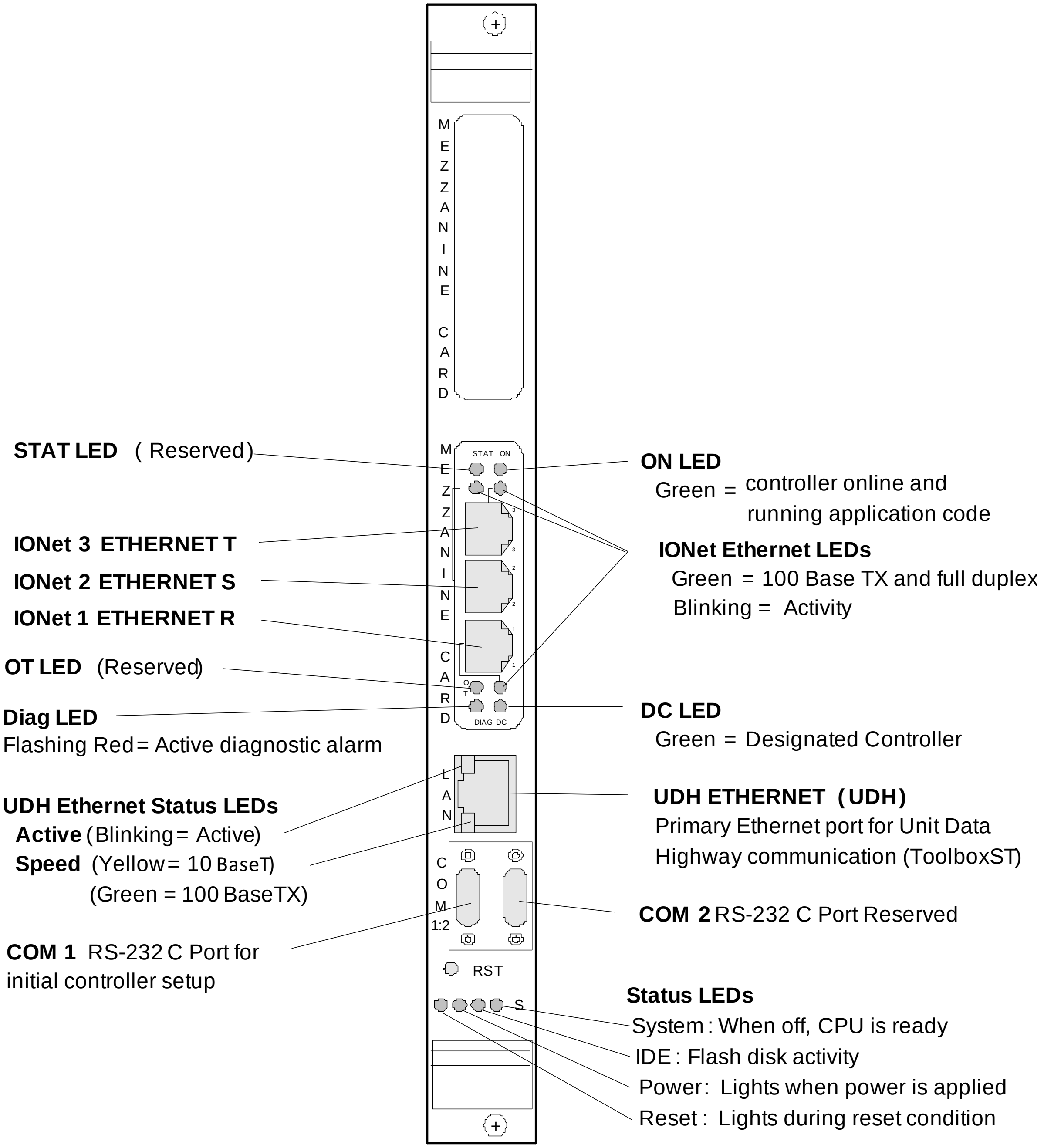
The IS200EPMC contains specific controller hardware functions as follows:

- Power supply monitoring
- Flash backed SRAM
- IONet Ethernets
- Ethernet physical layer packet snooping for precision time synchronization

The EPMC board plugs onto one of the PMC sites and communicates to the processor board through the PCI bus. The PCI interface on the EPMC is PCI Rev 2.2 compliant and supports both 3.3 V and 5 V signal levels.

1.12.2.4 UCCA Processor

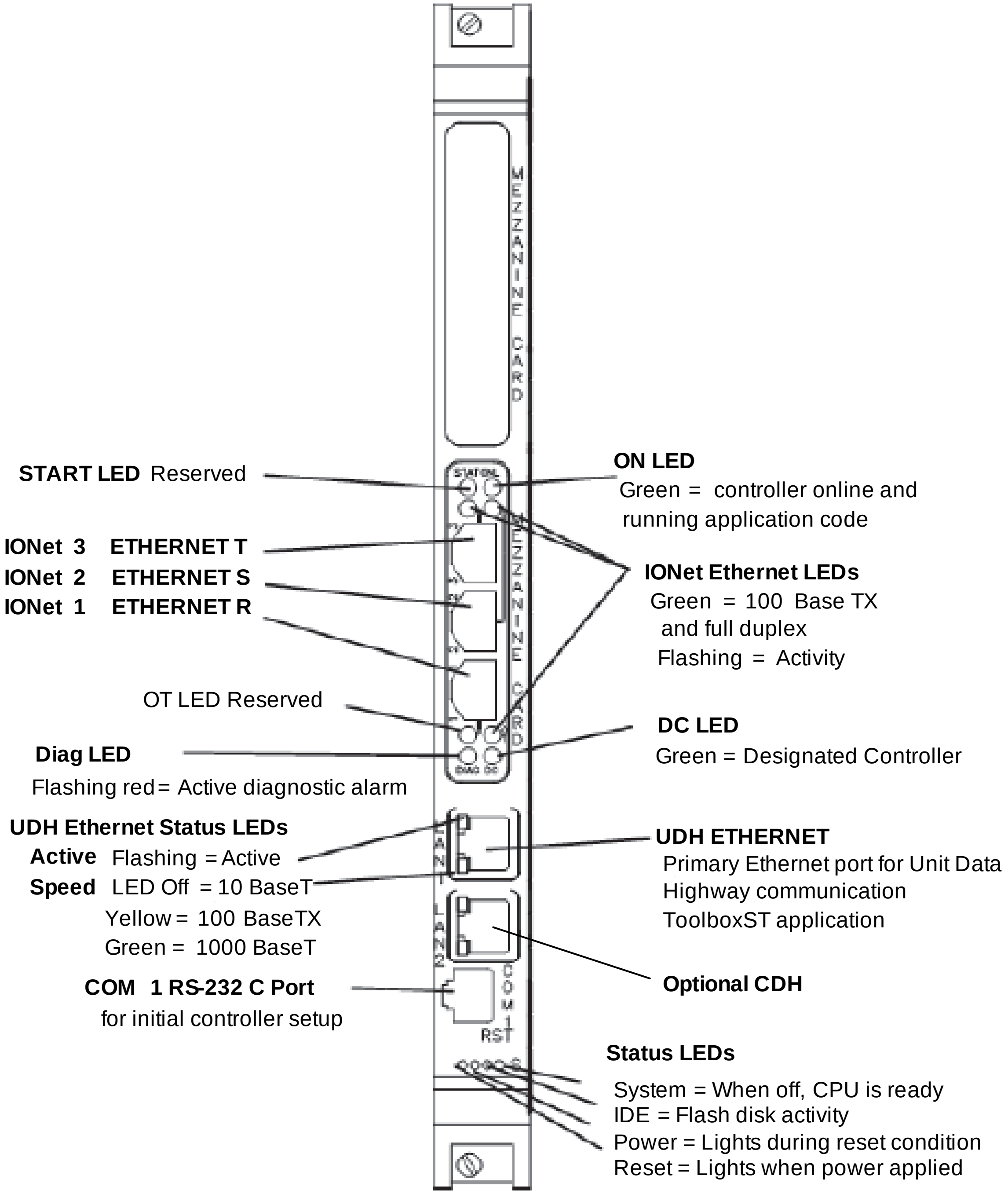
The UCCA (IS215UCCAH3) is a single-slot board using a 650 MHz Intel® Celeron® processor. A 10Base-TX/100Base-TX (RJ-45) Ethernet port provides connectivity to the Unit Data Highway (UDH). There are two PCI Mezzanine Card (PMC) sites and a watchdog timer. The processor board is the compute engine of the Mark VIe controller. The IS215UCCAM03 is a module assembly that includes the IS215UCCAH3 combined with 128 MB of flash memory, 128 MB of DRAM, and the IS200EPMC.


MEZZANINE CARD
MEZZANINE CARD
STAT ON
3
3
2
2
1
1
OT
DIAG DC
LAN
COM 1:2
RST
S
STAT LED (Reserved)
IONet 3 ETHERNET T
IONet 2 ETHERNET S
IONet 1 ETHERNET R
OT LED (Reserved)
Diag LED
Flashing Red = Active diagnostic alarm
UDH Ethernet Status LEDs
Active (Blinking = Active)
Speed (Yellow = 10 BaseT)
(Green = 100 BaseTX)
COM 1 RS-232 C Port for initial controller setup
ON LED
Green = controller online and running application code
IONet Ethernet LEDs
Green = 100 Base TX and full duplex
Blinking = Activity
DC LED
Green = Designated Controller
UDH ETHERNET (UDH)
Primary Ethernet port for Unit Data Highway communication (ToolboxST)
COM 2 RS-232 C Port Reserved
Status LEDs
System : When off, CPU is ready
IDE : Flash disk activity
Power: Lights when power is applied
Reset : Lights during reset condition

UCCA LEDs and Connections

1.12.2.5 UCCC Processor

The IS215UCCCH4 is a single-slot CPCI controller board containing a 1.6 GHz Pentium® M processor. Two 10/100/1000Base-TX Ethernet ports provide connectivity to the UDH and an optional Control Data Highway (CDH). The IS215UCCCM04 is a module assembly that includes the IS215UCCCH4 combined with 128 MB of flash memory, 256 MB of DRAM, and the IS200EPMC.


MEZZANINE CARD
START LED Reserved
ON LED
Green = controller online and running application code
IONet 3 ETHERNET T
IONet 2 ETHERNET S
IONet 1 ETHERNET R
IONet Ethernet LEDs
Green = 100 Base TX and full duplex
Flashing = Activity
OT LED Reserved
DC LED
Green = Designated Controller
Diag LED
Flashing red = Active diagnostic alarm
DIAG DC
UDH Ethernet Status LEDs
Active Flashing = Active
Speed LED Off = 10 BaseT
Yellow = 100 BaseTX
Green = 1000 BaseT
UDH ETHERNET
Primary Ethernet port for Unit Data Highway communication ToolboxST application
LAN 1
LAN 2
Optional CDH
COM 1 RS-232 C Port for initial controller setup
COM 1
RST
Status LEDs
System = When off, CPU is ready
IDE = Flash disk activity
Power = Lights during reset condition
Reset = Lights when power applied

UCCC LEDs and Connections

1.12.3 Specifications

1.12.3.1 UCCAM03 Specifications

Item	UCCA Specification
Microprocessor	Intel Ultra Low Voltage Celeron 650 MHz (8.3 Watts max)
Memory	128 MB DDR SDRAM through one SODIMM 256 KB L2 cache Flash-backed SRAM - 8K allocated as NVRAM for controller functions
Flash	128 MB ComactFlash module (GE part #336A5196AAP8)
Operating System	QNX Neutrino
Programming	Control block language with analog and discrete blocks; Boolean logic represented in relay ladder diagram format. Supported data types include: Boolean 16-bit signed integer 16-bit unsigned integer 32-bit signed integer 32-bit unsigned integer 32-bit floating point 64-bit long floating point
Primary Ethernet interface (one port)	TCP/IP protocol for communication between controller and ToolboxST application TCP/IP protocol used for alarm communication to HMIs Ethernet Global Data (EGD) protocol for application variable communication with CIMPLICITY® HMI and Series 90-70 programmable logic controllers (PLCs) Ethernet Modbus® protocol supported for communication between controller and third-party distributed control system (DCS)
EPMC Ethernet Interface (three ports)	Twisted pair 10Base-TX/100Base-TX, RJ-45 connectors: TCP/IP protocols used to communicate between controllers and I/O modules
COM ports	Two micro-miniature 9-pin D connectors: COM1 Reserved for diagnostics, 9600 baud, 8 data bits, no parity, 1 stop bit COM2 Not used For cabling, use one of the following: GE-provided Ethernet cables, which are specifically designed for use in the Mark* controller product family (GE part #342A4931ABP1) and a controller connector (GE part #342A4931ABP2), or a miniature D shell, null modem serial cable (GE part #336A3582P1), connected with a micro-miniature pigtail (GE part #336A4929G1)
Power requirements	3.3 V dc, 3.5 A typical, 4.25 A maximum 5 V dc, 150 mA typical, 300 mA maximum
† Ambient rating for enclosure design	0 to 60°C (32 to 140 ºF)
Technical Regulations, Standards, and Environments	† Refer to GEH-6721_Vol_I, the chapter *Technical Regulations, Standards, and Environments* for additional equipment rating information depending on application requirements.

1.12.3.2 UCCC Specifications

Item	**UCCC Specification**
Microprocessor	Intel Pentium M processor 1.6 GHz
Memory	256 MB DDR SDRAM through one SODIMM 128 MB CompactFlash Module 256 KB L2 cache Flash-backed SRAM - 8K allocated as NVRAM for controller functions
Flash	128 MB ComactFlash module (GE part #336A5196AAP8)
Operating System	QNX Neutrino
Programming	Control block language with analog and discrete blocks; Boolean logic represented in relay ladder diagram format. Supported data types include: Boolean 16-bit signed integer 16-bit unsigned integer 32-bit signed integer 32-bit unsigned integer 32-bit floating point 64-bit long floating point
Primary Ethernet Interface (2)	Twisted pair 10Base-TX/100Base-TX, RJ-45 connectors: TCP/IP protocol used for communication between controller and toolbox TCP/IP protocol used for alarm communication to HMIs EGD protocol for application variable communication with CIMPLICITY HMI and Series 90-70 PLCs Ethernet Modbus protocol supported for communication between controller and third-party DCS
EPMC Ethernet Interface (3 ports)	Twisted pair 10Base-TX/100Base-TX, RJ-45 connectors: TCP/IP protocols used to communicate between controllers and I/O packs
COM port	One accessible through RJ-45 connector on front panel For cabling use GE-provided Ethernet cables, which are specifically designed for use in the Mark* controller product family (GE part #342A4931ABP1)
Power Requirements	5 V dc (5%, -3%, 4.5 A (typical), 6.75 maximum) 3.3 V dc, (5%, -3%, 1.5 A (typical), 2.0 A maximum) 12 V dc (5%, -3%), 50 mA maximum -12 V dc (5%, -3%), 50 mA maximum
Mechanical Specifications	Shock: 10 Gs, 16 ms half sine, 6 axis, 10 pulses each Vibration: 6 Gs rms (20-2000 Hz) random, 0.0185 G2 per Hz
† Ambient rating for enclosure design	0 to 50°C (32 to 122 °F)
† Refer to GEH-6721_Vol_I, the chapter *Technical Regulations, Standards, and Environments* for additional equipment rating information depending on application requirements.	

1.12.4 Diagnostics

Refer to the figures in the *UCCA Processor* and *UCCC Processor* sections for an explanation of LEDs.

1.12.5 Configuration

The controller must be configured with a TCP/IP address prior to connecting to the UDH or CDH Ethernet. This is achieved through the ToolboxST application and the COM1 serial port.

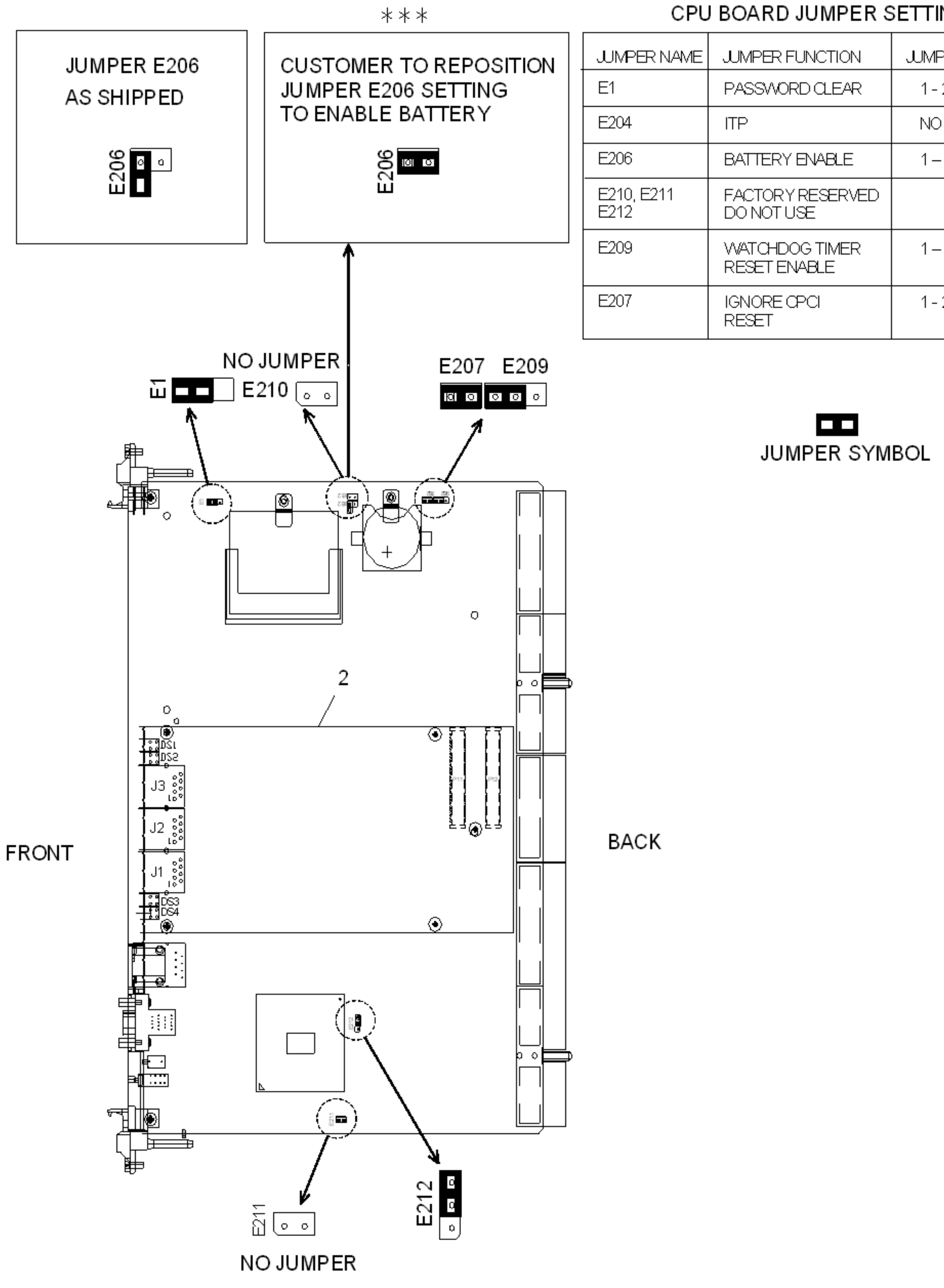
1.12.5.1 UCCA Jumper Settings

Caution

Airflow requirements as measured at the output side of the heat sink must be greater than 400LFM to prevent overheating and potential damage to the board.

CPU BOARD JUMPER SETTINGS

JUMPER NAME	JUMPER FUNCTION	JUMPER POSITION
E1	PASSWORD CLEAR	1 - 2
E204	ITP	NO JUMPERS
E206	BATTERY ENABLE	1 – 2 ***
E210, E211 E212	FACTORY RESERVED DO NOT USE	
E209	WATCHDOG TIMER RESET ENABLE	1 – 2
E207	IGNORE CPCI RESET	1 - 2

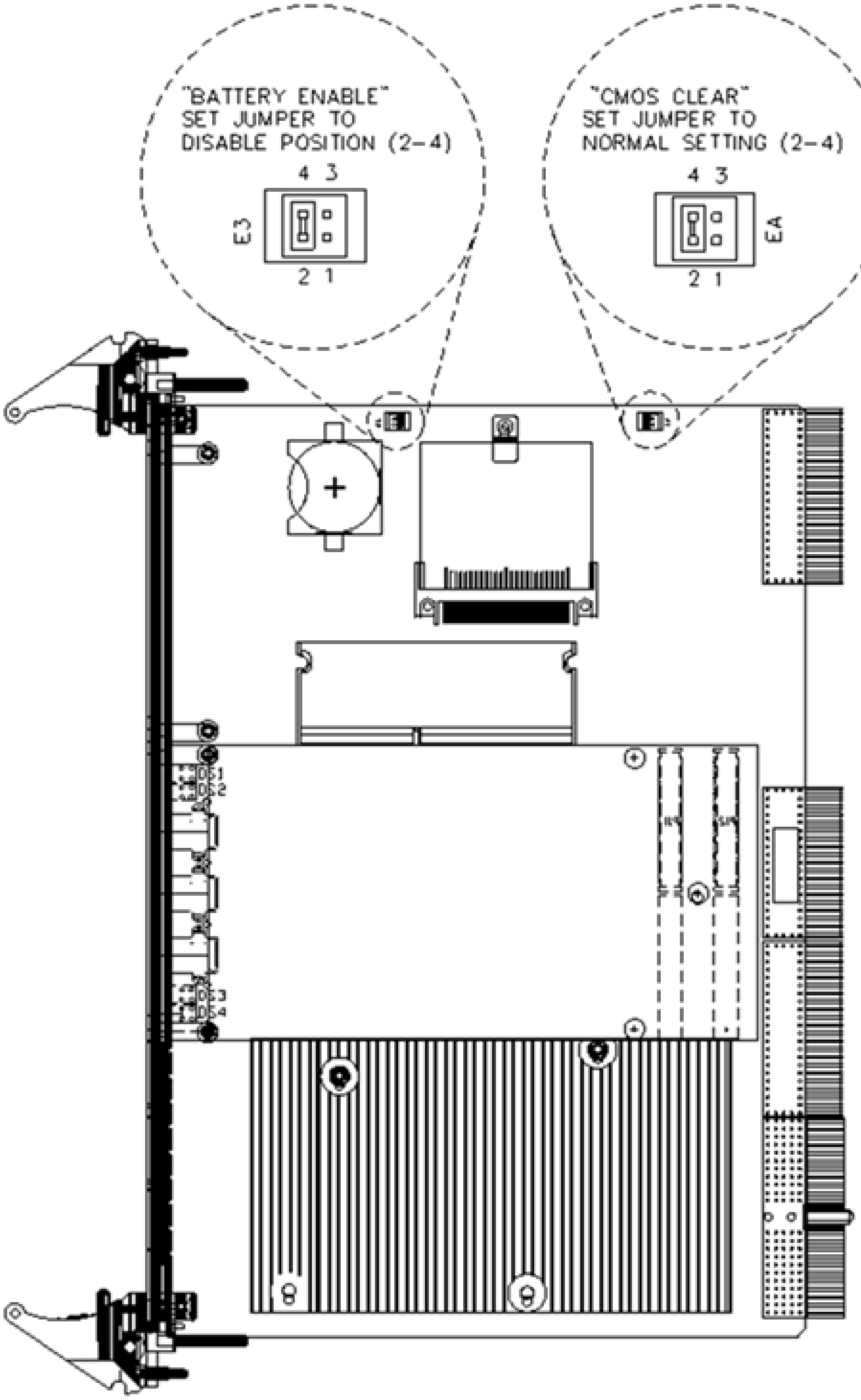


UCCA Jumper

1.12.5.2 UCCC Jumper Settings

Caution

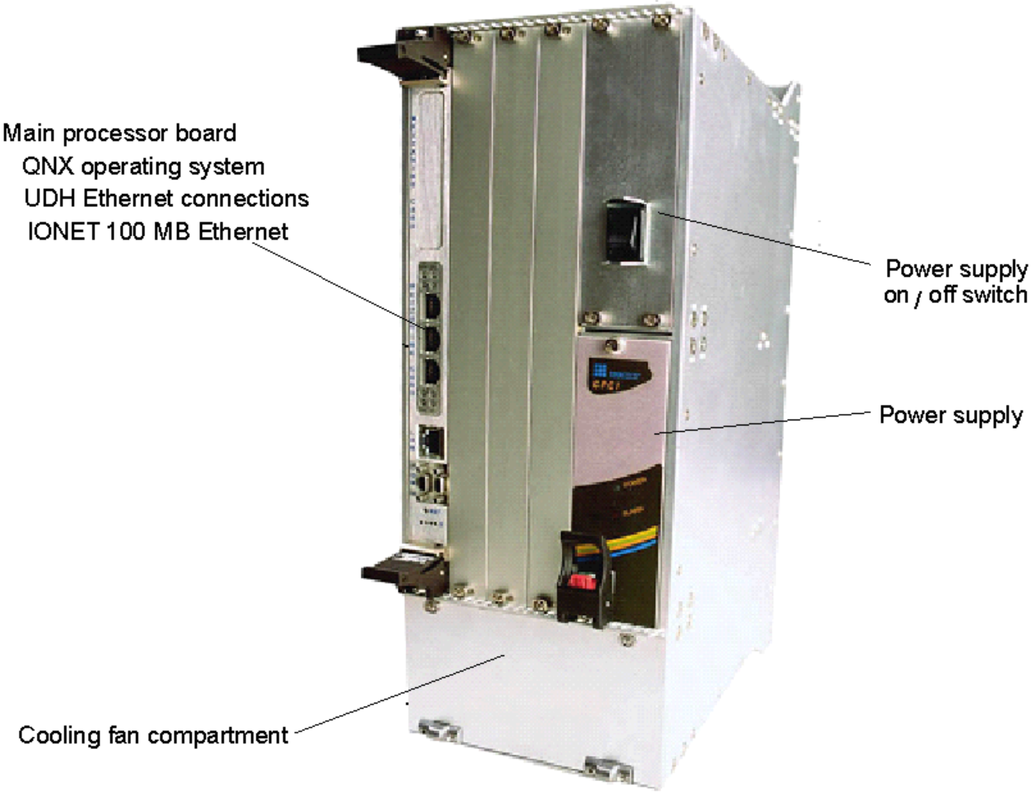
Airflow requirements as measured at the output side of the heat sink must be greater than 300LFM to prevent overheating and potential damage to the board.



UCCC Jumper

1.12.6 CPCI Rack

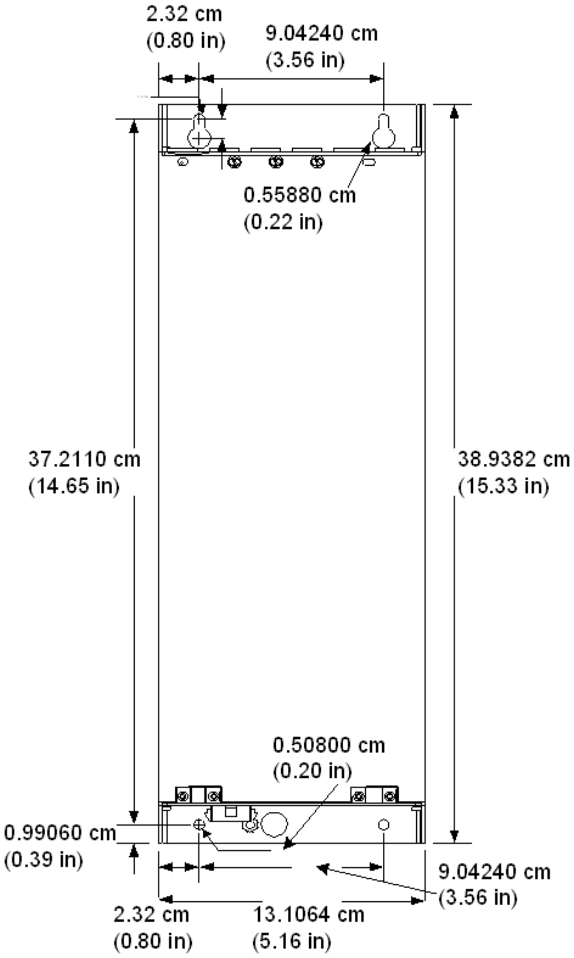
The CPCI rack provides an enclosure for the controller, an enclosure for the power supplies(s), and a cooling system. The rack backplane is only used to connect the power supplies to the controller and cooling fans.

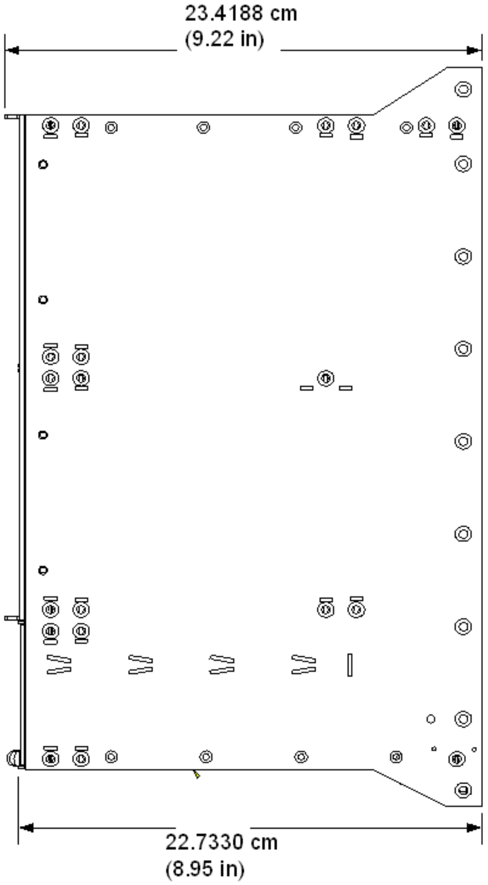


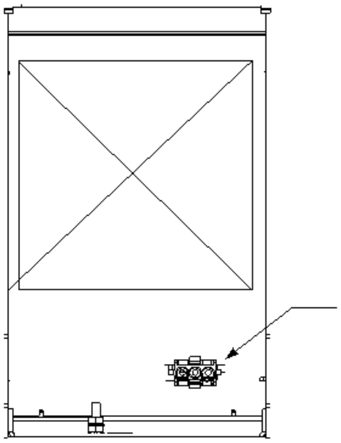
CPCI Rack

1.12.6.1 Installation

The CPCI rack is designed to be wall-mounted. Use the following drawing to determine the placement of the mounting hardware and the enclosure space required.







Power supply connector pin definitions

P1 = ac line or dc-
P2 = ac neutral or dc+
P3 = GND

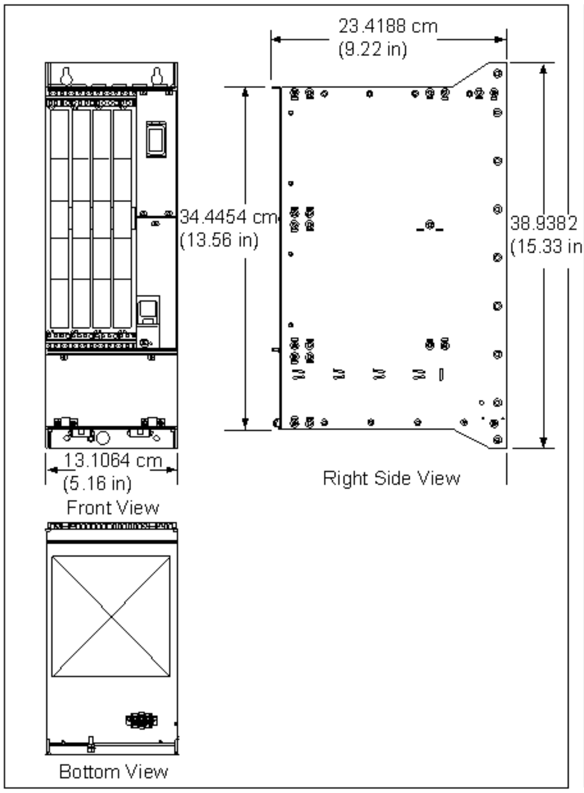
The plug connector is AMP# 350550-7 or equivalent with receptacle connector AMP#250766-1 or equivalent contacts.

1.12.6.2 Operation

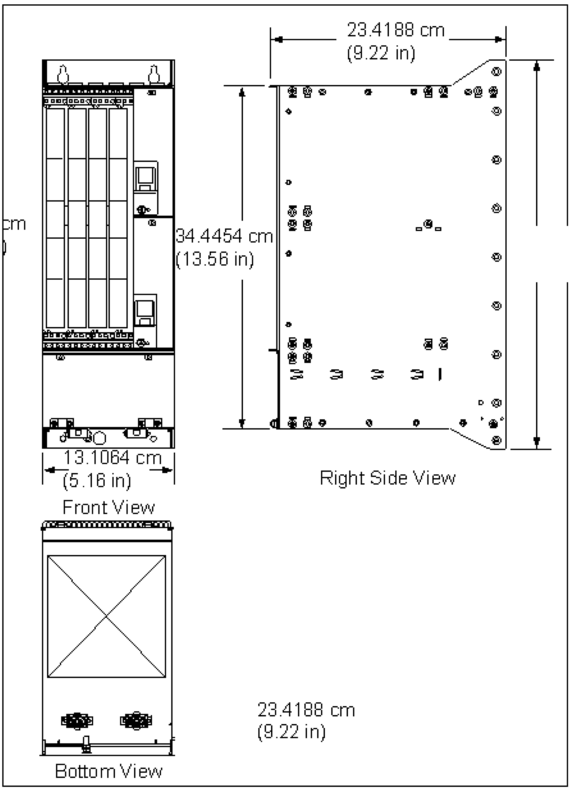
Bulk incoming power is supplied to the rack using one or two power connectors. The CPCI power supply converts the bulk input to ±12 V dc, 5 V dc, and 3.3 V dc. These voltages are distributed to the controllers and fans through the backplane.

Available Rack Parts

Catalog #	# Power Supplies Ports	Power Inputs
336A4940CTP1	1	1
336A4940CTP2	2	2



Part 1 (Single Power Supply)



Part 2 (Dual Power Supply)

The P1 version contains a on/off switch located in the upper right panel. The switch is connected to the disable outputs pin of the power supply, which turns off power to the controllers and fans. The P2 version does not have a switch so power is removed by ejecting the power supplies, disconnecting the incoming bulk power plugs or using a remote disconnect.

1.12.6.3 Specifications

Item	CPCI Rack Specification
Air flow provided	90 linear m (300 linear ft) per minute
Technical Regulations, Standards, and Environments	Refer to GEH-6721_Vol_I, the chapter *Technical Regulations, Standards, and Environments* for additional equipment rating information depending on application requirements.

1.12.6.4 CPCI Component Replacement

➢ **To replace the CPCI controller**

1. Power down the CPCI rack. If the rack has a single power supply (version P1), turn off the power switch located on the panel above the power supply. The power can also be removed by disconnecting the bulk power plug from the bottom of the rack or by using a remote disconnect.
2. When two power supplies are used (version P2), loosen the top and bottom screw on each one. Press down the red tab in the black release lever on each power supply. Press down on the black release lever and pull out to disconnect both power supplies from the CPCI rack backplane. The power can also be removed by disconnecting the bulk power plugs from the bottom of the rack or by using a remote disconnect.
3. Disconnect the IONet cables.
4. Disconnect the VLAN cable.
5. Loosen the screws at the top and bottom of the controller.
6. Press down on the top ejector tab and pull up on the bottom ejector tab to disconnect the controller from the backplane. Carefully pull the controller out of the CPCI rack.
7. If still functional, remove the CompactFlash® from the old controller, and install it into the new one.
8. Carefully slide the new controller module into the CPCI enclosure.
9. Press up on the top injector/ejector tab and push down on the bottom injector/ejector tab to seat the controller connectors with the receptacles on the backplane.
10. Tighten the screws at the top and bottom of the controller, securing it in the CPCI enclosure.
11. Power up the controller by turning on the power switch on CPCI enclosure with a single power supply or pushing in on both power supplies and securing them on a CPCI enclosure using dual supplies.
12. Connect the IONet cables.
13. Connect the VLAN cable.
14. If using new flash memory, configure the new controller's TCP/IP address.
15. From the ToolboxST application, verify the status of the controller. It should be in the controlling state with no warnings or errors and online.
16. If the ToolboxST application does not go online or the controller is not in the controlling state, download to the controller using the Download Wizard. Refer to *GEH-6700, ToolboxST* User Guide for Mark VIe* Control.*

1.12.7 CPCI Power Supply(s)

The CPCI power supply takes the incoming bulk power from the CPCI rack and creates ±12, 5, and 3.3 V dc. This power is provided to the backplane for use in the rack, mainly for the controller(s) and cooling fan.

The CPCI rack can hold one or two power supplies. The power supplies plug directly into the backplane using CPCI 47-pin connector. The power supply(s) are hot swap compliant and can be safely removed with powering down CPCI rack.

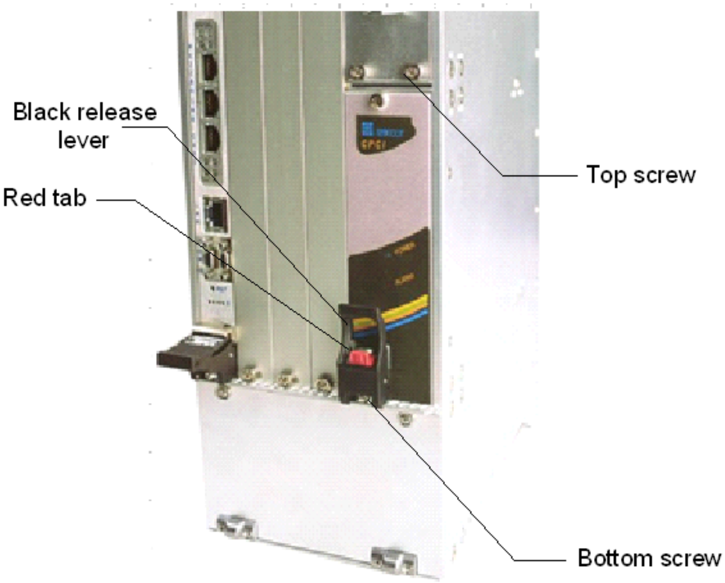
1.12.7.1 Installation

➢ **To remove the CPCI power supply(s)**

1. Loosen the two screws holding the power supply in the rack. The bottom screw is located beneath the black ejection lever at the bottom of the power supply faceplate.
2. Press down on the red tab inside the black ejection lever to release it.
3. Push the black release lever down to unplug the power supply from the backplane.
4. Slide the power supply out of the CPCI rack.

➢ **To install a new CPCI power supply(s)**

1. Slide the new power supply(s) into CPCI rack. Ensure the front of the power supply is flush with other components in the enclosure.
2. Push the black ejection lever up. The red tab in the black ejection lever will snap up when the power supply is fully inserted.
3. Tighten the top and bottom screws.



CPCI Power Supply

1.12.7.2 Operation

The power supply is a CPCI Rev 2.11 hot swap compliant 3U power supply using the standard Positronic® 47-pin connector. Remote sense and active current share on the +5 and +3.3 V dc outputs along with o-ring FETs allow it to be used in the dual power supply CPCI rack. The ±12 V dc outputs use regular o-ring diodes for parallel operation in the dual rack.

Supported Power Supply

Catalog #	Input Voltage
342A4920	20-36 V dc

1.12.7.3 Specifications

Item	CPCI Power Supply Specification
Vibration	Random vibration 10 Hz to 2 kHz, 3 axis (1 GRMS)
Incoming power	20-36 V dc
Output power	150 W (De-rated for 65°C [149 °F] operation and 3,000 m [10,000 ft] altitude)
Over temperature protection	System shut down due to excessive internal temperature, automatic reset
Over voltage protection	Latch style over-voltage protection (110% minimum to 130% of V nom)
Overload protection	Fully protected against output overload and short circuit. Automatic recovery upon removal of overload condition
Agency Approvals	UL 1950, UL 1950, EN60950 (TUV)
Dielectric withstand voltage	Input to output per EN60950 (minimum 1500 V dc)
ESD susceptibility	Per EN61000-4-2, level 4 (minimum 8 kV)
Radiated Susceptibility	Per EN61000-4-3, level 3 (minimum 10 V/M)
EFT Burst	Per EN61000-4-4, level 3 (minimum ±2 kV)
Input Surge	Per EN61000-4-5, level 3. (Line to Line minimum 1 kV) (Line to Ground minimum 2 kV)
Conducted Disturbance	Per EN61000-4-6, level 2 (maximum 3 V)
Insulation Resistance	Input to Output (Nominal 10 M Ω)
Technical Regulations, Standards, and Environments	Refer to GEH-6721_Vol_I, the chapter *Technical Regulations, Standards, and Environments* for additional equipment rating information depending on application requirements.

1.12.7.4 Diagnostics

20-36 dc Power Supply LEDs

LED	Description
Power	Solid green if all power supply outputs are OK
	LED will turn off on any output failure
Alarm	Solid red if one or more of the outputs have failed

1.12.7.5 Power Supply Replacement

➢ **To replace the CPCI power supply(s)**

1. Loosen the two screws holding the power supply in the rack. The bottom screw is located beneath the black ejection lever at the bottom of the power supply faceplate.
2. Press down on the red tab inside the black ejection lever to release it.
3. Push the black release lever down to unplug the power supply from the backplane.
4. Slide the power supply out of the CPCI rack.
5. Slide the new power supply(s) into the CPCI rack. Ensure the front of the power supply is flush with the other components in the enclosure.
6. Push the black ejection lever up. The red tab in the black ejection lever will snap up when the power supply is fully inserted.
7. Tighten the top and bottom screws. Refer to the figure *CPCI Power Supply*.

1.12.8 UCCx Replacement

Contact the nearest GE Sales or Service Office, or an authorized GE Sales Representative.

1.13 Controller Diagnostic Alarms

These diagnostic alarms are common among Mark Controls Platforms. However, some alarms are not applicable to all controller platforms.

0

Description Diagnostic Alarm Reset

20

Description ToolboxST application detects unhealthy link or loss of communication between [ ] and controller.

Possible Cause

- I/O pack configuration files missing
- I/O pack restarted or did not complete startup
- I/O pack configured for dual networks, but only one network is connected
- Network issue preventing connection to ToolboxST application
- Power failure to the I/O pack
- Terminal board **Bar Code** entered incorrectly in ToolboxST configuration
- Wrong terminal board is configured in ToolboxST application
- I/O pack or module plugged into wrong jack on terminal board, or wrong jack number in ToolboxST configuration
- I/O pack configured in ToolboxST application, but configuration not downloaded to the controller
- I/O pack in program mode

Solution

- Verify that the Ethernet cables and network switch are operating correctly.
- Verify that the I/O pack configuration (such as Type, HW Form, Bar Code, position) matches the actual hardware.
- Manually restart the I/O pack or module.
- If ToolboxST communication is working correctly, any additional diagnostics should indicate the cause of the problem.
- Build and download parameters to the I/O pack or module.
- Download firmware and parameters to the I/O pack or module.
- Build and download the configuration to the controller, wait for I/O pack communication status to change, then scan and download to the I/O pack.

Note This alarm is not reported to the WorkstationST Alarm Viewer. This alarm is generated by the ToolboxST application, not by the firmware.

21

Note This alarm is obsolete.

Description Control/Status communication failure between [ ] and controller

Possible Cause

- Asynchronous Drive Language (ADL) communication unhealthy
- Terminal board barcode typed incorrectly in the ToolboxST configuration
- Wrong terminal board is configured in the ToolboxST application
- I/O pack or module plugged into wrong jack on terminal board, or wrong jack number in ToolboxST configuration
- I/O pack or module is configured in the ToolboxST application, but configuration is not downloaded to the controller
- I/O pack or module in program mode

Solution

- Verify that the I/O pack or module configuration (such as Type, HW Form, Bar Code, position) matches the actual hardware.
- Perform a build and download the configuration to the controller, wait for pack communication status to change, then scan and download to the I/O pack or module.
- Manually restart the I/O pack or module.

22

Description ToolboxST application detects a diagnostic status signal (...L3DIAG, ATTN, and/or LINK_OK...) is [ ]; therefore, the status signal is inaccurate, unknown, or indeterminate

Possible Cause

- I/O status signal quality in warning state
- Signal quality unhealthy, forced, or being simulated
- Status information inaccurate

Solution

- Check status signal health.
- Remove the force or simulated condition applied to the status signal.

Note This alarm is not reported to the WorkstationST Alarm Viewer. This alarm is generated by the ToolboxST application, not by the firmware.

23

Description ToolboxST application detects a major difference in [ ] controller application code

Possible Cause

- Compressing variables, EGD pages, distributed I/O, or NVRAM
- Changing frame or background period
- Changing controller or network redundancy
- Changing controller platform or NTP client mode
- Changing controller host name or IP address
- Changing IONet IP address
- Adding/removing first/last linking device (PFFA), respectively
- Removing a WCBM module
- Changing from multicast to broadcast (or vice-versa) I/O communication
- Adding the first Shared I/O module or connecting the first Controller to Controller I/O variable
- Removing the last Modbus Slave point
- Disabling controller web pages
- Disabling Wind Compress Data Log
- Disabling Wind Farm Management System

Solution Rebuild the controller and download.

Note This alarm is not reported to the WorkstationST Alarm Viewer. This alarm is generated by the ToolboxST application, not by the firmware.

24

Description ToolboxST application cannot retrieve diagnostics information from I/O pack [ ]

Possible Cause

- Cannot get requested information from I/O pack or module
- Communication program failure
- I/O pack or module unable to retrieve IP address
- Terminal board **Bar Code** entered incorrectly in ToolboxST configuration
- Wrong terminal board configured in ToolboxST application
- I/O pack or module plugged into wrong jack on terminal board, or wrong jack number in ToolboxST configuration
- I/O pack or module configured in ToolboxST application, but configuration not downloaded to controller
- I/O pack or module in program mode
- I/O pack or module not able to load firmware
- Power failure to the I/O pack or module

Solution

- Verify that the I/O pack configuration (such as Type, HW Form, Bar Code, position) matches the actual hardware.
- Build and download the configuration to the controller, wait for pack communication status to change, then scan and download to the I/O pack or module.
- Manually restart the I/O pack or module.
- Check network cables for proper connection.
- Verify that the switch is functioning correctly.

Note This alarm is not reported to the WorkstationST Alarm Viewer. This alarm is generated by the ToolboxST application, not by the firmware.

25

Note This alarm is obsolete.

Description Control/Status communication Error: [ ]

Possible Cause

- Cannot get diagnostic information from I/O pack or module
- I/O pack or module not able to load firmware

Solution

- Verify that the I/O pack or module configuration is correct.
- Rebuild the application and download the firmware and application to the I/O pack or module.
- Check network cables for proper connection.
- Verify that the switch is functioning correctly.

259

Description Application Runtime Error - [ ] Frame overruns occurred

Possible Cause Overloaded processor sequencer malfunction (one or more frame overruns occurred)

Solution

For a controller, perform the following to increase the frame idle time:

- Reduce the application or increase the EGD period.
- Upgrade the controller to one with a faster processor.
- Replace the controller.

For an I/O module, perform the following:

- From the ToolboxST application, rebuild the system, then download the application and configuration to the I/O module.
- Replace the I/O module.

260

Description Application Runtime Error - [ ] Frame skips occurred

Possible Cause There is an overloaded processor or a processor malfunction. Frame number skips were detected. The frame number should incrementally increase during Controlling state.

Solution

For a controller, do the following:

- Reduce the application or increase the EGD period to reduce the processor load.
- Upgrade the controller to one with a faster processor.
- Replace the controller.

For an I/O module, do the following:

- From the ToolboxST application, rebuild the system, then download the application and configuration to the I/O module.
- Replace the I/O module.

279

Description Could not determine platform type from hardware

Possible Cause

- During commissioning/maintenance: Incorrect firmware version or hardware malfunction (firmware could not recognize host hardware type)
- During normal operation: Hardware failure

Solution

- Verify that all connectors are aligned properly and fully seated.
- Check the firmware version for compatibility with platform. If correct, replace the controller.

280

Description Platform hardware does not match configuration

Possible Cause

- During commissioning/maintenance: Platform type identified in the application configuration does not match actual hardware
- During normal operation: Hardware failure

Solution

- Fix the platform type in the ToolboxST application. From the **General** tab, select **General Properties** and **Platform**.
- Rebuild and download the application.
- If problem persists, replace the controller.

282

Description Firmware Load Error - application independent processes failed to initialize

Possible Cause Runtime malfunction. An application-independent firmware process could not be started successfully.

Solution

- Reload firmware and application and restart.
- If controller is a UCSA, try formatting and reloading the flash memory.
- If I/O pack has diagnostic: try to re-download the base load.
- Replace the controller or I/O module.

283

Description Firmware error - Internal process crashed

Possible Cause Runtime or hardware malfunction (runtime process failed).

Solution

- Reload firmware and application and restart.
- If controller is a UCSA, try formatting and reloading the flash memory.
- If this does not work, replace the controller.

292

Description Application Error - application overrunning the frame

Possible Cause Application cannot start within frame.

Solution Check application loading and reduce the amount of application code or frequency of execution. Build application and download to all controllers.

294

Description Controller CPU overtemperature, Temp [ ] °C, Threshold [ ] °C

Possible Cause

- Excessive ambient temperature
- Hardware malfunction
- Fan loss

Solution

- Check the fan (if applicable), the ambient temperature, and for the presence of dust.
- Replace the controller.

300

Description Application Code Load Failure

Possible Cause

During commissioning/maintenance:

- Invalid application configuration

During normal operation:

- Firmware or hardware malfunction

Solution

- Rebuild and download the application to all controllers.
- Reload firmware and application.
- If problem persists, replace the controller.

320

Description Process Alarm Buffers Full - controller can miss alarm transitions

Possible Cause

- Multiple alarm variables changing state too quickly to transmit all transitions
- Excessive alarms in queue (Plant-wide system failures)

Solution
During commissioning/maintenance:

- Reduce the number of alarms that can change state at the same time (filter alarm variables in the application code).

During normal operation:

- Eliminate the conditions causing excessive process alarms.

321

Description Internal Runtime error - Process Alarms not being scanned

Possible Cause Runtime malfunction: alarms not being scanned. Controller may restart on software watchdog timeout due to processor overload.

Solution

- Reload firmware and application, and restart.
- If problem persists, replace the controller.

322

Description Configuration Load error - Too many consumed EGD variables for Fault Tolerant EGD

Possible Cause Number of relevant, consumed UDH EGD variables exceeds fault tolerant EGD limitation of 1400 bytes of data.
Normal UDH EGD operation not affected; however, in the event of UDH EGD failure, some consumed variables may not be transmitted to redundant controllers over the IONet (if applicable).

Solution During commissioning/maintenance:

- Reduce the amount of relevant, consumed UDH EGD data by removing the appropriate number of variables from EGD pages.

323

Description EGD Error - Fault Tolerant EGD activated

Possible Cause EGD exchange timeout occurred on requesting controller. Redundant processor (if applicable) is unable to receive UDH EGD inputs and requested that EGD data be transferred over the IONet.

Solution

- Verify that all redundant controllers on the UDH network are receiving all expected EGD exchanges.
- Verify that all relevant devices are powered on and producing data on the network.

324

Description EGD Error - Fault Tolerant EGD data requested

Possible Cause An EGD exchange timeout occurred on the requesting controller. Redundant processor (if applicable) unable to receive UDH EGD inputs and has requested that EGD data be transferred over the IONet.

Solution

- Check UDH network and verify that all redundant controllers are receiving all expected EGD exchanges.
- Verify that all relevant devices are powered on and producing data on the network.

326

Description Communication lost from R processor

Possible Cause

- IONet or hardware malfunction
- S or T processor in redundant system lost communication with R processor
- Missing cable from the controller to the Unit Data Highway (UDH) network switch

Solution

- Go online with the R processor. Verify that the processor is in the Controlling state. If not communicating or in Controlling state, restart the processor.
- Check for disconnected IONet cables or malfunctioning switches.
- Rebuild and download the application.
- Check for a defective Ethernet cable to network switch.
- Check for a defective network switch:
  - Place the Ethernet cable into empty port.
  - If the problem persists, replace the network switch.

327

Description Communication lost from S processor

Possible Cause

- IONet or hardware malfunction
- R or T processor in redundant system lost communication with S processor
- Missing cable from the controller to the Unit Data Highway (UDH) network switch

Solution

- Go online with the S processor. Verify that the processor is in the Controlling state. If not communicating or in Controlling state, restart the processor.
- Check for disconnected IONet cables or malfunctioning switches.
- Rebuild and download the application.
- Check for a defective Ethernet cable to network switch.
- Check for a defective network switch:
  - Place the Ethernet cable into empty port.
  - If the problem persists, replace the network switch.

328

Description Communication lost from T processor

Possible Cause

- IONet or hardware malfunction
- R or S processor in redundant system lost communication with T processor
- Missing cable from the controller to the Unit Data Highway (UDH) network switch

Solution

- Go online with the T processor. Verify that the processor is in the Controlling state. If not communicating or in Controlling state, restart the processor.
- Check for disconnected IONet cables or malfunctioning switches.
- Rebuild and download the application.
- Check for a bad Ethernet cable to network switch.
- Check for a bad network switch:
  - Place the Ethernet cable into empty port.
  - If the problem persists, replace the network switch.

329

Description Startup sequence failed - Data initialization timeout R processor

Possible Cause Controller unable to complete startup data initialization

- IONet malfunction
- Controllers have different application revisions
- One or more controllers powered down
- Controller overloaded by external command messages

Solution

- Check for disconnected IONet cables or malfunctioning network switches.
- Rebuild and download the application.
- Verify that all controllers are powered on.
- Disable all other command senders (for example, Modbus masters) until controller is online.

330

Description Startup sequence failed - Data initialization timeout S processor

Possible Cause Controller is unable to complete startup data initialization.

- IONet malfunction
- Controllers have different application revisions
- One or more controllers are powered down
- Controller is overloaded by external command messages.

Solution

- Check for disconnected IONet cables or malfunctioning network switches.
- Rebuild and download application.
- Ensure all controllers are powered up.
- Disable all other command senders (for example, Modbus masters) until controller is online.

331

Description Startup sequence failed - Data initialization timeout T processor

Possible Cause Controller is unable to complete startup data initialization.

- IONet malfunction
- Controllers have different application revisions
- One or more controllers are powered down
- Controller is overloaded by external command messages

Solution

- Check for disconnected IONet cables or malfunctioning network switches.
- Rebuild and download application.
- Ensure all controllers are powered up.
- Disable all other command senders (for example, Modbus masters) until controller is online.

332

Description Overtemperature - Controller rebooted and throttled

Possible Cause

- Excessive ambient temperature
- Hardware malfunction
- Fan loss

Solution

- Check ambient temperature.
- Check for dust buildup on the cabinet filters, controller, and power supply.
- Replace the controller.
- Check fans.

334

Description Application Error – [ ] Frame Skips Detected

Possible Cause

- Hardware or IONet malfunction
- Frame number skips detected. Frame number should monotonically increase until rollover; alarm occurs following a single frame number skips in successive frames.

Solution

- Check IONet (switches, cables).
- Replace the controller.

335

Description Memory Verification Failed – Firmware Processes

Possible Cause A modification has occurred in the code segment for one of the processes. This indicates that a hardware memory failure has occurred.

Solution Replace the controller.

336

Description Controller is Unlocked

Possible Cause

- Leaving Data Init control state and not locked
- The controller is unlocked through the ToolboxST application.

Solution From ToolboxST application, lock the controllers before running safety functions.

337

Description Output exchange disagreement detected

Possible Cause IONet malfunction or hardware problem. For at least one output, a difference was detected between the controller outputs. This alarm remains active until the controllers agree on all outputs. A difference for non-Boolean data generally indicates a deviation of more than 10% from the median value or no IONet EGD configuration is present. For median values near zero, the variation exceeds integer 2 or real value 0.2.

Solution

- For the Mark VIe runtime, use the ToolboxST disagreement display (View | Disagreements) to determine which variables are in disagreement.
- In the application, avoid use of global variable 'ControllerID' and avoid the use of sequencing block 'USB_HB'.
- Check IONet (switches, cables); rebuild and download application to all processors. If the problem persists, replace the processor module.

347

Description Running Application does not match the Branded Application

Possible Cause Application not branded or different from branded version.

Note The purpose of branding is to label a verified safety application, and to ensure that it is running.

Solution

- Reload the branded application to the controller and I/O packs.
- Use the ToolboxST application to brand the currently running application.

348

Description Intermittent Communications on IONet1 – Packet Loss Exceeded [ ]%

Possible Cause

- Power cycled on I/O producer (controller or I/O module)
- Faulty Ethernet cable from I/O pack to IONet switch and/or from IONet switch to controller.
- Faulty IONet switch
- I/O message corruption
- Communication errors occurred on more than 5% of data transmissions on IONet1

Solution

- Check for evidence of I/O pack restart (diagnostic alarms, error logs).
- Replace Ethernet cable(s).
- Replace the I/O pack.
- Move the I/O pack's Ethernet cable into an empty IONet switch port. If problem persists, replace the IONet switch.

349

Description Intermittent Communications on IONet2 – Packet Loss Exceeded [ ]%

Possible Cause

- Power cycled on I/O producer (controller or I/O module)
- Faulty Ethernet cable from I/O pack to IONet switch and/or from IONet switch to controller.
- Faulty IONet switch
- I/O message corruption
- Communication errors occurred on more than 5% of data transmissions on IONet2

Solution

- Check for evidence of I/O pack restart (diagnostic alarms, error logs).
- Replace Ethernet cable(s).
- Replace the I/O pack.
- Move the I/O pack's Ethernet cable into an empty IONet switch port. If problem persists, replace the IONet switch.

350

Description Intermittent Communications on IONet3 – Packet Loss Exceeded [ ]%

Possible Cause

- Power cycled on I/O producer (controller or I/O module)
- Faulty Ethernet cable from I/O pack to IONet switch and/or from IONet switch to controller.
- Faulty IONet switch
- I/O message corruption
- Communication errors occurred on more than 5% of data transmissions on IONet3

Solution

- Check for evidence of I/O pack restart (diagnostic alarms, error logs).
- Replace Ethernet cable(s).
- Replace the I/O pack.
- Move the I/O pack's Ethernet cable into an empty IONet switch port. If problem persists, replace the IONet switch.

352

Description Memory Validation Failed – Blockware Data Structures

Possible Cause A hardware memory failure because application process data was modified (data should not change after controller goes online)

Solution Replace the controller.

353

Description Memory Validation Failed – Configuration Shared Memory

Possible Cause A hardware memory failure because system process data was modified (data should not change after controller goes online)

Solution Replace the controller.

354

Description Memory Validation Failed – IONet Data Structures

Possible Cause There is a hardware memory failure because IONet process data was modified (data should not change after the controller goes online)

Solution Replace the controller.

355

Description State Exchange Voter disagreement detected

Possible Cause

- State Exchange disagreement found
- Application sequencing error
- IONet malfunction or hardware problem

Solution

- Use the ToolboxST disagreement display (View | Disagreements) to determine which variables are in disagreement.
- In the application, avoid use of global variable 'ControllerID' and avoid the use of 'USB_HB' block.
- Check IONet (switches, cables). If problem persists, replace the processor module.

356

Description NANs detected in CALC or NAN_BREAKER block

Possible Cause

- NaN (Invalid floating point number) received from I/O interface
- Hardware problem

Solution

- Check for external devices that may be sending NaNs to the controller.
- If conditions persists, replace the controller.

357

Description Internal Runtime error - Sequencer out-of-order or overrun detected

Possible Cause There is a possible hardware malfunction. Sequencer critical clients were scheduled out of order or were overrun. This alarm occurs following three successive frames of sequencer critical client out-of-order detections. After five, the controller is put into the FAILURE control state.

Solution Replace the controller.

358

Description Internal Runtime error - Sequencer client execution underrun

Possible Cause Possible hardware malfunction. Sequencer critical client underrun detected. Alarm occurs after a sequencer critical client has been run slower than its nominal rate three times in a row; after five, controller put in FAILURE control state.

Solution

- Ignore this alarm if it occurs during a restart of the controller.
- If the alarm occurs during normal operation, then replace the controller.

359

Description Internal Runtime error - Sequencer client execution overrun

Possible Cause Possible hardware malfunction. Sequencer critical client overrun detected. Alarm occurs after a sequencer critical client has been run faster than its nominal rate three times in a row; after five, controller put in FAILURE control state.

Solution

- Ignore alarm if it occurs during a restart of the controller.
- Replace the controller, if the alarm occurs during normal operation.

360

Description Internal Runtime error - Sequencer frame period out-of-bounds (±15%)

Possible Cause Possible hardware malfunction. Frame period greater than ±15% of nominal. Alarm occurs following frame period out-of-bounds condition occurring three frames in a row; after five, controller put in FAILURE control state.

Solution

- Ignore alarm if it occurs during a restart of the controller.
- Replace the controller, if the alarm occurs during normal operation.

361

Description Internal Runtime error - Sequencer frame state timeout out-of-bounds (±15%)

Possible Cause Possible hardware malfunction. Sequencer frame state timeout greater than ±15% of nominal. Alarm occurs following a sequencer frame state timeout being out-of-bounds three frames in row; after five, controller put in FAILURE control state.

Solution

- Ignore alarm if it occurs during a restart of the controller.
- Replace the controller, if the alarm occurs during normal operation.

362

Description Internal Runtime error - Sequencer frame number skip detected

Possible Cause Possible hardware or IONet malfunction. Frame number skips detected. Frame number should monotonically increase until rollover; alarm occurs following three skips in a row, after five, controller put in FAILURE control state.

Solution

- Ignore this alarm if it occurs during a restart of the controller.

During normal operation:

- Check for hardware or network switch malfunction.
- Check for loose or defective network cables.
- Replace the controller.

363

Description Memory Validation failed - Sequencer data structures

Possible Cause Hardware memory failure. Sequencer process data was modified (data should not change after the controller is online).

Solution Replace the controller.

364

Description Too many state voter disagreements detected

Possible Cause

- State exchange voter disagreement overflow. System exceeded the limit of 128 simultaneous disagreements at once.
- Application error
- Hardware problem or IONet malfunction

Solution

- Use the ToolboxST disagreement display (View | Disagreements) to determine which variables are in disagreement.
- In the application, avoid use of global variable 'ControllerID' and avoid the use of 'USB_HB' block.
- Check IONet (switches, cables).
- If problem persists, replace the controller.

374

Description Invalid Calibration Settings

Possible Cause

- Calibration file not detected
- Calibration file corrupted
- Calibration constants invalid
- Hardware Failure

Solution Replace the module.

375

Description Controller has entered Quality Control (QC) Mode

Possible Cause The device has received a command to enter factory QC mode.

Solution Reboot the device.

462

Description Hardware Reconfigured: Reboot by removing and reapplying power

Possible Cause Flash memory file system corruption.

Solution

- After reapplying power, Rebuild and download baseload, firmware and application.
- If the problem persists, replace the controller.

463

Description Internal runtime error - Could not create the Command and Event Log (CEL) file

Possible Cause Internal runtime error. Could not create the CEL file.

Solution

- Rebuild and download baseload, firmware, and application to the controller.
- If the problem persists, replace the controller.

464

Description Ethernet Interface [ ] disabled due to excessive traffic

Possible Cause Network interface has been disabled to protect itself from excessive activity on the network.

Solution

- Check for network loops.
- Monitor network activity and remove excessive traffic.

465

Description Ethernet Interface [ ] disabled due to excessive traffic

Possible Cause Network interface has been disabled to protect itself from excessive activity on the network

Solution

- Check for network loops.
- Monitor network activity and remove excessive traffic.

466

Description Ethernet Interface [ ] disabled due to excessive traffic

Possible Cause Network interface has been disabled to protect itself from excessive activity on the network

Solution

- Check for network loops.
- Monitor network activity and remove excessive traffic.

467

Description Ethernet Interface [ ] disabled due to excessive traffic

Possible Cause Network interface has been disabled to protect itself from excessive activity on the network.

Solution

- Check for network loops.
- Monitor network activity and remove excessive traffic.

468

Description Ethernet Interface [ ] disabled due to excessive traffic

Possible Cause Network interface has been disabled to protect itself from excessive activity on the network.

Solution

- Check for network loops.
- Monitor network activity and remove excessive traffic.

469

Description UDH EGD fault detected by the R processor

Possible Cause

- UDH EGD producer is powered down
- Producer is unhealthy
- Ethernet connection(s) failure

Solution

- Ensure all EGD producers are powered on and healthy.
- Check for a defective Ethernet cable from producer to network switch. Replace the cable(s).
- Check for a defective network switch by placing the producer's Ethernet cable into an empty port. If the problem persists, replace the network switch.
- Replace the processor module.

470

Description UDH EGD fault detected by the S processor

Possible Cause

- UDH EGD producer is powered down
- Producer is unhealthy
- Ethernet connection(s) failure

Solution

- Ensure all EGD producers are powered up and healthy.
- Check for a defective Ethernet cable from producer to network switch. Replace the cable(s).
- Check for a defective network switch by placing the producer's Ethernet cable into an empty port. If the problem persists, replace the network switch.
- Replace the producer processor module.

471

Description UDH EGD fault detected by the T processor

Possible Cause

- UDH EGD producer is powered down
- Producer is unhealthy
- Ethernet connection(s) failure

Solution

- Ensure all EGD producers are powered up and healthy.
- Check for a defective Ethernet cable from producer to network switch. Replace the cable(s).
- Check for a defective network switch by placing the producer's Ethernet cable into an empty port. If the problem persists, replace the network switch.
- Replace the producer processor module.

486

Description Auto-Reconfiguration server installation is incomplete

Possible Cause

- A download from the ToolboxST application to an I/O pack and/or the Auto-Reconfiguration server has failed
- Not all of the I/O packs were selected for download

Solution Perform a scan and download using the ToolboxST application.

487

Description Auto-Reconfiguration server failed scanning or downloading an I/O pack

Possible Cause At least one I/O pack is in an unexpected state that the Auto-Reconfiguration server is unable to handle

Solution

- Cycle power on the I/O pack.
- Perform a scan and download using the ToolboxST application.
- Replace the I/O pack.

488

Description EGD Error - Could not configure consumed exchanges from one or more Producers

Possible Cause

- Producer EGD Page(s) configured incorrectly
- Producer(s) powered down
- Network connectivity intermittent or severed
- Internal Firmware failure

Solution

- Rectify configuration error. Compress all pages and download application to Producer.
- Ensure each Producer is powered on and in the Controlling state.
- Refer to the Network Troubleshooting guide for possible solutions.
- Replace the Consumer and/or Producer hardware.

489

Description EGD Error - One or more consumed exchanges contain unbound variables

Possible Cause

- An EGD variable has been removed from a Producer's EGD configuration
- An EGD variable has been added to a different Producer's EGD Page from its original EGD Page

Solution

- Add the offending variable to the Producer's EGD configuration, compress the Page and download the application to the Producer.
- Remove the reference to the offending variable from the Consumer's application code; build and download application to the Consumer.
- Compress the EGD Page in the Producer where the variable has been added; build and download the application to the Producer.

490

Description Software watchdog has been disabled

Possible Cause

- A runtime malfunction has disabled the software watchdog protective function
- An invalid version of firmware has been downloaded

Solution

- Reload base load, firmware, and application and restart.
- If using a UCSA, reformat the flash and reload the firmware.
- I/O pack or module: re-download the base load.
- If this does not work, replace the controller or I/O module.

491

Description Hardware watchdog has been disabled

Possible Cause

- A runtime malfunction has disabled the hardware watchdog protective function
- A hardware failure has disabled the hardware watchdog protective function

Solution

- Reload firmware and restart.
- If problem persists, replace hardware.

493

Description CDH EGD fault detected by the R processor

Possible Cause

- CDH EGD producer is powered down
- Producer is unhealthy
- Ethernet connection(s) failure

Solution

- Ensure all EGD producers are powered up and healthy.
- Check for a defective Ethernet cable from producer to network switch. Replace the cable(s).
- Check for a defective network switch by placing the producer's Ethernet cable into an empty port. If the problem persists, replace the network switch.
- Replace the producer processor module.

494

Description CDH EGD fault detected by the S processor

Possible Cause

- CDH EGD producer is powered down
- Producer is unhealthy
- Ethernet connection(s) failure

Solution

- Ensure all EGD producers are powered up and healthy.
- Check for a defective Ethernet cable from producer to network switch. Replace the cable(s).
- Check for a defective network switch by placing the producer's Ethernet cable into an empty port. If the problem persists, replace the network switch.
- Replace the producer processor module.

495

Description CDH EGD fault detected by the T processor

Possible Cause

- CDH EGD producer is powered down
- Producer is unhealthy
- Ethernet connection(s) failure

Solution

- Ensure all EGD producers are powered up and healthy.
- Check for a defective Ethernet cable from producer to network switch. Replace the cable(s).
- Check for a defective network switch by placing the producer's Ethernet cable into an empty port. If the problem persists, replace the network switch.
- Replace the producer processor module.

496

Description Failed to incorporate the user-configured frame state timeouts

Possible Cause

- Invalid user-configured frame state timeout values
- Failed to parse the user-configured frame state timeouts file

Solution

- Timeout values configured by the user must satisfy the condition *Frame Rate > Output Timeout > App Timeout > Input Timeout > 0.*
- Rebuild the application and force an offline download of the application to the controller.

497-498

Description Fan loss detected for controller fan [ ]

Possible Cause

- Hardware malfunction
- Fan power not applied

Solution

- Check the fan.
- Verify that the power connector is properly inserted.
- Replace the fan.

501

Description Total memory consumption has exceeded [ ] percent

Possible Cause Memory usage is driven from three functions:

- The online download procedure temporarily stores the previous and new application configuration in memory.
- The footprint of the application configuration/code has been enlarged.
- Memory usage can grow over time if there is a memory leak.

Solution

- The alarm should return to normal state after download is complete.
- Reduce the content of the application configuration/code.
- To address a memory leak, reboot the device to reinitialize baseline memory use. Monitor for reoccurrence and contact your GE representative.

502

Description Syspage inconsistency detected

Possible Cause Memory corruption

Solution Restart the controller to re-initialize QNX syspage.

503

Description Communications timeout with Remote System Log Server

Possible Cause

- Remote Syslog server not in network
- Remote Syslog server down
- Incorrect Remote Syslog server IP address in system configuration
- Network issue (cables/switch) connecting controller to Remote Syslog server

Solution

- Verify that the Remote Syslog server is in operation.
- Verify that the correct Remote Syslog server IP address in the system configuration.
- Check the network connections.

504

Description Unauthorized executable was detected and terminated

Possible Cause When in Secure mode, the controller only permits authorized executables. An unauthorized executable has been detected and dismissed.

Solution

- Inspect the syslog/error log messages
- Rebuild and download the baseload, firmware, and application to the controller.
- Re-install the ControlST application, then rebuild and download the baseload, firmware, and application to the controller.

505

Description R network shared I/O module inputs unhealthy

Possible Cause

- I/O module restarting or restarted
- I/O module application/configuration missing
- Application/configuration does not match in I/O module and controller
- Failed Ethernet connection between I/O module and controller
- Ethernet cable inserted into wrong connector on I/O module

Note When using the Shared IONet feature, this alarm is generated if there is a problem with receiving inputs from any shared I/O module on the R IONet. Refer to *Mark Controllers Shared IONet User Guide* (GEH-6812).

Solution

- Rebuild and download application/parameters to all controllers and I/O modules.
- Reload firmware and parameters to the affected I/O module.
- Reload firmware and application to all controllers.
- If the problem persists, replace the affected I/O module, then replace the controller.

506

Description S network shared I/O module inputs unhealthy

Possible Cause

- I/O module restarting or restarted
- I/O module application/configuration missing
- Application/configuration does not match in I/O module and controller
- Failed Ethernet connection between I/O module and controller
- Ethernet cable inserted into wrong connector on I/O module

Note When using the Shared IONet feature, this alarm is generated if there is a problem with receiving inputs from any shared I/O module on the S IONet. Refer to *Mark Controllers Shared IONet User Guide* (GEH-6812).

Solution

- Rebuild and download application/parameters to all controllers and I/O modules.
- Reload firmware and parameters to the affected I/O module.
- Reload firmware and application to all controllers.
- If the problem persists, replace the affected I/O module, then replace the controller.

507

Description T network shared I/O module inputs unhealthy

Possible Cause

- I/O module restarting or restarted
- I/O module application/configuration missing
- Application/configuration does not match in I/O module and controller
- Failed Ethernet connection between I/O module and controller
- Ethernet cable inserted into wrong connector on I/O module

Note When using the Shared IONet feature, this alarm is generated if there is a problem with receiving inputs from any shared I/O module on the T IONet. Refer to *Mark Controllers Shared IONet User Guide* (GEH-6812).

Solution

- Rebuild and download application/parameters to all controllers and I/O modules.
- Reload firmware and parameters to the affected I/O module.
- Reload firmware and application to all controllers.
- If the problem persists, replace the affected I/O module, then replace the controller.

508

Description Application mismatch between redundant controllers

Possible Cause

- One processor installed new application code while the other processor(s) did not
- Processor was replaced and application code was built with a different version of the ToolboxST application

Solution

- Rebuild and download the application code to all controllers.
- Verify that the *Application Code* checkbox is selected in the download wizard for all controllers prior to downloading.

509

Description Controller certificate has been revoked

Possible Cause

- Controller certificate is in the Certificate Revocation List (CRL)
- Certificate Authority (CA) Administrator revoked the certificate

Solution

- Transition the controller from Secure to Open state then back to Secure to generate a new certificate and private key.
- Contact the Certificate Authority (CA) Administrator.

510

Description Controller certificate will expire within 30 days

Possible Cause Controller certificate will expire within 30 days

Solution

- Transition the controller from Secure to Open state then back to Secure to generate a new certificate and private key.
- Contact the Certificate Authority (CA) Administrator.

511

Description Controller certificate will expire within seven days

Possible Cause Controller certificate will expire within seven days

Solution

- Transition the controller from Secure to Open state then back to Secure to generate a new certificate and private key.
- Contact the Certificate Authority (CA) Administrator.

512

Description Controller certificate will expire in one day

Possible Cause Controller certificate will expire in one day

Solution

- Transition the controller from Secure to Open state then back to Secure to generate a new certificate and private key.
- Contact the Certificate Authority (CA) Administrator.

513

Description Controller certificate has expired; controller is no longer in Secure state

Possible Cause

- Controller is not in Secure state
- Controller certificate has expired

Solution

- Place the controller in the Secure state.
- Contact the Certificate Authority (CA) Administrator.

514-537

Description Controller To Controller (C2C) Inputs Unhealthy on IONet [ ] from ControlSet [ ]

Possible Cause

- Failed Ethernet connection between controllers
- Ethernet cable is inserted into the wrong connector on the IONet switch
- Controller to Controller (C2C) packet production is restarting or not occurring
- Application or configuration is missing in the controller or does not match in both controllers

Note A control set is a controller in a shared IONet group. There are 24 Controller to Controller (C2C) diagnostic alarms assigned for eight control sets. Each control set contains three diagnostics for its IONets.

Solution

- Check for Ethernet connectivity between the controllers.
- Rebuild and download the application to all controllers.
- Reload the firmware and application to all controllers.
- If the problem persists, replace the affected switch and Ethernet cables, then replace the controller.

538

Description Certificate Authority (CA) certificate will expire within 30 days

Possible Cause CA certificate will expire within 30 days

Solution Contact the CA Administrator.

539

Description Certificate Authority (CA) certificate will expire within seven days

Possible Cause CA certificate will expire within seven days

Solution Contact the CA Administrator.

540

Description Certificate Authority (CA) certificate will expire within one day

Possible Cause CA certificate will expire within one day

Solution Contact the CA Administrator.

541

Description Certificate Authority (CA) certificate has expired; controller is no longer in Secure state

Possible Cause CA certificate has expired

Solution Contact the CA Administrator.

542

Description Certificate Revocation List (CRL) has expired

Possible Cause CRL has expired

Solution

1. Contact the CA Administrator and request/confirm the renewal of the CRL.
2. After the CRL is renewed, from the Mark VIe Device menu select View | Diagnostics | Controller Advanced Diagnostics.
3. Expand the **Commands** tree, expand the **Diagnostics** tree, and double-click **Get CRL for controller from CA Server**.
4. Confirm the reply, **CRL received successfully**, which indicates that the Mark VIe to CA Server connection is healthy.
5. Close the Advanced Diagnostics Commands window.

543

Description Total memory consumption has exceeded [ ] percent

Possible Cause

- Memory leak
- Application code is too large

Solution

- Decrease memory usage.
- Restart the controller.

544

Description Communications error with Certificate Authority Server

Possible Cause

- Certificate Authority (CA) server not in network or not in operation (server is down)
- Incorrect CA server IP address in system configuration
- Network issue (cables/switch) connecting controller to CA server

Solution

- Verify that the CA server is in operation.
- Verify that the CA server IP address is correct in the system configuration.
- Check the network connections.

545

Description Active PFFA diagnostics detected

Possible Cause At least one configured PFFA module contains an active diagnostic. Since each controller within a control set monitors the diagnostic conditions of PFFA modules and connected Fieldbus devices, PFFA diagnostics may differ between the individual controllers.

Solution

- If there are active PFFA diagnostics in the WorkstationST Alarm Viewer, correct those issues.
- If there are no active PFFA diagnostics in the Alarm Viewer, go online specifically to the controller with this 545 diagnostic using the ToolboxST application. From the Component Editor Hardware tab, select the PFFA with active diagnostics, and correct the identified issues.

546

Description This component is or has been in factory test mode.

Possible Cause The controller or I/O pack has received the command to enter factory test mode.

Solution Reboot the I/O pack or controller.

547

Description Default user password detected

Possible Cause The controller password is the default value.

Solution From the ToolboxST application, set the password.

Note It is the user’s responsibility to change the default password to a unique password. If you do not know the default password, contact the nearest GE Sales or Service Office, or an authorized GE Sales Representative.

To change the controller password, refer to the *ToolboxST User Guide for Mark Controls Platform (GEH-6703)*, the section *Controller Password Change*.

1000-2024

Description Inputs unhealthy on IO Module [ ], R pack IONet [ ] - Message Timeout

Possible Cause

- I/O pack restarting or restarted
- I/O pack application/configuration is missing
- Application/configuration does not match in the I/O pack and controller
- Failed Ethernet connection between I/O pack and controller
- Ethernet cable inserted into wrong connector on I/O pack

Solution

- Reset all diagnostic alarms.
- Rebuild and download application to all controllers and I/O packs.
- Reload firmware and application.
- Verify that Ethernet cable on I/O pack matches the ToolboxST configuration.
- Check for faulty Ethernet cable from pack to network switch and/or from switch to controller. Replace cable(s) if necessary.
- Replace the I/O pack.
- Defective network switch, place I/O pack's Ethernet cable into empty port. If problem persists, replace network switch.

1000-2024

Description Inputs unhealthy on IO Module [ ], S pack IONet [ ] - Message Timeout

Possible Cause

- I/O pack restarting or restarted
- I/O pack application/configuration is missing
- Application/configuration does not match in the I/O pack and controller
- Failed Ethernet connection between I/O pack and controller
- Ethernet cable inserted into wrong connector on I/O pack

Solution

- Reset all diagnostic alarms.
- Rebuild and download application to all controllers and I/O packs.
- Reload firmware and application.
- Verify that Ethernet cable on I/O pack matches the ToolboxST configuration.
- Check for faulty Ethernet cable from I/O pack to network switch and/or from switch to controller. Replace cable(s) if necessary.
- Replace the I/O pack.
- Defective network switch, place I/O pack's Ethernet cable into empty port. If problem persists, replace network switch.

1000-2024

Description Inputs unhealthy on IO Module [ ], T pack IONet [ ] - Message Timeout

Possible Cause

- Pack restarting or restarted
- I/O pack application/configuration is missing
- Application/configuration does not match in the I/O pack and controller
- Failed Ethernet connection between I/O pack and controller
- Ethernet cable inserted into wrong connector on I/O pack

Solution

- Reset all diagnostic alarms.
- Rebuild and download application to all controllers and I/O packs.
- Reload firmware and application.
- Verify that Ethernet cable on I/O pack matches the ToolboxST configuration.
- Check for faulty Ethernet cable from I/O pack to network switch and/or from switch to controller. Replace cable(s) if necessary.
- Replace the I/O pack.
- Defective network switch, place I/O pack's Ethernet cable into empty port. If problem persists, replace network switch.

1000-2024

Description Inputs unhealthy on IO Module [ ], IONet [ ] - Message Timeout

Possible Cause

- I/O pack restarting or restarted
- I/O pack application/configuration is missing
- Application/configuration does not match in the I/O pack and controller
- Failed Ethernet connection between I/O pack and controller
- Ethernet cable inserted into wrong connector on I/O pack

Solution

- Reset all diagnostic alarms.
- Rebuild and download application to all controllers and I/O packs.
- Reload firmware and application.
- Verify that Ethernet cable on I/O pack matches the ToolboxST configuration.
- Check for faulty Ethernet cable from I/O pack to network switch and/or from switch to controller. Replace cable(s) if necessary.
- Replace the I/O pack.
- Defective network switch, place I/O pack's Ethernet cable into empty port. If problem persists, replace network switch.

1000-2024

Description Inputs unhealthy on IO Module [ ], R pack IONet [ ] - Message Length not valid

Possible Cause Application/configuration does not match in the I/O pack and controller.

Solution

- Rebuild and download application/parameters to all controllers and I/O packs.
- Reload firmware and parameters to the affected I/O pack.
- Reload firmware and application to all controllers.
- If problem persists, replace affected I/O pack, then replace controller.

1000-2024

Description Inputs unhealthy on IO Module [ ], S pack IONet [ ] - Message Length not valid

Possible Cause Application/configuration does not match in the I/O pack and controller.

Solution

- Rebuild and download application/parameters to all controllers and I/O packs.
- Reload firmware and parameters to the affected I/O pack.
- Reload firmware and application to all controllers.
- If problem persists, replace affected I/O pack, then replace controller.

1000-2024

Description Inputs unhealthy on IO Module [ ], T pack IONet [ ] - Message Length not valid

Possible Cause Application/configuration does not match in the I/O pack and controller.

Solution

- Rebuild and download application/parameters to all controllers and I/O packs.
- Reload firmware and parameters to the affected I/O pack.
- Reload firmware and application to all controllers.
- If problem persists, replace affected I/O pack, then replace controller.

1000-2024

Description Inputs unhealthy on IO Module [ ], IONet [ ] - Message Length not valid

Possible Cause Application/configuration does not match in the I/O pack and controller.

Solution

- Rebuild and download application/parameters to all controllers and I/O packs.
- Reload firmware and parameters to the affected I/O pack.
- Reload firmware and application to all controllers.
- If problem persists, replace affected I/O pack, then replace controller.

1000-2024

Description Inputs unhealthy on IO Module [ ], R Pack IONet [ ] - Major Signature Mismatch

Possible Cause Application/configuration does not match in the I/O pack and controller.

Solution

- Rebuild and download application/parameters to all controllers and I/O packs.
- Reload firmware and parameters to the affected I/O pack.
- Reload firmware and application to all controllers.
- If problem persists, replace affected I/O pack, then replace controller.

1000-2024

Description Inputs unhealthy on IO Module [ ], S Pack IONet [ ] - Major Signature Mismatch

Possible Cause Application/configuration does not match in the I/O pack and controller.

Solution

- Rebuild and download application/parameters to all controllers and I/O packs.
- Reload firmware and parameters to the affected I/O pack.
- Reload firmware and application to all controllers.
- If problem persists, replace affected I/O pack, then replace controller.

1000-2024

Description Inputs unhealthy on IO Module [ ], T Pack IONet [ ] - Major Signature Mismatch

Possible Cause Application/configuration does not match in the I/O pack and controller.

Solution

- Rebuild and download application/parameters to all controllers and I/O packs.
- Reload firmware and parameters to the affected I/O pack.
- Reload firmware and application to all controllers.
- If problem persists, replace affected I/O pack, then replace controller.

1000-2024

Description Inputs unhealthy on IO Module [ ] IONet [ ] - Major Signature Mismatch

Possible Cause Application/configuration does not match in the I/O pack and controller.

Solution

- Rebuild and download application/parameters to all controllers and I/O packs.
- Reload firmware and parameters to the affected I/O pack.
- Reload firmware and application to all controllers.
- If problem persists, replace affected I/O pack, then replace controller.

1000-2024

Description Inputs unhealthy on IO Module [ ], R Pack IONet [ ] - Minor Signature Mismatch

Possible Cause Application/configuration does not match in the I/O pack and controller.

Solution

- Rebuild and download application/parameters to all controllers and I/O packs.
- Reload firmware and parameters to the affected I/O pack.
- Reload firmware and application to all controllers.
- If problem persists, replace affected I/O pack, then replace controller.

1000-2024

Description Inputs unhealthy on IO Module [ ], S Pack IONet [ ] - Minor Signature Mismatch

Possible Cause Application/configuration does not match in the I/O pack and controller.

Solution

- Rebuild and download application/parameters to all controllers and I/O packs.
- Reload firmware and parameters to the affected I/O pack.
- Reload firmware and application to all controllers.
- If problem persists, replace affected I/O pack, then replace controller.

1000-2024

Description Inputs unhealthy on IO Module [ ], T Pack IONet [ ] - Minor Signature Mismatch

Possible Cause Application/configuration does not match in the I/O pack and controller.

Solution

- Rebuild and download application/parameters to all controllers and I/O packs.
- Reload firmware and parameters to the affected I/O pack.
- Reload firmware and application to all controllers.
- If problem persists, replace affected I/O pack, then replace controller.

1000-2024

Description Inputs unhealthy on IO Module [ ] IONet [ ] - Minor Signature Mismatch

Possible Cause Application/configuration does not match in the I/O pack and controller.

Solution

- Rebuild and download application/parameters to all controllers and I/O packs.
- Reload firmware and parameters to the affected I/O pack.
- Reload firmware and application to all controllers.
- If problem persists, replace affected I/O pack, then replace controller.

1000-2024

Description Inputs unhealthy on IO Module [ ], R Pack IONet [ ] - Timestamp Mismatch

Possible Cause Application/configuration does not match in the I/O pack and controller.

Solution

- Rebuild and download application/parameters to all controllers and I/O packs.
- Reload firmware and parameters to the affected I/O pack.
- Reload firmware and application to all controllers.
- If problem persists, replace affected I/O pack, then replace controller.

1000-2024

Description Inputs unhealthy on IO Module [ ], S Pack IONet [ ] - Timestamp Mismatch

Possible Cause Application/configuration does not match in the I/O pack and controller.

Solution

- Rebuild and download application/parameters to all controllers and I/O packs.
- Reload firmware and parameters to the affected I/O pack.
- Reload firmware and application to all controllers.
- If problem persists, replace affected I/O pack, then replace controller.

1000-2024

Description Inputs unhealthy on IO Module [ ], T Pack IONet [ ] - Timestamp Mismatch

Possible Cause Application/configuration does not match in the I/O pack and controller.

Solution

- Rebuild and download application/parameters to all controllers and I/O packs.
- Reload firmware and parameters to the affected I/O pack.
- Reload firmware and application to all controllers.
- If problem persists, Immediate Attention Required: Fieldbus I/O Module [ ] Not Detected on IoNet [ ]ts, replace affected I/O pack, then replace controller.

1000-2024

Description Inputs unhealthy on IO Module [ ] IONet [ ] - Timestamp Mismatch

Possible Cause Application/configuration does not match in the I/O pack and controller.

Solution

- Rebuild and download application/parameters to all controllers and I/O packs.
- Reload firmware and parameters to the affected I/O pack.
- Reload firmware and application to all controllers.
- If problem persists, replace affected I/O pack, then replace controller.

1000-2024

Description Inputs unhealthy on IO Module [ ] IONet [ ] - Message Timeout

Possible Cause Application/configuration does not match in the I/O pack and controller.

Solution

- Rebuild and download application/parameters to all controllers and I/O packs.
- Reload firmware and parameters to the affected I/O pack.
- Reload firmware and application to all controllers.
- If problem persists, replace affected I/O pack, then replace controller.

1000-2024

Description Immediate Attention Required: Fieldbus I/O Module [ ] Not Detected on IoNet [ ]

Possible Cause Note: If this diagnostic is active, the module needs to be replaced immediately. If it is simplex, the devices under this PFFA have lost communication. If it is redundant and not replaced, and a controller on the remaining module's IONet goes down, then control is lost for all devices under the PFFA modules.

- PFFA module did not complete Start
- PFFA module configuration files missing
- PFFA module restarted
- PFFA module configured for Hot Backup, but only one network is connected
- Serial connection between PFFA modules is broken
- Network issue

Solution

- If the Control/Status communication is working correctly, any additional diagnostics should indicate the cause of the problem.
- Build and download parameters to the PFFA module and controller.
- Verify Serial cable is attached correctly.
- Verify that the Ethernet cables and network switch are operating correctly.
- Manually restart the PFFA module.

2400

Description EtherCAT scan bus error

Possible Cause

- EtherCAT device(s) is unplugged or without power
- An Ethernet cable is disconnected or damaged
- Redundancy mode is not set correctly
- Redundant Ring is broken

Solution

- Ensure all devices are connected and powered.
- Verify all Ethernet LINK lights are lit.
- Verify redundant configuration is correct.

2401

Description EtherCAT All Ethernet links disconnected

Possible Cause

- Ethernet LINK between Mark VIe controller and EtherCAT network is lost
- EtherCAT device(s) are unplugged or without power

Solution

- Reconnect Ethernet cables.
- Verify all Ethernet LINK lights are lit.
- Verify all EtherCAT devices are powered.

2402

Description EtherCAT linebreak detected between devices [ ] and [ ]

Possible Cause

- An Ethernet cable is disconnected or damaged
- EtherCAT device(s) is unplugged or without power

Solution

- Reconnect Ethernet cables.
- Verify all Ethernet LINK lights are lit.
- Verify all EtherCAT devices are powered.

2404

Description EtherCAT limit for lost frames has been exceeded

Possible Cause

- A device or network component is corrupting the EtherCAT frame
- An Ethernet cable is damaged

Solution Use Controller Advanced Diagnostic tool to determine where network issues are located in the device topology.

2405

Description EtherCAT device disconnected

Possible Cause

- EtherCAT device(s) is unplugged or without power
- An Ethernet cable is disconnected or damaged

Solution

- Ensure all devices are connected and powered.
- Verify all Ethernet LINK lights are lit.

2406

Description EtherCAT device in unexpected state

Possible Cause EtherCAT device(s) have invalid configuration or have experienced a watchdog event.

Solution Check the EtherCAT device configuration in the ENI file and EtherCAT Configuration Tool.

2407

Description EtherCAT Master in unexpected state

Possible Cause Bus does not match ENI file.

Solution Download a new ENI file or plug in all devices.

2408

Description EtherCAT ENI file does not match bus configuration

Possible Cause ENI File imported in ToolboxST does not match the discovered network.

Solution

- Verify ENI file matches the network connected to the Mark VIe controller.
- Verify EtherCAT network is connected and intact.

2409

Description EtherCAT redundant Ethernet links crossed

Possible Cause Main and Redundant Ethernet links are swapped on the controller.

Solution Switch the EtherCAT Network connections on the controller.

2410

Description EtherCAT configuration is not supported

Possible Cause

- The ENI file contains unsupported commands or features
- The ENI file contains commands that are unsupported in redundancy

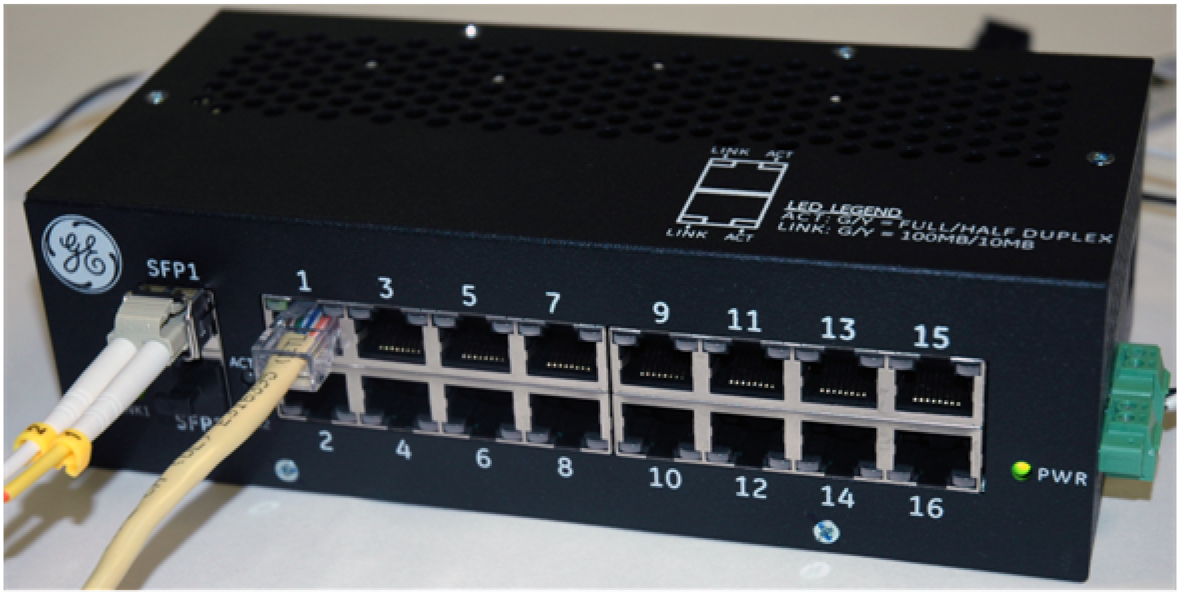
Solution

- Remove unsupported commands or disable unsupported features.
- In redundant operation, replace LRW commands with LRD / LWR.

1.14 ESWA and ESWB Industrial Unmanaged Ethernet Switches

GE's product line of industrial unmanaged Ethernet 10/100 switches, ESWA and ESW, are specifically designed to meet the needs of real-time industrial control solutions. To meet the requirements for speed and functionality, the following features are provided:

- 802.3, 802.3u, and 802.3x compatibility
- 10/100 base copper with auto negotiation
- Full/half duplex auto-negotiation
- 100 Mbps FX uplink port
- HP-MDIX auto sensing
- LEDs for Link Presence, Activity and Duplex, and Speed per port (each LED has two colors)
- LED for Power
- Minimum 256 KB buffer with 4K media access control (MAC) addresses



1.14.1 Available Form Factors

The ESWx switch is available in the following form factors:

Part #	Description
IS420ESWAH1A	8 ports 10/100BASE-TX + 1 port 100BASE-FX LC-type connection
IS420ESWAH2A	8 ports 10/100BASE-TX + 2 ports 100BASE-FX LC-type connection
IS420ESWAH3A	8 ports 10/100BASE-TX
IS420ESWAH4A	8 ports 10/100BASE-TX + 1 port 100BASE-LX10 LC-type connection
IS420ESWAH5A	8 ports 10/100BASE-TX + 2 ports 100BASE-LX10 LC-type connection
IS420ESWBH1A	16 ports 10/100BASE-TX + 1 port 100BASE-FX LC-type connection
IS420ESWBH2A	16 ports 10/100BASE-TX + 2 ports 100BASE-FX LC-type connection
IS420ESWBH3A	16 ports 10/100BASE-TX
IS420ESWBH4A	16 ports 10/100BASE-TX + 1 port 100BASE-LX10 LC-type connection
IS420ESWBH5A	16 ports 10/100BASE-TX + 2 ports 100BASE-LX10 LC-type connection

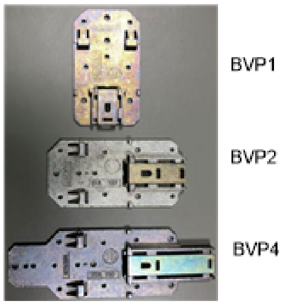
1.14.2 Installation

For new installations, mount the switch or switches onto the control system panel(s) using a DIN-rail. Connect the copper and/or fiber cables in accordance with system requirements and redundancy. Connect the 28 V dc power from the power distribution board to the switch.

Note For system requirements, redundancy, and other related information, refer to the *Mark VIe and Mark VIeS Control System Volume I: System Guide* (GEH-6721_Vol_I), the chapter *Ethernet Networks*.

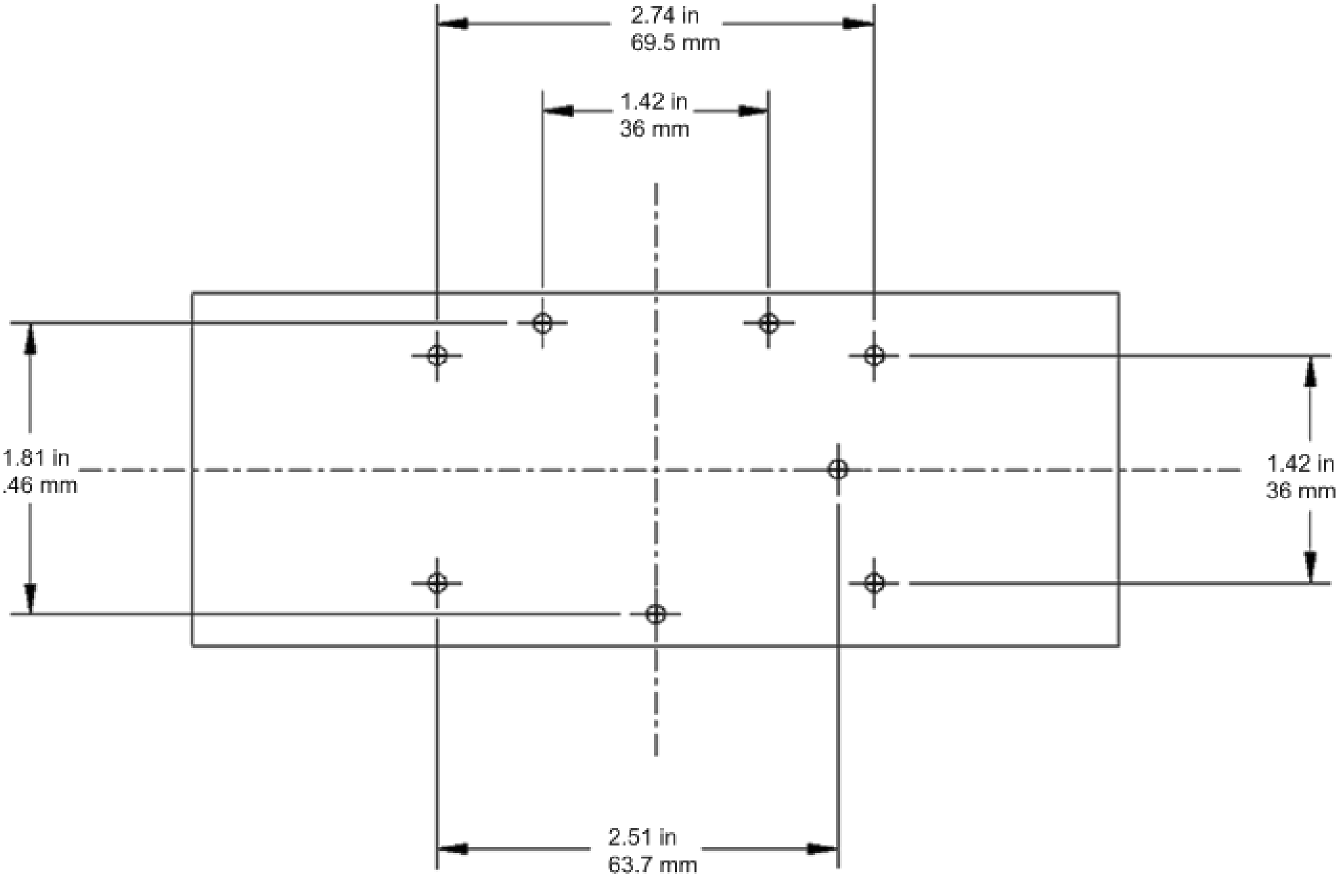
GE has qualified the following DIN-rail clips for use with the ESWx switches.

Clip Part #	Switch Usage	Mounting Orientation
259B2451BVP1	ESWA (8-port) or ESWB (16-port)	Long edge of switch body parallel to rail
259B2451BVP2	ESWA (8-port)	Long edge of switch body perpendicular to rail
259B2451BVP4	ESWB (16-port)	Long edge of switch body perpendicular to rail



1.14.2.1 Replacement for Third-party Switch

When the ESWA or ESWB is used to replace a different unmanaged switch, it uses the existing mounting brackets, which can either be panel or DIN rail mounts. There are seven screw holes used on the existing switch to support panel mounting. The following drawing displays the pattern and dimensions for these holes.



Holes to Support Panel Mounting

Switches in existing cabinets already have cables with appropriate lengths for the existing switch box. The replacement switch allows for no more than three inches of slack in the existing wiring. The mechanical location of the ports allows the replacement in an existing cabinet.

Third-party Switch to GE Switch Replacement Matrix

Third-party Switch to be Replaced	# Copper Ports	# Multi-mode Fiber Ports	# Single-mode Fiber Ports	New Compatible GE Switch	
336A4940DNP508TX	8	0	—	ESWA	H3A
336A4940DNP509FX	8	1	—	ESWA	H1A
336A4940DNP516TX	16	0	—	ESWB	H3A
336A4940DNP517FX	16	1	—	ESWB	H1A
336A4940DNP508FX2	6	2	—	ESWA	H2A
336A4940DNP508FXE2	6	—	2	ESWA	H4A
336A4940DNP509FXWTB	8	1	—	ESWA	H1A
336A4940DNP508TXWHB	8	0	—	ESWA	H3A
336A4940JDP8M2T1DAU	7	1	—	ESWA	H1A
336A4940JDP8M2T1DAE	7	1	—	ESWA	H1A
336A4940JDP8T1TDAE	8	0	—	ESWA	H3A

When used to replace an existing N-TRON® switch, the following three part kits include both the switch and the required port adapter(s):

- PK-IS420ESWAH1A = IS420ESWAH1A + 336A5026P01 (quantity 1)
- PK-IS420ESWAH2A = IS420ESWAH2A + 336A5026P01 (quantity 2)
- PK-IS420ESWBH1A = IS420ESWBH1A + 336A5026P01 (quantity 1)

1.14.2.2 Connectors

The RJ-45 connectors support multiple insertions and removals with an estimated service life expectancy of 200 insertion/removal cycles. Connector components are exposed to torsion forces across any axis of the connector and tension forces that are static from cable weight and cable dressing. Dynamic stresses are imposed on the connectors from transients in assembled system transport to the plant site and operation in a high vibration power production environment. Connector design anticipated static forces of three pounds force (89.9 Newton) per connection while complying with the other dynamic operating load requirements.

Connector	Description
28 V dc power	Phoenix® contact part number MC 1.5/S-STF-3.81
Copper	RJ-45 ports for Cat 5e UTP
Fiber	LC-type † Single Mode Fiber (SMF) requires the additional IR SFP single-mode transducer, GE part # 65G2100–008.
† A port adapter is used if needing to interface an existing SC fiber termination to the LC fiber port. GE part # 336A5026P01 SC to LC adapter is required for multi-mode fiber (most common). GE part # 336A5026P02 SC to LC adapter is required for single-mode fiber.	

Control Power Connections, Phoenix MC 1,5/2-STF-3,81 - Order # 1827703

Item	Minimum	Maximum	Units
Wire size	28	16	AWG
Wire cross section	0.14	1.5	mm^2
Connector screw torque	0.22	0.25	NM

1.14.3 Operation

The performance of a level 1 Ethernet switch is mainly centered on the ability to buffer packets. When a level 1 switch has a continuous stream of incoming broadcast or multicast packets, the switch must in turn send those packets out upon complete reception. A single incoming stream should require enough space to buffer one packet or at the most one packet per port. When the switch has multiple incoming streams, it is only able to relieve one of the incoming streams and must buffer the rest for later transmission.

1.14.3.1 Conformance Criteria

The packet traffic can be synchronized by IEEE 1588 timing and triggered to initiate within a 1-microsecond packet start window. The switch's capability and conformance is tested to meet the following four criteria:

- Initiation of the required Multicast packet load on one port, without IEEE 802.3x flow control negotiated
- Initiation of the required Multicast packet load on one port, with IEEE 802.3x flow control negotiated
- Initiation of the required Multicast packet load distributed across all ports, packet count per port must average required per number of switch ports with no IEEE 802.3x flow control
- Initiation of the required packet Multicast load distributed across all ports, packet count per port must average 200 per number of switch ports with IEEE 802.3x flow control negotiated on half the ports

1.14.3.2 Flow Control (Pause)

The switch supports flow control between switches. It uses IEEE defined pause packets to receive and honor pause packets. The switch only sends the pause packets if it needs flow control on a port.

1.14.3.3 Reliability and Performance

Because high reliability is critical to any controls solutions business, the switch exceeds 4 million hours Mean Time Between Failures (MTBF) at 35°C (95 °F) ambient temperature, ground fixed controlled environment. The switch also meets the following performance criteria:

Performance Criteria

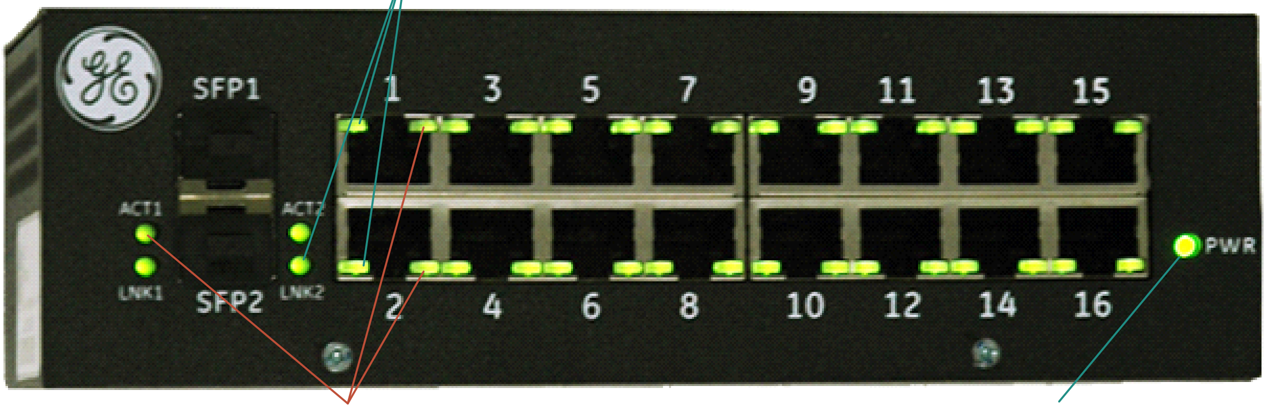
Feature	Description
Switch latency	Switch packet latency does not exceed required application limits.
Switch architecture	The switch supports store and forward architecture, providing high data confidence.
Inrush current	The switch provides soft start capability that limits inrush current to less than 200% of the normal operating current.

1.14.4 IONet Switch Specifications

Item	Description
Mounting	The switch enclosure can be panel mounted (switch mounts to rear wall of panel with bracket) or DIN-rail mounted. DIN-rail mounting meets vibration and shock specifications. User connections are freely accessible with both mounting types.
Dimensions (width x depth x height)	ESWA: 138 x 86 x 56 mm (5.45 x 3.40 x 2.20 in) ESWB: 188 x 86 x 56 mm (7.40 x 3.40 x 2.20 in)
Incoming power connection	Supports two redundant diode-OR'd power supply inputs of 18 to 36 V dc
Cooling	Convection cooled when mounted vertically or horizontally
Coating	Resistant to corrosion with provisions made for grounding per IEC 60721-3-3 Class 3C2
Ambient rating for enclosure design	IS420ESWAHxA rated for -40 to 70°C (-40 to 158 °F) IS420ESWBHxA rated for -30 to 65°C (-22 to 149 °F) *Refer to the Mark VIe and Mark VIeS Control Systems Volume I: System Guide (GEH-6721_Vol_I), the chapter Technical Regulations, Standards, and Environments.*
Absolute Maximum Current	IS420ESWAHxA: < 0.5 A IS420ESWBHxA: < 1.0 A
Shipping vibration, shock	The switch can survive 72 hours at 0.3 G rms between frequencies of 4 to 16 Hz. Three shocks of 15G, 2-millisecond impulse each repeated for all three axes as mounted on panel base.
Operating vibration	Can survive 1.0 G Horizontal, 0.5 G vertical at 15 to 120 Hz

1.14.5 Diagnostics

The following figure defines the LED functions on the ESWx switch.



For each of the 16 ports (and SPF ports), the **Link** LED functions as follows:

- Solid green with 100 MB link
- Solid yellow with 10 MB link
- Not lit if no link

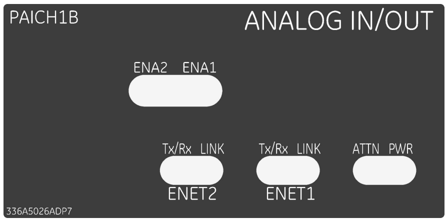
For each of the 16 ports (and SPF ports), the **Activity** LED functions as follows:

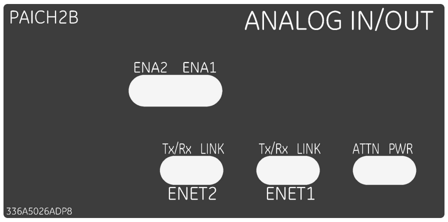
- flashes green for activity at full duplex
- flashes yellow for activity at half duplex

Power is solid green when internal power supply is up and regulating

2 PAIC, YAIC Analog I/O Modules

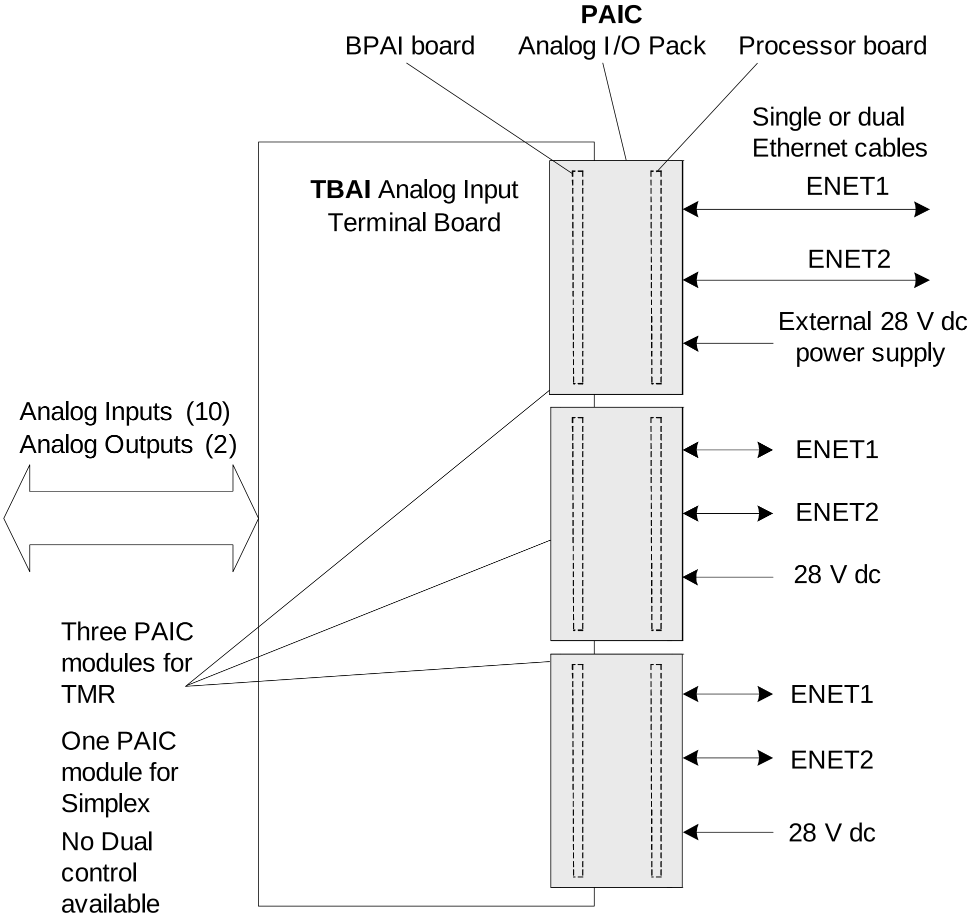
2.1 Mark VIe PAIC Analog I/O Pack





The Analog I/O pack (PAIC) provides the electrical interface between one or two I/O Ethernet networks and an analog input terminal board. The PAIC contains a BPPx processor board and an acquisition board specific to the analog I/O function. The PAIC provides 10 analog inputs. The first eight inputs can be configured as ±5 V or ±10 V inputs, or 4-20 mA current loop inputs. The last two inputs can be configured as ±1 mA or 4-20 mA current inputs. The load terminal resistors for current loop inputs are located on the terminal board and voltage is sensed across these resistors by the PAIC.

PAICH1 or H2 provides two 0-20 mA current loop outputs. The PAICH2 also includes extra hardware to support 0-200 mA current on the first output only. The I/O pack receives or sends data to the controller through dual RJ-45 Ethernet connectors and has a three-pin connector to power it on. Communication to field devices is through a DC-37 pin connector that connects directly with the associated terminal board. Visual diagnostics are provided through indicator LEDs.



2.1.1 PAIC Compatibility

The following are PAIC I/O pack versions and minimum software requirements:

- The PAICH1A and H2A contain a BPPB processor. These processors are reaching end of life. With ControlST* software V04.04 and later, these I/O packs can be replaced with PAICH1B or H2B.
- The PAICH1B and H2B contain a BPPC processor that is supported in the ControlST software V04.04 and later.
- PAICH2A and H2B include extra hardware to support 0-200 mA current on the first output.

Terminal Board Compatibility

Terminal Board	Module Redundancy
TBAIH1C †	One I/O pack with one or two IONets Three I/O packs with one IONet on each pack
STAIH1A, STAIH2A	One I/O pack with one or two IONets
SAIIH1A, SAIIH2A	
† The PAIC is only compatible with the H1C version of TBAI	

2.1.2 PAIC Installation

➢ **To install the PAIC I/O pack**

1. Securely mount the desired terminal board.
2. Directly plug the PAIC I/O pack into the terminal board connectors.
3. Mechanically secure the I/O pack(s) using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right-angle force applied to the DC-37 pin connector between the I/O pack and the terminal board. The adjustment should only be required once in the service life of the product.

Note The I/O pack mounts directly to the terminal board. The simplex terminal board has a single DC-37 pin connector that receives the I/O pack. The TMR-capable terminal board has three DC-37 pin connectors and can also be used in simplex mode if only one I/O pack is installed. The I/O pack directly supports all of these connections.

4. Plug in one or two Ethernet cables depending on the system configuration. The I/O pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
5. Apply power to the I/O pack by plugging in the connector on the side of the pack. It is not necessary to remove power from the cable before plugging it in because the I/O pack has inherent soft-start capability that controls current inrush on power application.
6. Use the ToolboxST* application to configure the I/O pack as necessary. From the ToolboxST application, press F1 for help.

2.1.2.1 Connectors

The I/O pack contains the following connectors:

- A DC-37 pin connector on the underside of the I/O pack connects directly to the terminal board. The connector contains the 24 input signals, ID signal, relay coil power, and feedback multiplex command.
- An RJ-45 Ethernet connector named ENET1 on the side of the pack is the primary system interface.
- A second RJ-45 Ethernet connector named ENET2 on the side of the pack is the redundant or secondary system interface.
- A 3-pin power connector on the side of the I/O pack is for 28 V dc power for the I/O pack and terminal board.

2.1.3 Operation

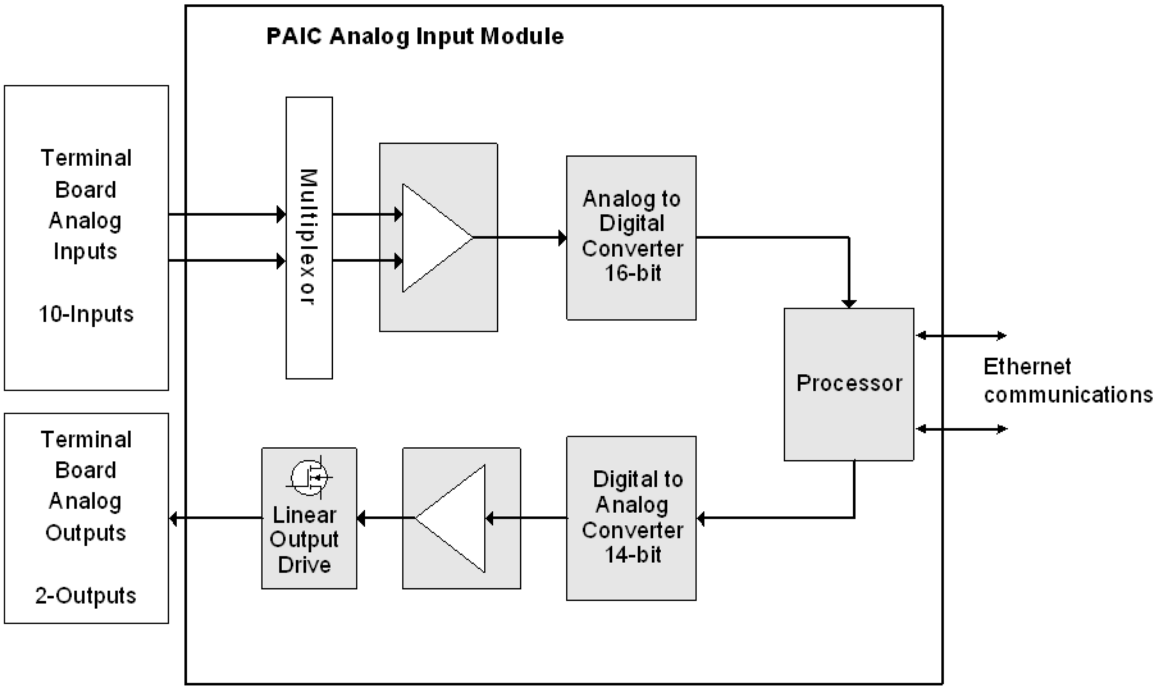
The following features are common to the distributed I/O modules:

- *BPPx Processor*
- *Processor LEDs*
- *Power Management*
- *ID Line*
- *I/O Module Common Diagnostic Alarms*

2.1.3.1 Analog Input Hardware

The PAIC accepts input voltage signals from the terminal board for all 10 input channels. The analog input section consists of an the following items:

- Analog multiplexer block
- Several gain and scaling selections
- 16-bit analog-to-digital converter (ADC)

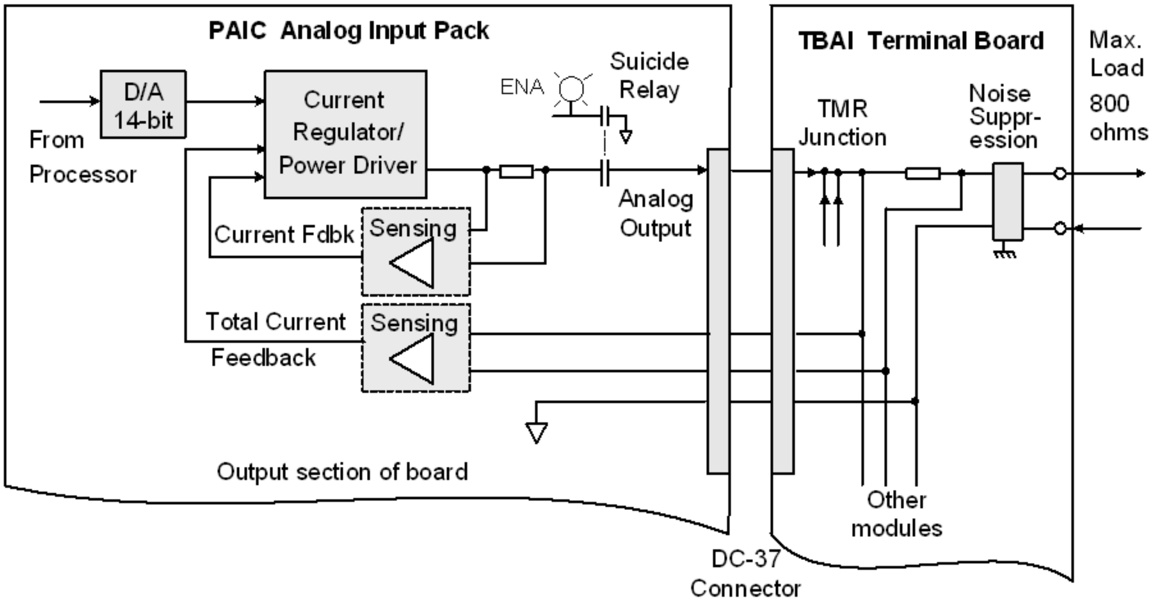

PAIC Analog Input Module
Terminal Board Analog Inputs
10-Inputs
Multiplexor
Analog to Digital Converter 16-bit
Processor
Ethernet communications
Terminal Board Analog Outputs
2-Outputs
Linear Output Drive
Digital to Analog Converter 14-bit

Inputs 1-8 can be individually configured as ±5 V, ±10 V, or 4-20 mA scale signals, depending on the input configuration. Inputs 9-10 can only be configured for ±1 mA or 4-20 mA. The terminal board provides a 250 Ω burden resistor when configured for current inputs yielding a 5 V signal at 20 mA. These analog input signals are first passed through a passive, low pass filter network with a pole at 75.15 Hz. Voltage signal feedbacks from the analog output circuits and calibration voltages are also sensed by the PAIC analog input section.

2.1.3.2 Analog Output Hardware

The PAIC includes two 0-20 mA analog outputs capable of 18 V compliance running simplex or TMR. A 14-bit DAC commands a current reference to the current regulator loop in the PAIC that senses current both in the PAIC pack and on the terminal board. In TMR mode, the three current regulators in each PAIC share the commanded current loads among themselves. Analog output status feedbacks for each output include:

- Current reference voltage
- Individual current (output current sourced from within the PAIC)
- Total current (as sensed from the terminal board, summed current in TMR mode)



Each analog output circuit also includes a normally open mechanical relay to enable or disable operation of the output. The relay is used to remove a failed output from a TMR system allowing the remaining two PAICs to create the correct output without interference from the failed circuit. When the suicide relay is de-activated, the output opens through the relay, open-circuiting that PAIC's analog output from the customer load that is connected to the terminal board. The mechanical relay's second normally open contact is used as a status to indicate position of the relay to the control and includes visual indication with an LED.

2.1.3.3 PAICH2 Additional Hardware

The PAICH2 includes support for additional hardware in the form of an add-on daughterboard that adds 0-200 mA output capability to the first analog output, analog output #1. The 200 mA circuit is capable of 9 V compliance and is identical to the diagram displayed with the exception of the P28 power source. Power for the 200 mA circuit is derived from a variable voltage source on the daughterboard to reduce power dissipation of the linear output transistor.

Note When configured for 200 mA mode operation, the 20 mA suicide relay is automatically opened and the 200 mA suicide relay on the optional daughterboard is closed.

2.1.4 PAIC Specifications

Item	PAIC Specification
Number of channels	12 channels per terminal board with 10 Analog Inputs (AI) and 2 Analog Outputs (AO)
AI types supported	Inputs 1 to 8: ±5 V dc, ±10 V dc, or 4–20 mA Inputs 9 to 10: 4–20 mA or ±1 mA
Input converter resolution	16-bit analog-to-digital converter
Scan time	Normal scan 5 ms (200 Hz). Note that maximum controller frame rate is 100 Hz.
Input accuracy	With TBAI or STAI terminal boards: ±0.1% of full scale over the full operating temp. range With SAII terminal board: ±0.4% of full scale over the full operating temperature range
Noise suppression on inputs	The ten circuits have a hardware filter with single pole down break at 80 Hz. A software filter, using a two pole low pass filter, is configurable for: 0 (no filter), 0.75, 1.5, 3, 6, or 12 Hz.
Common mode rejection	Ac common mode rejection 60 dB at 60 Hz, with up to ±5 V common mode voltage. Dc common mode rejection 80 dB with from -5 to +7 peak V common mode voltage
Common mode voltage range	±5 V (±2 V CMR for the ±10 V inputs)
Output converter	14-bit D/A converter with 0.5% accuracy
Output load	800 Ω max for 0-20 mA output 50 Ω max for 0-200 mA output
Output accuracy	±0.5% of full measurement range
Power consumption	5.3 W typical, 6.2 W worst case
Compressor stall detection	Detection and relay operation time delay is configurable from 10 to 40 ms (default is 20 ms)
Size	8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in x 1.65 in x 4.78 in)
† Ambient rating for enclosure design	PAICH1B is rated from -40 to 70 ºC (-40 to 158 ºF) PAICH1A is rated from -30 to 65 ºC (-22 to 149 ºF)
Technology	Surface mount

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

2.1.5 PAIC Diagnostics

The PAIC or YAIC performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set
- Each analog input has hardware limit checking based on configurable high and low levels for 4-20 mA inputs and preset (non-configurable) levels for ± 5 V, ± 10 V, and ± 1 mA inputs. If the limit is exceeded, then the I/O pack raises an alarm and marks the input as unhealthy. A logic signal (L3DIAG_pack) is set, which refers to the entire board.
- Each input has configurable system limit checking with high and low levels, latching, and non-latching selection options. These limits can be used in the programming of the controller to generate process alarms. This controller logic requires using a RSTSYS pin on a SYS_OUTPUTS block to reset the out of limits status when the latch is enabled. System limit checking can be configured as Enable/Disable at point level, and are only functional only when system limits are enabled at module level (Parameters tab).
- The analog input hardware includes precision reference voltages in each scan. Measured values are compared against expected values and are used to confirm health of the analog to digital converter circuits.
- Analog output current is sensed on the terminal board using a small burden resistor. The I/O pack conditions this signal and compares it to the commanded current to confirm health of the digital to analog converter circuits.
- The analog output suicide relay is continuously monitored for agreement between commanded state and feedback indication.

Details of the individual diagnostics are available from the ToolboxST application. The diagnostic signals can be individually latched and then reset with the RSTDIAG signal if they go healthy.

2.1.5.1 Status LEDs

Relay Application LEDs

LED	Label	Description
Yellow	ENA1	Indicates the closure of the relay controlling output 1
Yellow	ENA2	Indicate the closure of the relay controlling output 2

2.1.6 PAIC ToolboxST Configuration

2.1.6.1 Parameters

Parameter	Description	Choices
SystemLimits	Enable or *temporarily* disable all system limit checks. Setting this parameter to Disable will cause a diagnostic alarm to occur.	Enable, Disable
Min_ MA_Input	Select minimum current for healthy 4-20 mA input	0 to 22.5 mA
Max_ MA_Input	Select maximum current for healthy 4-20 mA input	0 to 22.5 mA
CompStallType	The Compressor Stall function is used by GE. Refer to GEH-6721_Vol_III for GE Industrial Applications. The below parameters are also only relevant to this function.	Unused (default), three_xducer, two_ Xducer
InputForPS3A	Select analog input circuit for PS3A	AnalogInput 1, 2, 3, or 4
InputForPS3B	Select analog input circuit for PS3B	AnalogInput 1, 2, 3, or 4
InputForPS3C	Select analog input circuit for PS3C	AnalogInput 1, 2, 3, or 4
SelMode	This select mode for excessive difference pressure is available only with the two_xducer type.	Max, Avg
PressDelta	Excessive difference pressure threshold	5 to 500
TimeDelay	Time delay on stall detection in (milliseconds)	10 to 40
KPS3_Drop_Min	Minimum pressure rate	10 to 2000
KPS3_Drop_I	Pressure rate intercept	-250 to 100
KPS3_Drop_S	Pressure rate slope	.05 to 10
KPS3_Delta_S	Pressure delta slope	.05 to 10
KPS3_Delta_I	Pressure delta intercept	-250 to 100
KPS3_Delta_Mx	Pressure delta max	-250 to 100
KPS3_Drop_L	Threshold pressure rate	10 to 2000
KPS3_Drop_Mx	Max pressure rate	10 to 2000

2.1.6.2 Inputs

Input	Description	Choices
AnalogInput01 through AnalogInput10	First of 10 Analog Inputs – board point. Point edit	(Input REAL)
InputType	Current or voltage input type	Unused or 4-20 mA (for any AnalogInput) ±5 V, ±10 V (for AnalogInput01 to 08 only) ±1 mA (for AnalogInput09 and 10 only)
Low_Input	Value of input current (mA) or voltage (V) at low end of input scale	-10 to 20
Low_Value	Value of input in engineering units at Low_Input	-3.4082 e + 038 to 3.4028 e + 038
High_Input	Value of input current (mA) or voltage (V) at high end of input scale	-10 to 20
High_Value	Value of input in engineering units at High_Input	-3.4082 e + 038 to 3.4028 e + 038
InputFilter	Bandwidth of input signal filter	Unused, 0.75hz, 1.5hz, 3hz, 6hz, 12hz
TMR_DiffLimit	Difference limit for voted inputs in % of High_Value - Low_Value	0 to 200
SysLim1Enabl	Enable System Limit 1 fault check	Enable, Disable
SysLim1Latch	System Limit 1 fault latch - if set, requires a Reset System Limits (RSTSYS) on SYS_OUTPUTS block to clear	Latch, NotLatch
SysLim1Type	System Limit 1 Check Type	>= or <=
SysLim1	System Limit 1 in engineering units	-3.4082 e + 038 to 3.4028 e + 038
SysLim2Enabl	Enable System Limit 1 fault check	Enable, Disable
SysLim2Latch	System Limit 2 fault latch - if set, requires a Reset System Limits (RSTSYS) on SYS_OUTPUTS block to clear	Latch, NotLatch
SysLim2Type	System Limit 2 Check Type	>= or <=
SysLimit2	System Limit 2 in Engineering Units	-3.4082 e + 038 to 3.4028 e + 038
DiagHighEnab	Enables the generation of a high limit diagnostic alarm when the value of the 4-20 mA input is greater than the value of parameter *Max_MA_Input*	Enable, Disable
DiagLowEnab	Enables the generation of a low limit diagnostic alarm when the value of the 4-20 mA input is less than the value of parameter *Min_MA_Input*	Enable, Disable
TMR_DiffLimt	Diag limit, TMR input vote difference, in percent of (High_Value - Low_Value)	0 to 200 %

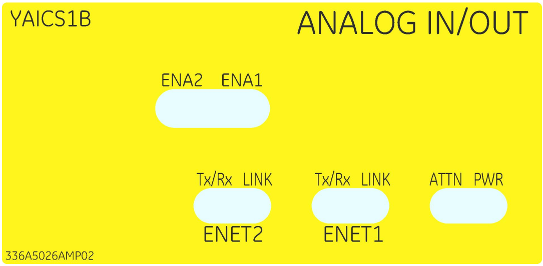
2.1.6.3 Outputs

Output Name	Output Description	Choices
AnalogOutput01 - AnalogOutput02	First of two analog outputs - board point, Point edit	Output REAL
Output_MA	Output current, mA selection. Note: 0-200mA selection is only available on a PAICH2. Terminal board jumper JPO selection must match with this configuration to ensure proper operation.	Unused, 0-20 mA, 0-200 mA (first output)
OutputState	State of the outputs when offline. When the PAIC loses communication with the controller, this parameter determines how it drives the outputs: PwrDownMode - Open the output relay and drive outputs to zero current HoldLastVal - Hold the last value received from the controller Output_Value - Go to the configured output value set by the parameter Output_Value	PwrDownMode HoldLastVal Output_Value
Output_Value	Pre-determined value for the outputs	-3.4082 e + 038 to 3.4028 e + 038
Low_MA	Output mA at low value	0 to 200 mA
Low_Value	Output in Engineering Units at Low_MA	-3.4082 e + 038 to 3.4028 e + 038
High_MA	Output mA at high value	0 to 200 mA
High_Value	Output value in Engineering Units at High_MA	-3.4082 e + 038 to 3.4028 e + 038
TMR_Suicide	Enables suicide for faulty output current, TMR only	Enable, Disable
TMR_SuicLimit	Suicide threshold (Load sharing margin) for TMR operation, in mA	0 to 200 mA
D/A_ErrLimit	Difference between D/A reference and feedback, in % for suicide, TMR only	0 to 200 %
Dither_Ampl	Dither % current of Scaled Output mA	0 to 10
Dither_Freq	Dither rate in Hertz	Unused, 12.5hz, 25hz, 33.33hz, 50hz, 100hz

2.1.6.4 Variables

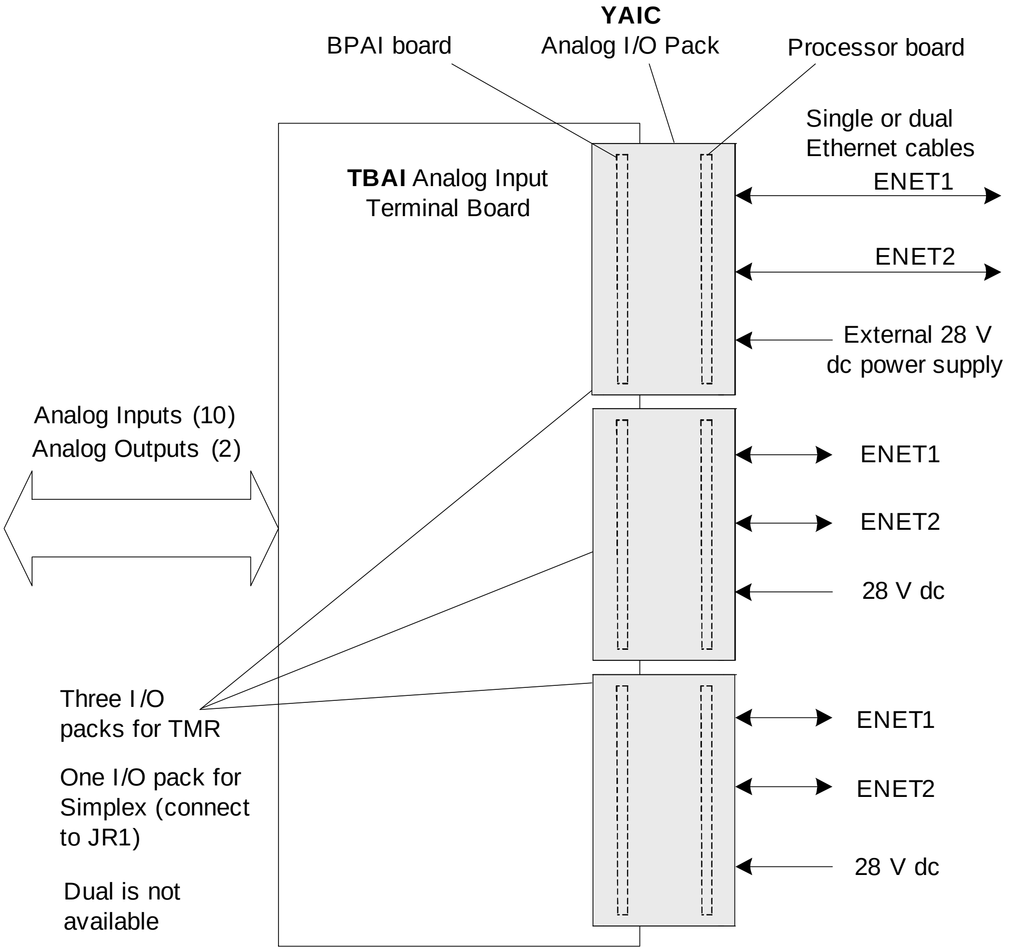
Variable Name	Description	Direction	Type
L3DIAG_PAIC	Board diagnostic	Input	BOOL
LINK_OK_PAIC	I/O Link OK indication	Input	BOOL
ATTN_PAIC	Module Diagnostic	Input	BOOL
IOPackTmpr	I/O Pack Temperature (deg F)	Input	REAL
PS18V_PAIC	I/O 18V Power Supply Indication	Input	BOOL
PS28V_PAIC	I/O 28V Power Supply Indication	Input	BOOL
SysLimit1_1	System Limit 1	Input	BOOL
↓	↓	Input	BOOL
SysLimit1_10	System Limit 1	Input	BOOL
SysLimit2_1	System Limit 2	Input	BOOL
↓	↓	Input	BOOL
SysLimit2_10	System Limit 2	Input	BOOL
OutSuicide1	Status of Suicide Relay for Output 1	Input	BOOL
OutSuicide2	Status of Suicide Relay for Output 2	Input	BOOL
DeltaFault	Excessive difference pressure	Input	BOOL
Out1MA	Feedback, Total Output Current, mA	Input	REAL
Out2MA	Feedback, Total Output Current, mA	Input	REAL
CompPressSel	The Compressor Stall function is used by GE. Refer to GEH-6721_Vol_III for GE Industrial Applications.	Input	REAL
CompStall		Input	BOOL
CompStalPerm		Input	BOOL
PressRateSel		Input	REAL

2.2 Mark VIeS YAIC Analog I/O Pack



The Analog I/O pack (YAIC) provides the electrical interface between one or two I/O Ethernet networks and an analog I/O terminal board. The YAIC contains a common processor board and an acquisition board specific to the analog input function. The I/O pack is capable of handling up to 10 analog inputs, the first eight of which can be configured as ±5 V or ±10 V inputs, or 4-20 mA current loop inputs. The last two inputs can be configured as ±1 mA or 4-20 mA current inputs.

The load terminal resistors for current loop inputs are located on the terminal board and voltage is sensed across these resistors by the YAIC. The I/O pack also includes support for two 0-20 mA current loop outputs. The I/O pack receives or sends data through dual RJ-45 Ethernet connectors to the controller and has a three-pin connector to power it on. Output is through a DC-37 pin connector that connects directly with the associated terminal board connector. Visual diagnostics are provided through indicator LEDs.



2.2.1 YAIC Compatibility

The YAIC I/O pack contains an internal processor board. The following table lists the available versions of the YAIC.

YAIC Version Compatibility

I/O Pack	Processor Board	Compatible (Supported) Firmware	ControlST Software Suite Versions
YAICS1A	BPPB	V04.06	Supported in V04.06 and all later versions
YAICS1B	BPPC	V05.01 and later	Supported in V06.01 and later versions

Attention

YAICS1A and YAICS1B I/O pack versions cannot be mixed on the same T-type terminal board.

All three YAIC I/O packs in a TMR set must be the same hardware form.

To upgrade or replace the YAIC, refer to the following replacement procedures for specific instructions:

- *Replace Mark VIeS Safety I/O Pack with Same Hardware Form*
- *Replace Mark VIeS Safety I/O Pack with Upgraded Hardware Form*

The YAIC I/O pack is compatible with the TBAISIC and STAIS#A terminal boards.

YAIC Terminal Board Compatibility

Terminal Board	Description	I/O Pack Redundancy		
		Simplex	Dual	TMR
TBAIS1C	TMR Analog input/output terminal board	Yes	No	Yes
STAIS#A	Simplex Analog input/output terminal board	Yes	No	No

I/O pack redundancy refers to the number of I/O packs used in a signal path, as follows:

- Simplex uses one I/O pack.
- TMR uses three I/O packs.

2.2.2 YAIC Installation

➢ **To install a new YAIC I/O module into an existing Mark VIeS panel**

1. Securely mount the desired terminal board.
2. Directly plug one YAIC I/O pack for simplex or three YAIC I/O packs for TMR into the terminal board connectors.
3. Mechanically secure the packs using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right-angle force applied to the DC-37 connector between the pack and the terminal board. The adjustment should only be required once in the life of the product.
4. Plug in one or two Ethernet cables depending on the system configuration. The pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller. These choices are also defined in the ToolboxST configuration.
5. Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to insert this connector with the power removed from the cable as the I/O pack has inherent soft-start capability that controls current inrush on power application.
6. Configure the I/O pack as necessary using the ToolboxST application.

2.2.2.1 Connectors

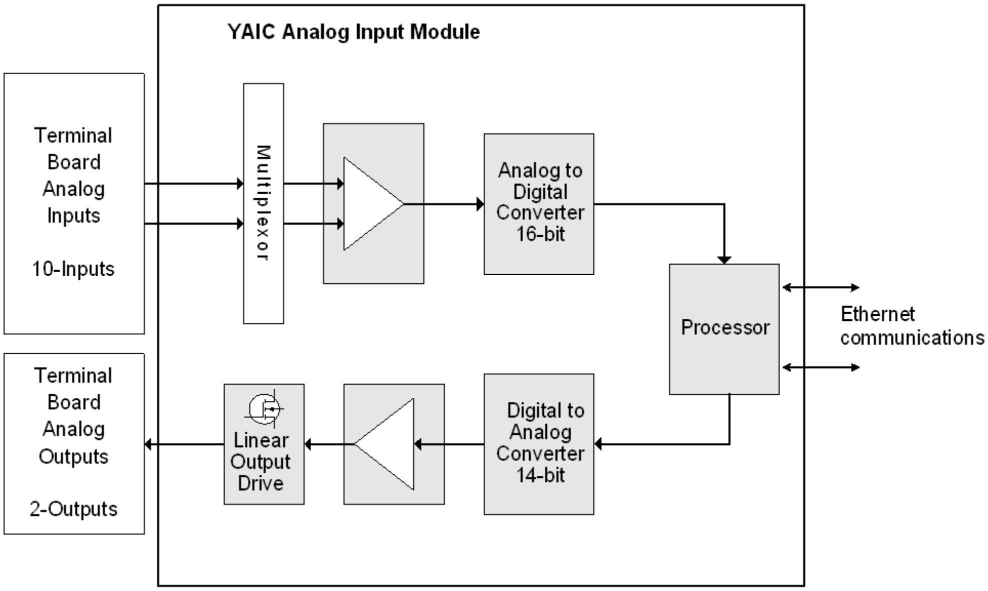
The I/O pack contains the following connectors:

- A DC-37 pin connector on the underside of the YAIC connects directly to the discrete input terminal board. The connector contains the 24 input signals, ID signal, relay coil power, and feedback multiplex command.
- An RJ-45 Ethernet connector named ENET1 on the side of the pack is the primary system interface.
- A second RJ-45 Ethernet connector named ENET2 on the side of the I/O pack is the redundant or secondary system interface.
- A 3-pin power connector on the side of the pack is for 28 V dc power for the pack and terminal board.

2.2.3 YAIC Operation

2.2.3.1 Analog Input Hardware

The YAIC accepts input voltage signals from the terminal board for all 10 input channels. The analog input section consists of an analog multiplexer block, several gain and scaling selections, and a 16-bit analog-to-digital converter (ADC).

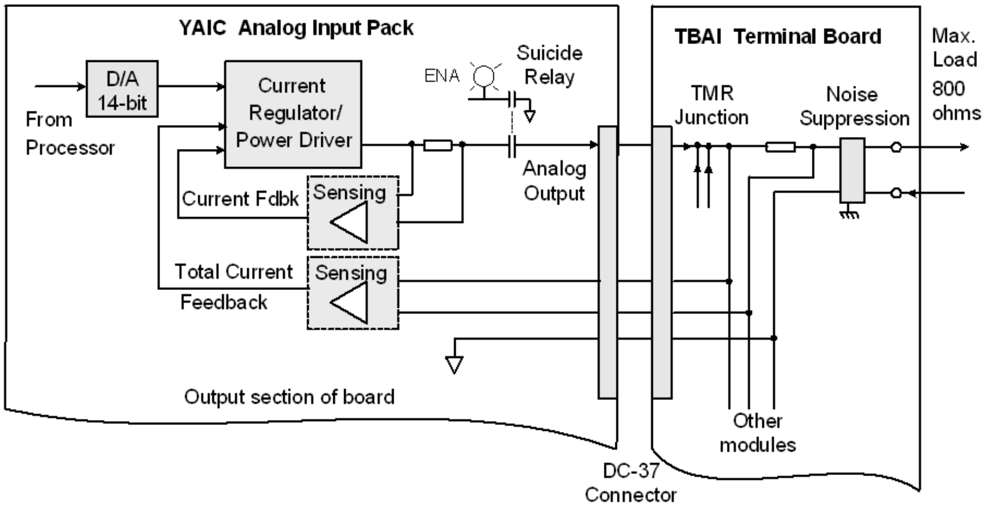

YAIC Analog Input Module
Terminal Board Analog Inputs
10-Inputs
Multiplexor
Analog to Digital Converter 16-bit
Processor
Ethernet communications
Terminal Board Analog Outputs
2-Outputs
Linear Output Drive
Digital to Analog Converter 14-bit

Inputs 1–8 can be individually configured as ±5 V or ±10 V, or 4–20 mA scale signals, depending on the input configuration. Inputs 9–10 can only be configured for ±1 mA or 4-20 mA. The terminal board provides a 250 Ω burden resistor when configured for current inputs yielding a 5 V signal at 20 mA. These analog input signals are first passed through a passive, low pass filter network with a pole at 75.15 Hz. Voltage signal feedbacks from the analog output circuits and calibration voltages are also sensed by the YAIC analog input section.

2.2.3.2 Analog Output Hardware

The YAIC includes two 0-20 mA analog outputs capable of 18 V compliance running simplex or TMR. A 14-bit digital-to-analog converter (DAC) commands a current reference to the current regulator loop in the YAIC that senses current both in the YAIC pack and on the terminal board. In TMR mode, the three current regulators in each YAIC share the commanded current loads among themselves. Analog output status feedbacks for each output include:

- Current reference voltage
- Individual current (output current sourced from within the YAIC)
- Total current (as sensed from the terminal board, summed current in TMR mode)



Each analog output circuit also includes a normally open mechanical relay to enable or disable operation of the output. The relay is used to remove a failed output from a TMR system allowing the remaining two YAICs to create the correct output without interference from the failed circuit. When the suicide relay is de-activated, the output opens through the relay, open-circuiting the analog output from the customer load that is connected to the terminal board. The mechanical relay has a second normally open contact that is used as a status to indicate position of the relay to the control and includes visual indication with an LED.

2.2.4 Specifications

Item	YAIC Specification
Number of Cchannels	12 channels per terminal board (10 AI, 2 AO)
AI Types Supported	Inputs 1 to 8: ±5 V dc, ±10 V dc, or 4–20 mA Inputs 9 to 10: 4–20 mA or ±1 mA
Input Converter Resolution	16-bit ADC
Scan Time	Normal scan 5 ms (200 Hz) *The update rate in the controller is based on the frame rate.*
Input Accuracy	0.1% of full scale over the full operating temperature range.
Noise Suppression on Inputs	The 10 circuits have hardware filter with single pole down break at 500 rad/s. A software filter, using a two pole low pass filter, is configurable for: 0.75 Hz, 1.5 Hz, 3 Hz, 6 Hz, 12 Hz
Common Mode Rejection	AC CMR 60 dB at 60 Hz, with up to ±5 V common mode voltage. DC CMR 80 dB with -5 to +7 peak V common mode voltage
Common Mode Voltage Range	±5 V (±2 V CMR for the ±10 V inputs)
Output Converter	14-bit D/A converter with 0.5% accuracy
Output Load	800 Ω max for 4-20 mA output
Output Accuracy	±0.5% of full measurement range
Power Consumption	5.3 watts typical, 6.2 watts worst case
Compressor Stall Detection	Not supported
Size	8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in x 1.65 in x 4.78 in)
Ambient Rating for Enclosure Design†	-30 to 65 ºC (-22 to 149 ºF)
Technology	Surface mount

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

2.2.5 YAIC Diagnostics

The PAIC or YAIC performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set
- Each analog input has hardware limit checking based on configurable high and low levels for 4-20 mA inputs and preset (non-configurable) levels for ± 5 V, ± 10 V, and ± 1 mA inputs. If the limit is exceeded, then the I/O pack raises an alarm and marks the input as unhealthy. A logic signal (L3DIAG_pack) is set, which refers to the entire board.
- Each input has configurable system limit checking with high and low levels, latching, and non-latching selection options. These limits can be used in the programming of the controller to generate process alarms. This controller logic requires using a RSTSYS pin on a SYS_OUTPUTS block to reset the out of limits status when the latch is enabled. System limit checking can be configured as Enable/Disable at point level, and are only functional only when system limits are enabled at module level (Parameters tab).
- The analog input hardware includes precision reference voltages in each scan. Measured values are compared against expected values and are used to confirm health of the analog to digital converter circuits.
- Analog output current is sensed on the terminal board using a small burden resistor. The I/O pack conditions this signal and compares it to the commanded current to confirm health of the digital to analog converter circuits.
- The analog output suicide relay is continuously monitored for agreement between commanded state and feedback indication.

Details of the individual diagnostics are available from the ToolboxST application. The diagnostic signals can be individually latched and then reset with the RSTDIAG signal if they go healthy.

2.2.5.1 Status LEDs

Relay Application LEDs

LED	Label	Description
Yellow	ENA1	Indicates the closure of the relay controlling output 1
Yellow	ENA2	Indicate the closure of the relay controlling output 2

2.2.6 YAICS1B Configuration

2.2.6.1 Parameters

Parameter	Description	Choices
SystemLimits	Enable or *temporarily* disable all system limit checks. Setting this parameter to Disable will cause a diagnostic alarm to occur.	Enable, Disable
Min_ MA_Input	Select minimum current for healthy 4-20 mA input	0 to 22.5 mA
Max_ MA_Input	Select maximum current for healthy 4-20 mA input	0 to 22.5 mA

2.2.6.2 Inputs

Input	Description	Choices
AnalogInput01 through AnalogInput10	First of 10 Analog Inputs – board point. Point edit	(Input REAL)
InputType	Current or voltage input type	Unused or 4-20 mA (for all Analog Inputs) ±5 V or ±10 V (for AnalogInput01 to 08 only) ±1 mA (for AnalogInput09 and 10 only)
Low_Input	Value of input current (mA) or voltage (V) at low end of input scale	-10 to 20
Low_Value	Value of input in engineering units at Low_Input	-3.4082 e + 038 to 3.4028 e + 038
High_Input	Value of input current (mA) or voltage (V) at high end of input scale	-10 to 20
High_Value	Value of input in engineering units at High_Input	-3.4082 e + 038 to 3.4028 e + 038
InputFilter	Bandwidth of input signal filter	Unused, 0.75hz, 1.5hz, 3hz, 6hz, 12hz
TMR_DiffLimit	Difference limit for voted inputs in % of High_Value - Low_Value	0 to 200
SysLim1Enabl	Enable System Limit 1 fault check	Enable, Disable
SysLim1Latch	System Limit 1 fault latch - if set, requires a Reset System Limits (RSTSYS) on SYS_OUTPUTS block to clear	Latch, NotLatch
SysLim1Type	System Limit 1 Check Type	>= or <=
SysLim1	System Limit 1 in engineering units	-3.4082 e + 038 to 3.4028 e + 038
SysLim2Enabl	Enable System Limit 1 fault check	Enable, Disable
SysLim2Latch	System Limit 2 fault latch - if set, requires a Reset System Limits (RSTSYS) on SYS_OUTPUTS block to clear	Latch, NotLatch
SysLim2Type	System Limit 2 Check Type	>= or <=
SysLimit2	System Limit 2 in Engineering Units	-3.4082 e + 038 to 3.4028 e + 038
DiagHighEnab	Enables the generation of a high limit diagnostic alarm when the value of the 4-20 mA input is greater than the value of parameter *Max_MA_Input*	Enable, Disable
DiagLowEnab	Enables the generation of a low limit diagnostic alarm when the value of the 4-20 mA input is less than the value of parameter *Min_ MA_Input*	Enable, Disable
TMR_DiffLimt	Diag limit, TMR input vote difference, in percent of (High_Value - Low_Value)	0 to 200 %

2.2.6.3 Outputs

Output Name	Output Description	Choices
AnalogOutput01 - AnalogOutput02	First of two analog outputs - board point, Point edit	Output REAL
Output_MA	Output current, mA selection.	Unused, 0-20 mA
OutputState	State of the outputs when offline. When the PAIC loses communication with the controller, this parameter determines how it drives the outputs: PwrDownMode - Open the output relay and drive outputs to zero current HoldLastVal - Hold the last value received from the controller Output_Value - Go to the configured output value set by the parameter Output_Value	PwrDownMode HoldLastVal Output_Value
Output_Value	Pre-determined value for the outputs	-3.4082 e + 038 to 3.4028 e + 038
Low_MA	Output mA at low value	0 to 200 mA
Low_Value	Output in Engineering Units at Low_MA	-3.4082 e + 038 to 3.4028 e + 038
High_MA	Output mA at high value	0 to 200 mA
High_Value	Output value in Engineering Units at High_MA	-3.4082 e + 038 to 3.4028 e + 038
TMR_Suicide	Enables suicide for faulty output current, TMR only	Enable, Disable
TMR_SuicLimit	Suicide threshold (Load sharing margin) for TMR operation, in mA	0 to 200 mA
D/A_ErrLimit	Difference between D/A reference and feedback, in % for suicide, TMR only	0 to 200 %
Dither_Ampl	Dither % current of Scaled Output mA	0 to 10
Dither_Freq	Dither rate in Hertz	Unused, 12.5hz, 25hz, 33.33hz, 50hz, 100hz

2.2.6.4 Variables

Variable Name	Description	Direction	Type
L3DIAG_YAIC	Board diagnostic	Input	BOOL
LINK_OK_YAIC	I/O Link OK indication	Input	BOOL
ATTN_YAIC	Module Diagnostic	Input	BOOL
IOPackTmpr	I/O Pack Temperature (deg F)	Input	REAL
PS18V_YAIC	I/O 18V Power Supply Indication	Input	BOOL
PS28V_YAIC	I/O 28V Power Supply Indication	Input	BOOL
SysLimit1_1	System Limit 1	Input	BOOL
↓	↓	Input	BOOL
SysLimit1_10	System Limit 1	Input	BOOL
SysLimit2_1	System Limit 2	Input	BOOL
↓	↓	Input	BOOL
SysLimit2_10	System Limit 2	Input	BOOL
OutSuicide1	Status of Suicide Relay for Output 1	Input	BOOL
OutSuicide2	Status of Suicide Relay for Output 2	Input	BOOL
Out1MA	Feedback, Total Output Current, mA	Input	REAL
Out2MA	Feedback, Total Output Current, mA	Input	REAL

2.3 PAIC or YAIC Specific Alarms

The following alarms are specific to the PAIC or YAIC I/O pack.

32-41

Description Analog Input [ ] unhealthy

Possible Cause

- Excitation to transducer is wrong or missing.
- Transducer is defective.
- Analog input current/voltage input is beyond the specified range.
- Terminal board jumper settings do not match the ToolboxST configuration.
- Open or short-circuit on input

Solution

- Check the field wiring and connections to indicated analog input channel.
- Check the field device for failure.
- Verify that the configuration matches terminal board jumper settings for the indicated analog input channel.

44-45

Description Output [ ] individual current feedback unhealthy

Possible Cause

- Commanded output is beyond the range of the output.
- Field wiring problem
- Field device problem
- Open loop or too much resistance in the loop
- I/O pack failed
- Terminal board failed

Solution

- Verify that the commanded output is within the range of the output.
- Confirm the correct I/O pack 28 V input power.
- Check the field wiring and device.
- Replace the I/O pack.

46-47

Description Output [ ] total current feedback unhealthy

Possible Cause

- Commanded output is beyond the range of the output.
- Field wiring problem
- Field device problem
- Open loop or too much resistance in the loop.

Solution

- Verify that the commanded output is within the range of the output.
- Confirm the correct I/O pack 28 V input power.
- Check the field wiring and the component.
- Replace the I/O pack.

48-49

Description Output [ ] Internal reference current unhealthy

Possible Cause I/O pack failure

Solution

- Confirm the correct I/O pack 28 V input power.
- Replace the I/O pack.

66-67

Description Output [ ] Individual current too high relative to total current

Possible Cause In a TMR setup, the individual current feedback is greater than ½ the total current feedback + *TMR_SuicLimit*.

- The *TMR_SuicLimit* is set too low.
- Hardware failure causing one I/O pack to drive too much output current

Solution

- Verify that the value of *TMR_SuicLimit* is set correctly.
- Replace the I/O pack.

70-71

Description Output [ ] Total current varies from reference current

Possible Cause The difference between the commanded output current and total feedback is greater than *TMR_SuicLimit*.

- Field wiring problem
- Open-circuit on output or total loop resistance is too high
- Command is beyond the range of the output.

Solution

- Check field wiring and device.
- Verify that the value of *TMR_SuicLimit* is set correctly.
- Verify that commanded output is within output range.

74-75

Description Output [ ] commanded current fdbk error

Possible Cause The difference between the commanded output current and current feedback on the terminal board is greater than *D/A_ErrLimit* (%).

- Open-circuit on output
- Terminal board output jumper (JPO) setting is incorrect (for output 1).
- Command is beyond the range of the output.

Solution

- Check the field wiring and device.
- Check the JPO jumper setting on the terminal board.
- Verify that the value of *D/A_ErrLimit* is set correctly.
- Verify that the commanded output is within output range.
- Replace the I/O pack.

82-83

Description Output [ ] Suicide relay non-functional

Possible Cause The analog output suicide relay command doesn't match the feedback.

- Relay failure on the acquisition board.
- Hardware failure

Solution Replace the I/O pack.

86

Description Output [ ] 20/200 mA selection non-functional

Note This diagnostic only applies to PAICH2

Possible Cause The analog output has been configured for 200 mA but the hardware is not responding to the configuration.

Solution Replace the I/O pack.

90-91

Description Output [ ] 20/200 mA suicide active

Possible Cause

- Suicide is enabled on analog output.
- Review any additional diagnostics for possible causes.
- The *TMR_SuicLimit* is set too low.
- Field wiring problem
- Command is beyond the range of the output.
- Analog output configuration does not match hardware jumpers.

Solution

- Verify that the value of *TMR_SuicLimit* is set correctly.
- Verify that the value of *D/A_ErrLimit* is set correctly.
- Verify the field wiring connections.
- Verify that the commanded output is within output range.
- On PAICH2, verify that terminal board jumper (JPO) settings for analog output match the configuration (20mA/200mA).

92-93

Description Output [ ] Suicide on overcurrent, check terminal board jumper

Possible Cause

- Incorrect setting of terminal board 20/200 mA jumper
- Hardware failure in I/O pack

Solution

- Check the terminal board jumper (JPO).
- Replace the I/O pack.

97

Description Hardware form (PAICH1) does not support 200mA on Output 01

Possible Cause Analog Output 1 is configured for 0-200 mA, but the PAICH1 does not support 200 mA.

Solution

- Configure the analog output 1 to be 0-20 mA.
- If 200 mA is required, the I/O pack must be replaced with the PAICH2.

98

Description PAICH2 200mA driver temperature ([ ] °F) exceeds the max limit ([ ] °F)

Possible Cause

- The internal temperature on a PAICH2A has exceeded the maximum temperature limit of 185 °F (85 °C)
- The internal temperature on a PAICH2B has exceeded the maximum temperature limit of 194 °F (90 °C).

Solution Check the environmental controls applied to the cabinet containing the I/O pack. The I/O pack does continue to operate beyond these temperature limits, but long-term operation at elevated temperatures may reduce equipment life.

99

Description I/O pack internal power supply status not OK

Possible Cause The internal power supply that provides analog circuit control power is not operating correctly.

Solution

- Check the I/O pack ground quality through mounting bolts.
- Confirm that 28 V input power is within 26.6 - 29.4 V range.
- Replace the I/O pack.

100

Description Dither Time is frozen or out of range - [ ]

Possible Cause The time signal used to generate a dither on the valve output signal does not appear to being changing. This could cause a frozen valve.

Solution

- Cycle power to the I/O pack.
- Replace the I/O pack.

101

Description I/O pack internal reference voltage out of limits

Possible Cause The calibration reference voltage for the analog inputs is more than ±5% from the expected value, indicating a hardware failure.

Solution

- Check the I/O pack ground quality through mounting bolts.
- Cycle power to the I/O pack.
- Replace the I/O pack.

102

Description I/O pack internal null voltage out of limits

Possible Cause The calibration Null voltage for the analog inputs is more than ±5% from the expected value, indicating a hardware failure.

Solution

- Check the I/O pack ground quality through mounting bolts.
- Cycle power to the I/O pack.
- Replace the I/O pack.

128

Description Logic Signal [ ] Voting Mismatch

Possible Cause N/A

Solution N/A

224-235

Description Input Signal [ ] Voting Mismatch, Local=[ ], Voted=[ ]

Possible Cause

- Voter disagreement between the R, S and T I/O packs
- I/O pack is not seated correctly on the terminal board.

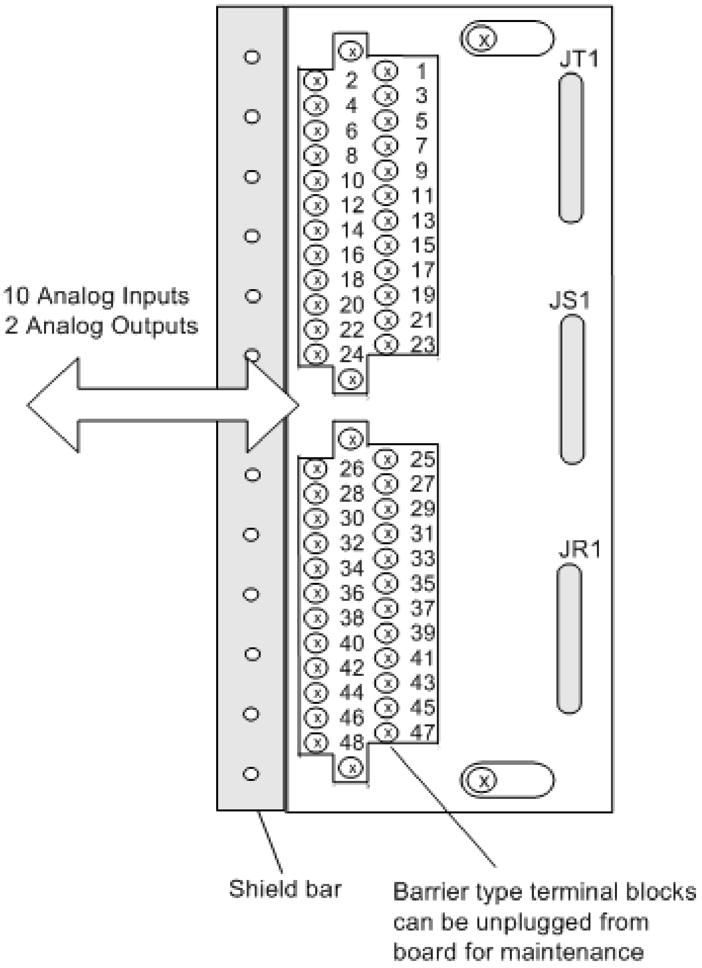
Solution

- Adjust the parameter *TMR_DiffLimt* or correct the cause of the difference.
- Re-seat the I/O pack to the terminal board.
- Replace the I/O pack.

2.4 TBAIH1C, TBAIS1C Analog Input/Output

The Analog Input/Output (TBAI) terminal board supports 10 analog inputs and 2 outputs. The 10 analog inputs accommodate two-wire, three-wire, four-wire, or externally powered transmitters. The analog outputs can be set up for 0-20 mA. With the Mark VIe PAICH2, there is also support for 0-200 mA current on the first output. Inputs and outputs have noise suppression circuitry to protect against surge and high frequency noise. The TBAI has three DC-37 pin connectors for TMR I/O packs. Simplex I/O redundancy is also supported using a single JR1 connection.

Note The TBAIS1C is IEC 61508 safety-certified when used with the Mark VIeS YAIC.



J ports

For simplex, connect I/O pack to JR1.
For TMR, use all three connectors.

With TMR I/O redundancy, the input signals are fanned to the three connectors for the R, S, and T I/O packs. TMR outputs combine the current of the three connected output drivers and determine the total current with a measuring shunt. TBAI then presents the total current signal to the I/O packs for regulation to the commanded setpoint.

Compatibility

Board Revision	Mark VIe IS220PAIC	Mark VIeS IS200YAIC	Comments
TBAIH1C	Yes	No	Current production
TBAIS1C	Yes	Yes	IEC 61508 safety certified with YAIC

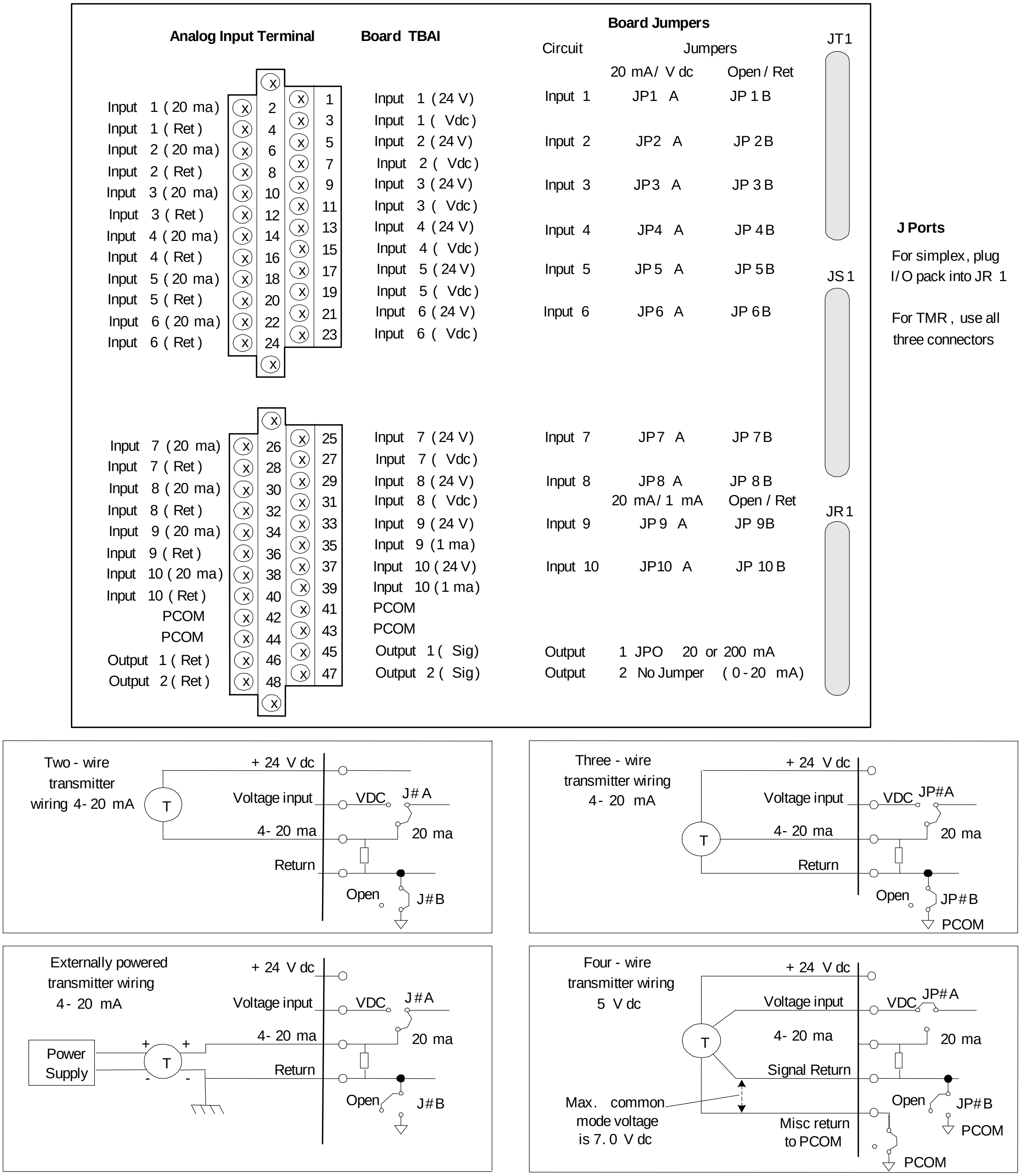
2.4.1 Installation

Connect the input and output wires directly to two I/O terminal blocks mounted on the terminal board. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield terminal attachment point is located adjacent to each terminal block.

TBAI can accommodate the following analog I/O types:

- Analog input, two-wire transmitter
- Analog input, three-wire transmitter
- Analog input, four-wire transmitter
- Analog input, externally powered transmitter
- Analog input, voltage ±5 V, ±10 V dc
- Analog input, current 4-20 mA
- Analog output, 0-20 mA
- Only with Mark VIe PAICH2: Analog output, 0-200 mA

The following figure displays the wiring connections, jumper positions, and cable connections for TBAI.



2.4.2 Operation

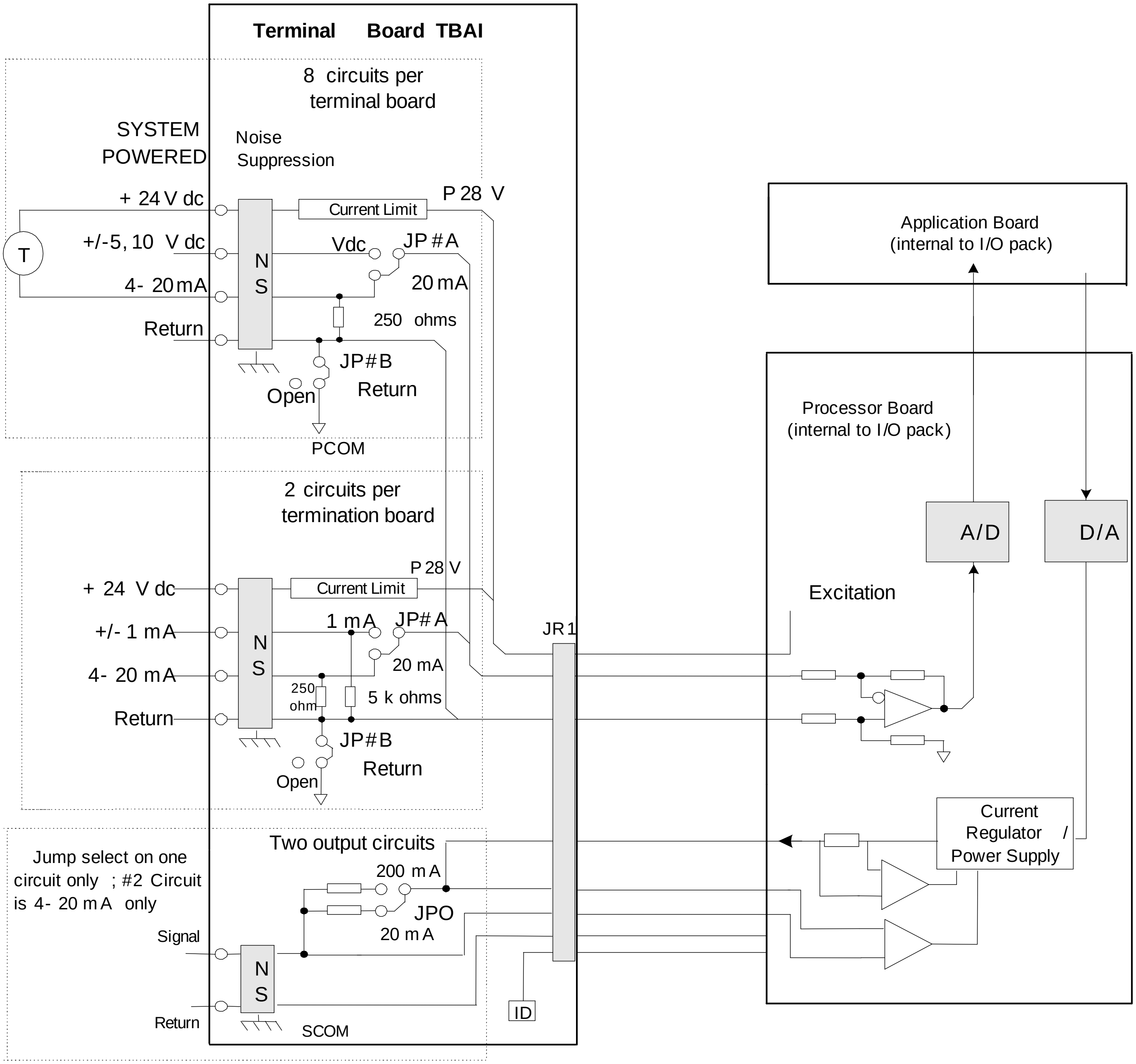
TBAI provides a 24 V dc power source for all the transducers. The inputs can be configured as current or voltage inputs using jumpers (JP#A and JP#B). One of the two analog output circuits is 4-20 mA and the other can be configured as 4-20 mA or (with Mark VIe PAICH2) 0-200 mA.

TBAI Analog I/O Capacity

Input Quantity	Analog Input Types	Output Quantity	Analog Output Types
8	±10 V dc, or ±5 V dc, or 4-20 mA	1	0-20 mA or 0-200 mA option only with Mark VIe PAICH2
2	4-20 mA, or ±1 mA	1	0-20 mA

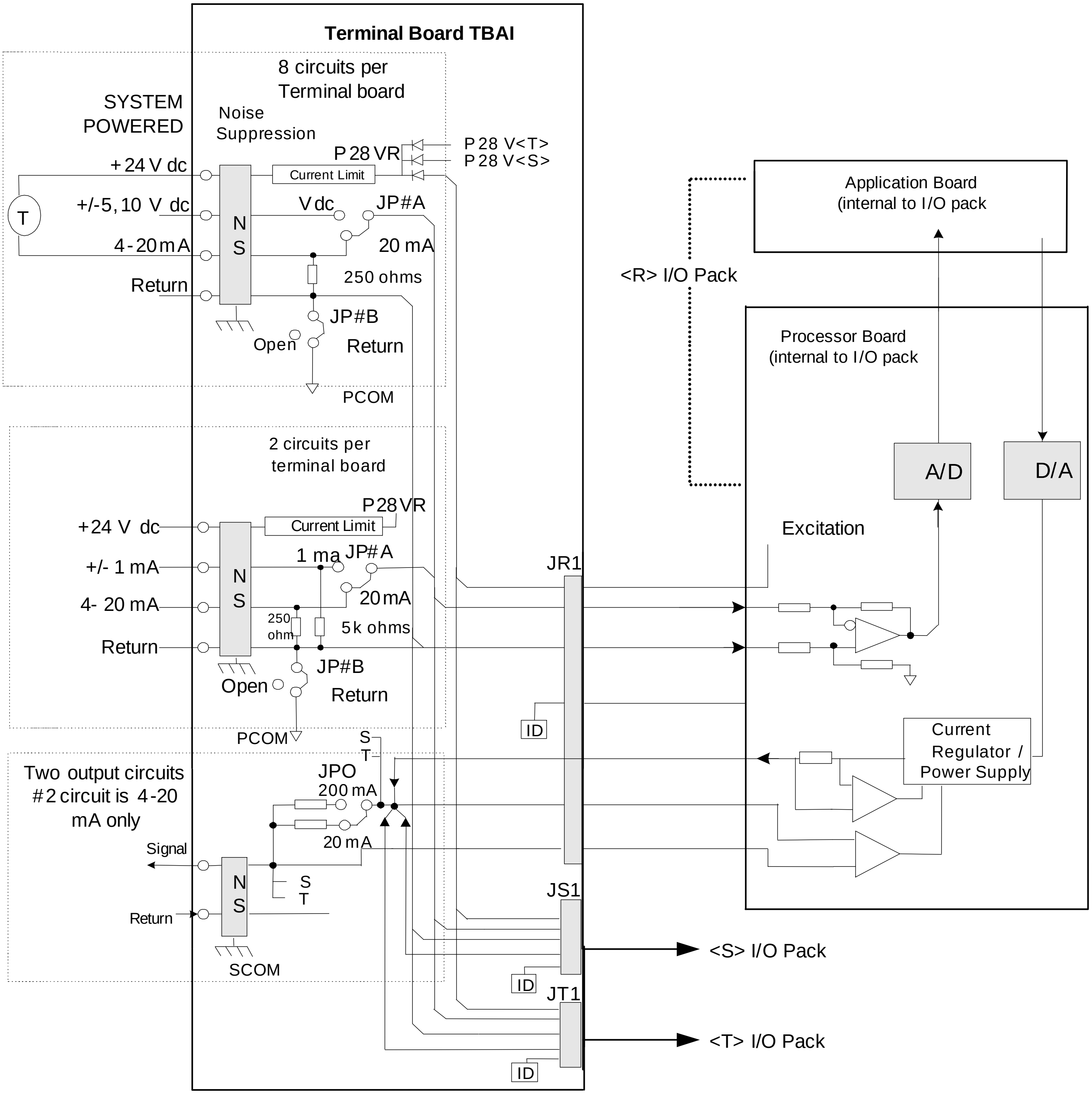
Note With noise suppression and filtering, the input ac CMR is 60 dB, and the dc CMR is 80 dB.

Each 24 V dc power output is rated to deliver 21 mA continuously and is protected against operation into a short circuit. Transmitters/transducers can be powered by the 24 V dc source in the control system, or can be independently powered. Jumper JPO selects the type of current output. Diagnostics monitor each output, and a suicide relay in the I/O pack disconnects the corresponding output if a fault cannot be cleared by a command from the processor.



Simplex Analog Inputs and Outputs

In a TMR system, analog inputs fan out to the three I/O packs. The 24 V dc power to the transducers also comes from all three I/O packs and is diode shared on TBAI. Each analog current output is fed by currents from all three I/O packs. The actual output current is measured with a series resistor, which feeds a voltage back to each I/O pack. The resulting output is the voted middle value (median) of the three currents. The following figure displays TBAI in a TMR system.



TMR Analog Inputs and Outputs

2.4.3 Specifications

Item	TBAI Specification
Number of channels	12 channels with 10 Analog Inputs (AI) and 2 Analog Outputs (AO)
AI types supported	Inputs 1 to 8: ±5 V dc, ±10 V dc, or 4–20 mA Inputs 9 to 10: 4–20 mA or ±1 mA
Input accuracy	±0.1% of full scale over the full operating temperature range
Outputs	24 V outputs provide 21 mA each connection
Maximum lead resistance	15 Ω maximum two-way cable resistance, cable length up to 300 m (984 ft)
Output load	800 Ω max for 4-20 mA output Only available with Mark VIe PAICH2: 50 Ω max for 200 mA output
Fault detection	Monitor total output current Check connector ID chip for hardware incompatibility
Size	10.16 cm wide x 33.02 cm high (4.0 in x 13 in)

2.4.4 TBAI Diagnostics

Diagnostic tests are made on the terminal board as follows:

- The terminal board provides the voltage drop across a series resistor to indicate the output current. The I/O pack creates a diagnostic alarm (fault) if either of the two outputs goes unhealthy.
- Each cable connector on the terminal board has its own ID device that is interrogated by the I/O pack. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the JR, JS, JT connector location. When this chip is read by the I/O pack and a mismatch is encountered, a hardware incompatibility fault is created.

2.4.5 TBAI Jumper Configuration

The terminal board is configured by jumpers. For the location of these jumpers, refer to the installation diagram. The jumper choices are as follows:

- Jumpers JP1A through JP8A select either current input or voltage input.
- Jumpers JP1B through JP8B select whether the return is connected to common or is left open.
- Jumpers JP9A and JP10A select either 1 mA or 20 mA input current.
- Jumpers JP9B and JP10B select whether the return is connected to common or is left open.
- Jumper JPO sets output 1 to either 20 mA or (only with Mark VIe PAICH2: 200 mA).

2.5 STAIH#A, S#A Simplex Analog Input

The Simplex Analog Input (STAI) terminal board is a compact analog input terminal board that accepts 10 analog inputs and two analog outputs, and connects to the pack. The 10 analog inputs accommodate two-wire, three-wire, four-wire, or externally powered transmitters. The two analog outputs are 0-20 mA. Only with the Mark VIe PAICH2, one analog output jumper can be configured to 0-200 mA current. High-density Euro style box terminal blocks are used. An on-board ID chip identifies the board to the pack for system diagnostic purposes.

Compatibility

Board Revision	Mark VIe PAIC	Mark VIeS YAIC	Comments
STAIH1A	Yes	No	Fixed terminals
STAIH2A	Yes	No	Plug in terminals
STAIS1A	Yes	Yes	Fixed terminals, IEC 61508 safety certified with YAIC
STAIS2A	Yes	Yes	Plug in terminals, IEC 61508 safety certified with YAIC
STAIS3A	No	Yes	No terminal block

2.5.1 Installation

The STAI plus a plastic insulator mounts on a sheet metal carrier that then mounts on a DIN-rail. Optionally, the STAI plus insulator mounts on a sheet metal assembly and then bolts directly to a cabinet. There are three types of terminals available as follows:

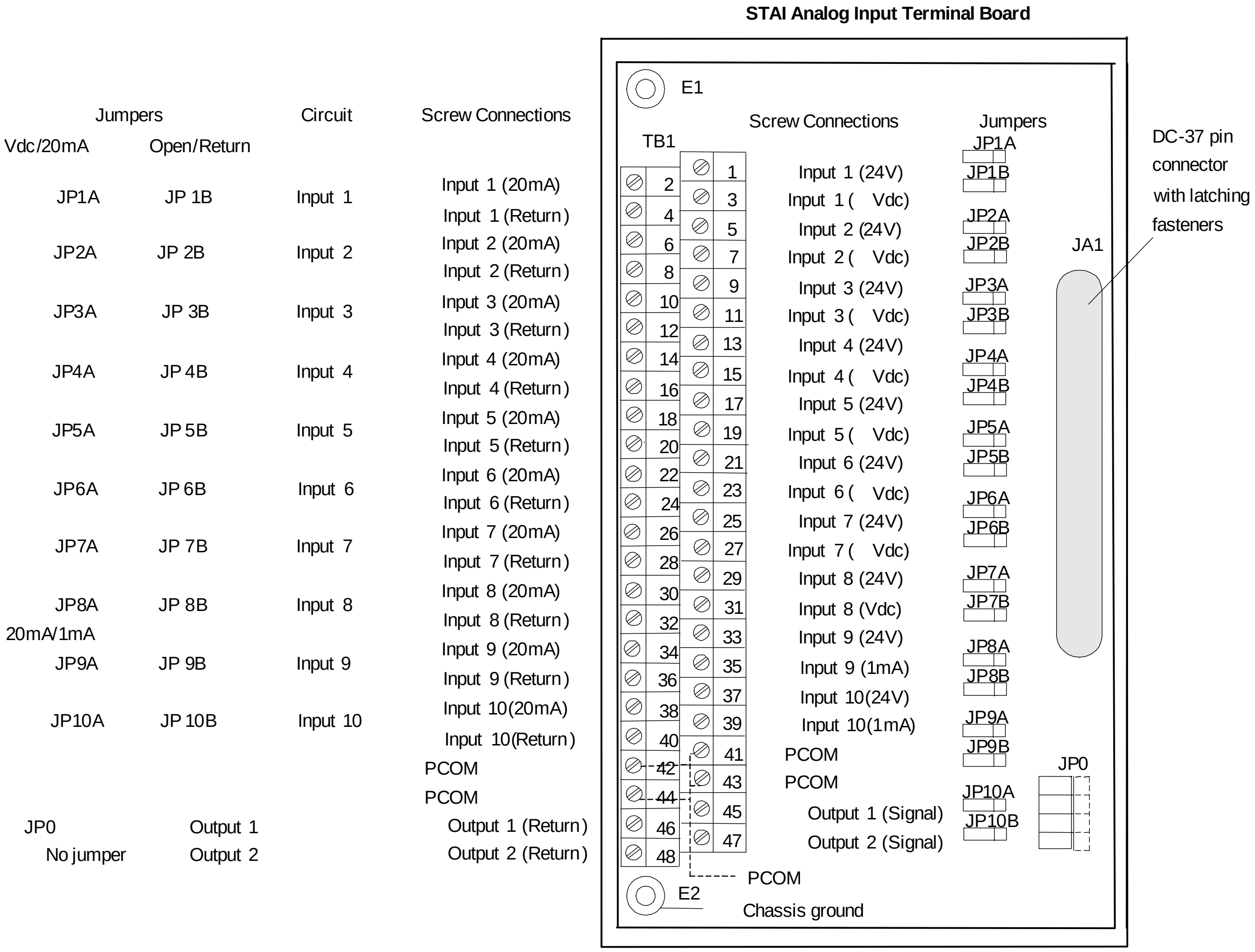
- STAI_1A has a permanently mounted Euro-style terminal block with 48 terminals.
- STAI_2A has a right angle header accepting a range of commercially available pluggable Euro-style terminal blocks, with a total of 48 terminals.
- STAI_3A does not have any terminal block, allowing for field wiring to be directly soldered to the board.

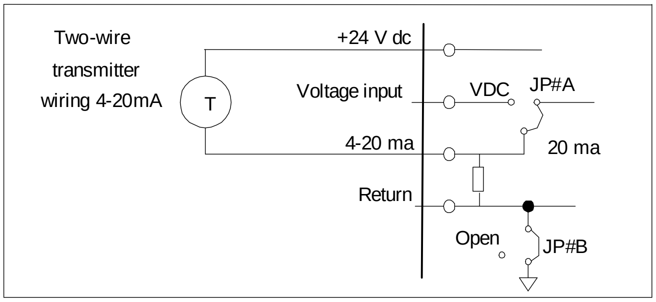
Note Typically #18 AWG wires (shielded twisted pair) are used. I/O cable shield terminal is provided adjacent to the terminal blocks.

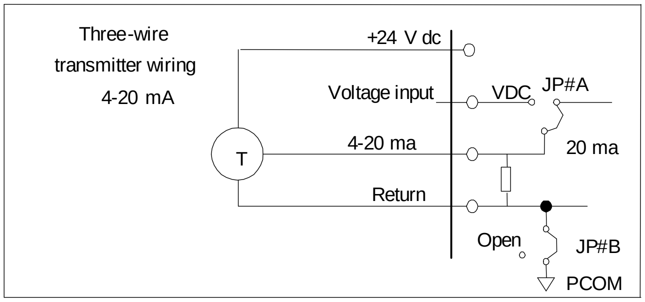
The following types of analog inputs and outputs can be accommodated:

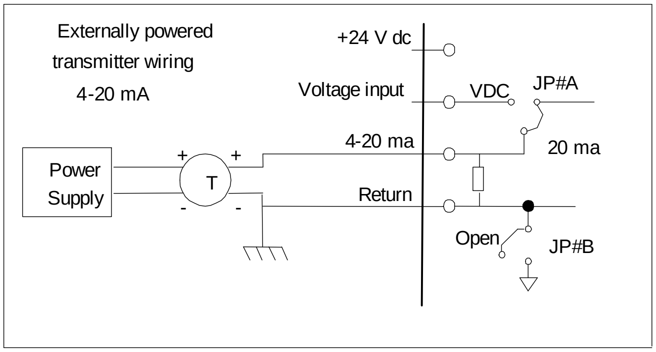
- Analog input, two-wire transmitter
- Analog input, three-wire transmitter
- Analog input, four-wire transmitter
- Analog input, externally powered transmitter
- Analog input, voltage ±5 V, ±10 V dc
- Analog input, current 4-20 mA
- Two analog outputs, 0-20 mA current
- Only with the Mark VIe PAICH2: one analog output, 0-200 mA current

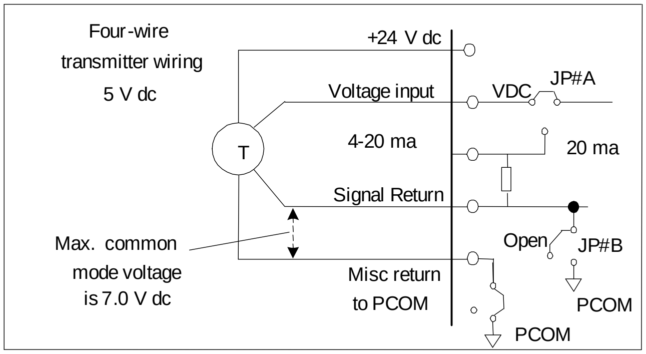
Wiring, jumper positions, and cable connections display on the wiring diagram.


STAI Analog Input Terminal Board









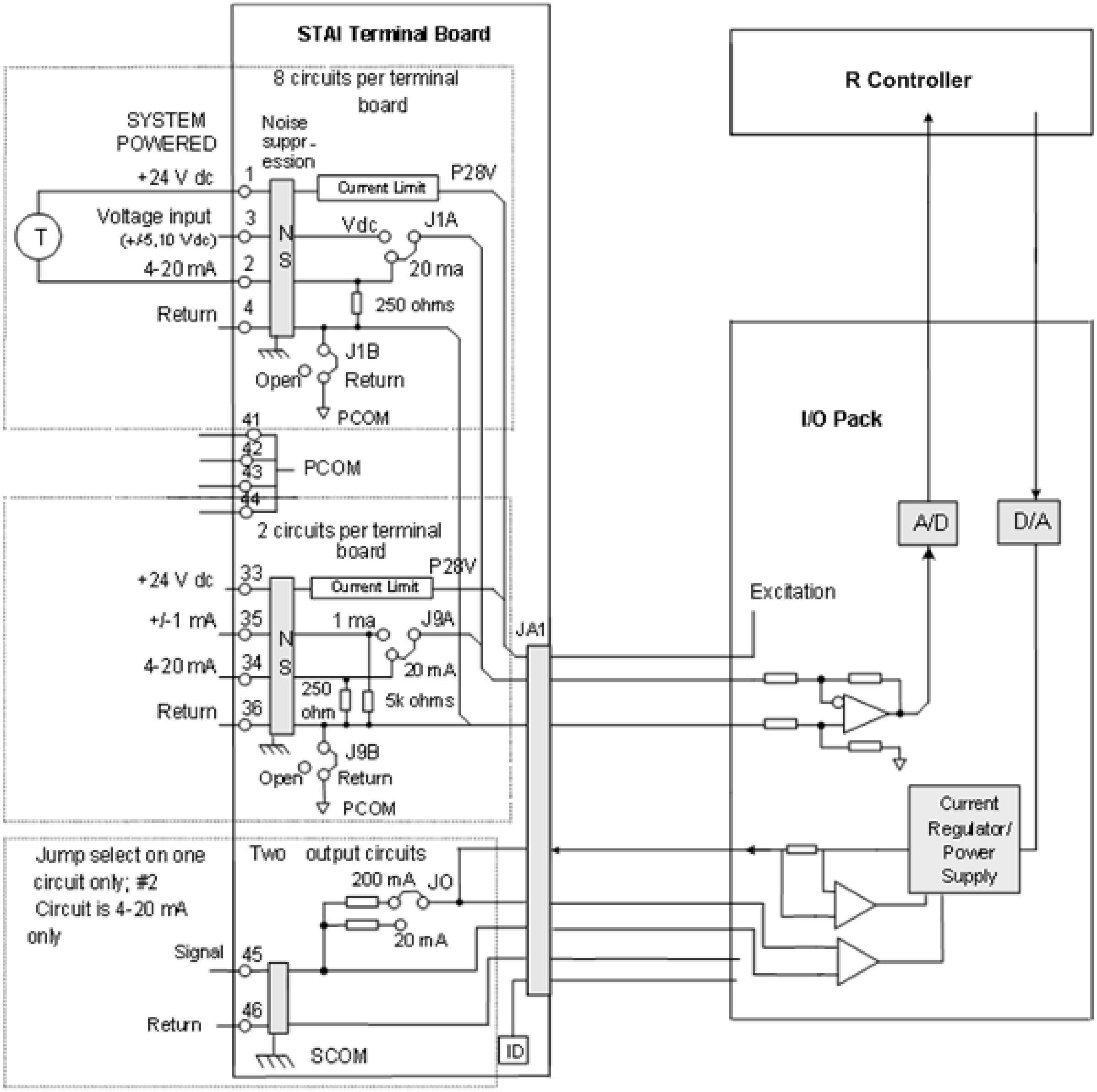
2.5.2 Operation

24 V dc power is available on the terminal board for all the transmitters (transducers). There is a choice of current or voltage inputs using jumpers. One of the two analog output circuits is 4-20 mA, and the other can be jumper configured for 4-20 mA or 0-200 mA (only with the Mark VIe PAICH2).

Note The 200 mA output is not supported by the Mark VIeS YAIC.

The following table displays the analog input/output capacity of the STAI terminal board.

Quantity Inputs	Analog Input Types	Quantity Outputs	Analog Output Types
8	±10 V dc, or ±5 V dc, or 4-20 mA	1	4-20 mA or 0-200 mA (only with the Mark VIe PAICH2)
2	4-20 mA, or ±1 mA	1	0-20 mA



2.5.3 Specifications

Item	STAI Specification
Number of channels	12 channels with 10 Analog Inputs (AI) and 2 Analog Outputs (AO)
AI types supported	Inputs 1 to 8: ±5 V dc, ±10 V dc, or 4–20 mA Inputs 9 to 10: 4–20 mA or ±1 mA
Input accuracy	±0.1% of full scale over the full operating temperature range
Maximum lead resistance	15 Ω maximum two-way cable resistance, cable length up to 300 m (984 ft).
Outputs	24 V dc outputs rated at 21 mA each
Load on output currents	800 Ω max burden for 4-20 mA output Only with Mark VIe PAICH2: 50 Ω max burden for 200 mA output
Size	15.9 cm high x 10.2 cm wide (6.25 in x 4.0 in)
Technology	Surface mount

2.5.4 Diagnostics

Diagnostic tests are made on the terminal board as follows:

- The board provides the voltage drop across a series resistor to indicate the output current. The I/O pack creates a diagnostic alarm (fault) if any one of the eight outputs goes unhealthy.
- Each cable connector on the terminal board has its own ID device that is interrogated by the I/O pack. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the JR, JS, JT connector location. When this chip is read by the I/O pack and a mismatch is encountered, a hardware incompatibility fault is created.

2.5.5 Jumper Configuration

The terminal board is configured by jumpers. For the location of these jumpers, refer to the installation diagram. The jumper choices are as follows:

- Jumpers JP1A through JP8A select either current input or voltage input.
- Jumpers JP1B through JP8B select whether the return is connected to common or is left open.
- Jumpers JP9A and JP10A select either 1 mA or 20 mA input current.
- Jumpers JP9B and JP10B select whether the return is connected to common or is left open.
- Jumper JP0 sets output 1 to either 20 mA or 0-200 mA (only with the Mark VIe PAICH2)

2.6 SAIIH#A Simplex Isolated Analog Input

The Simplex Analog Input (SAII) terminal board is a compact analog input terminal board that accepts 10 analog inputs and offers two analog outputs, and connects to the Mark VIe PAIC. The I/O pack plugs into the D-type connector and communicates with the controller over Ethernet. The 10 analog inputs accommodate 2-wire, 3-wire, 4-wire, or externally powered transmitters.

Note The SAII terminal board is not compatible with the Mark VIeS YAIC.

Each analog input features point isolation when configured for externally powered devices. Each analog input has an isolator in the circuit with a rating of 1500 V rms. The two analog outputs are 0-20 mA but one can be jumper configured to 0-200 mA current when used with a PAICH2. High-density Euro-block type terminal blocks are used. An on-board ID chip identifies the SAII to the PAIC for system diagnostic purposes.

2.6.1 Installation

The SAII plus a plastic insulator mounts on a sheet metal carrier that then mounts on a DIN-rail. Optionally, the SAII plus insulator mounts on a sheet metal assembly and then bolts directly to a cabinet. There are two types of Euro-block terminal blocks available as follows:

- SAIIH1A has a permanently mounted terminal block with 48 terminals
- SAIIH2A has a right angle header accepting a range of commercially available pluggable terminal blocks, with a total of 48 terminals

2.6.1.1 Conductors

The Euro style box-type terminal blocks on SAII accept conductors with the following characteristics:

Type	Size
Conductor cross section solid min.	0.2 mm²
Conductor cross section solid max.	2.5 mm²
Conductor cross section stranded min.	0.2 mm²
Conductor cross section stranded max.	2.5 mm²
Conductor cross section stranded, with ferrule without plastic sleeve min.	0.25 mm²
Conductor cross section stranded, with ferrule without plastic sleeve max.	2.5 mm²
Conductor cross section stranded, with ferrule with plastic sleeve min.	0.25 mm²
Conductor cross section stranded, with ferrule with plastic sleeve max.	2.5 mm²
Conductor cross section AWG/kcmil min.	24 AWG
Conductor cross section AWG/kcmil max	12 AWG
2 conductors with same cross section, solid min.	0.2 mm²
2 conductors with same cross section, solid max.	1 mm²
2 conductors with same cross section, stranded min.	0.2 mm²
2 conductors with same cross section, stranded max.	1.5 mm²
2 conductors with same cross section, stranded, ferrules without plastic sleeve, min.	0.25 mm²
2 conductors with same cross section, stranded, ferrules without plastic sleeve, max.	1 mm²
2 conductors with same cross section, stranded, TWIN ferrules with plastic sleeve, min.	0.5 mm²
2 conductors with same cross section, stranded, TWIN ferrules with plastic sleeve, max.	1.5 mm²

2.6.1.2 SAII Terminal Screw Assignments

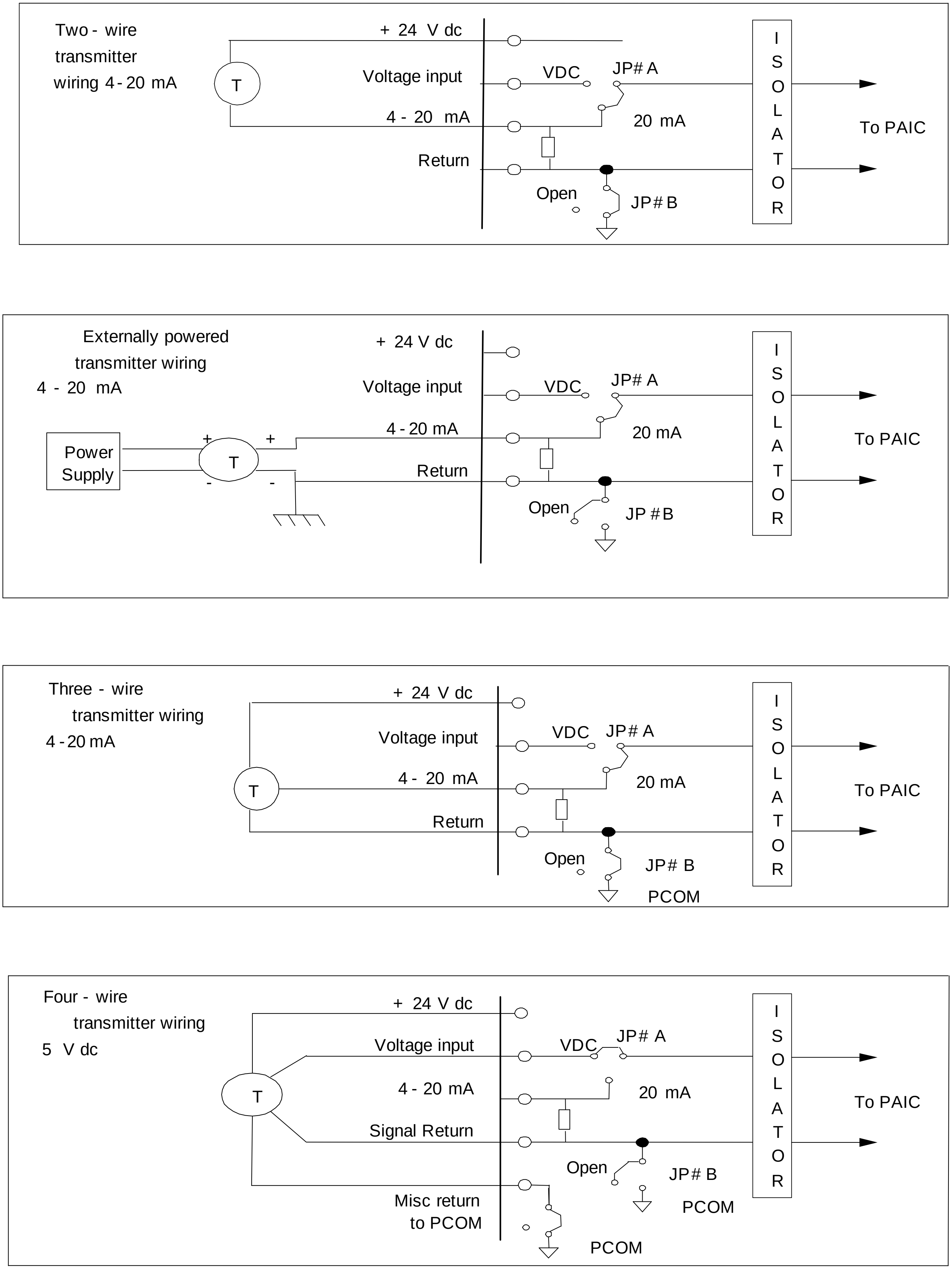
#	Name	#	Name
1	Input 1 (24 V)	25	Input 7 (24 V)
2	Input 1 (20 mA)	26	Input 7 (20 mA)
3	Input 1 (V dc)	27	Input 7 (V dc)
4	Input 1 (Return)	28	Input 7 (Return)
5	Input 2 (24 V)	29	Input 8 (24 V)
6	Input 2 (20 mA)	30	Input 8 (20 mA)
7	Input 2 (V dc)	31	Input 8 (V dc)
8	Input 2 (Return)	32	Input 8 (Return)
9	Input 3 (24 V)	33	Input 9 (24 V)
10	Input 3 (20 mA)	34	Input 9 (20 mA)
11	Input 3 (V dc)	35	Input 9 (1 mA)
12	Input 3 (Return)	36	Input 9 (Return)
13	Input 4 (24 V)	37	Input 10 (24 V)
14	Input 4 (20 mA)	38	Input 10 (20 mA)
15	Input 4 (V dc)	39	Input 10 (1 mA)
16	Input 4 (Return)	40	Input 10 (Return)
17	Input 5 (24 V)	41	PCOM
18	Input 5 (20 mA)	42	PCOM
19	Input 5 (V dc)	43	PCOM
20	Input 5 (Return)	44	PCOM
21	Input 6 (24 V)	45	Output 1 (Signal)
22	Input 6 (20 mA)	46	Output 1 (Return)
23	Input 6 (V dc)	47	Output 2 (Signal)
24	Input 6 (Return)	48	Output 2 (Return)

2.6.1.3 SAII Analog I/O Types

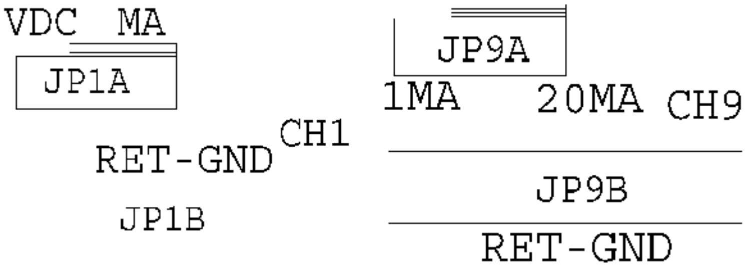
The following types of analog inputs and outputs can be accommodated:

- Analog input, two-wire transmitter
- Analog input, three-wire transmitter
- Analog input, four-wire transmitter
- Analog input, externally powered transmitter
- Analog input, voltage ±5 V, ±10 V dc
- Analog input, current 4-20 mA
- Analog output, 0-20 mA current
- Analog output, 0-200 mA current (with PAICH2)

Note Wiring options and jumper positions are displayed on the following wiring diagram.

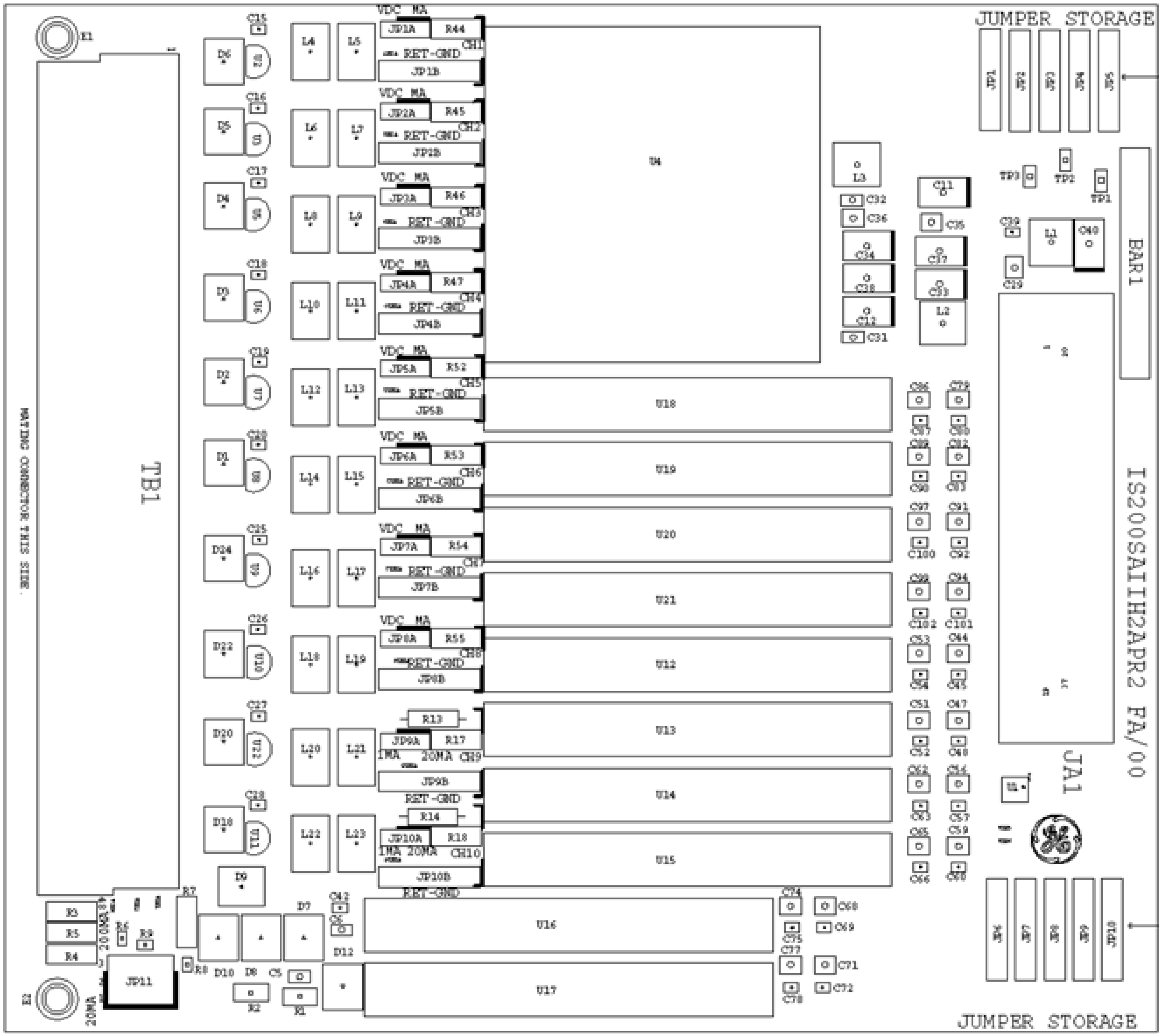


SAII Field Wiring Diagrams



SAII Jumper Details- Inputs 1-8 (Left) and Inputs 9-10 (Right)

The jumpers for inputs one through eight select between voltage and milliamp input (JP#A), and grounded or ungrounded operation (JP#B). Inputs 9 and 10 substitute a 1 mA input range for the voltage input option.



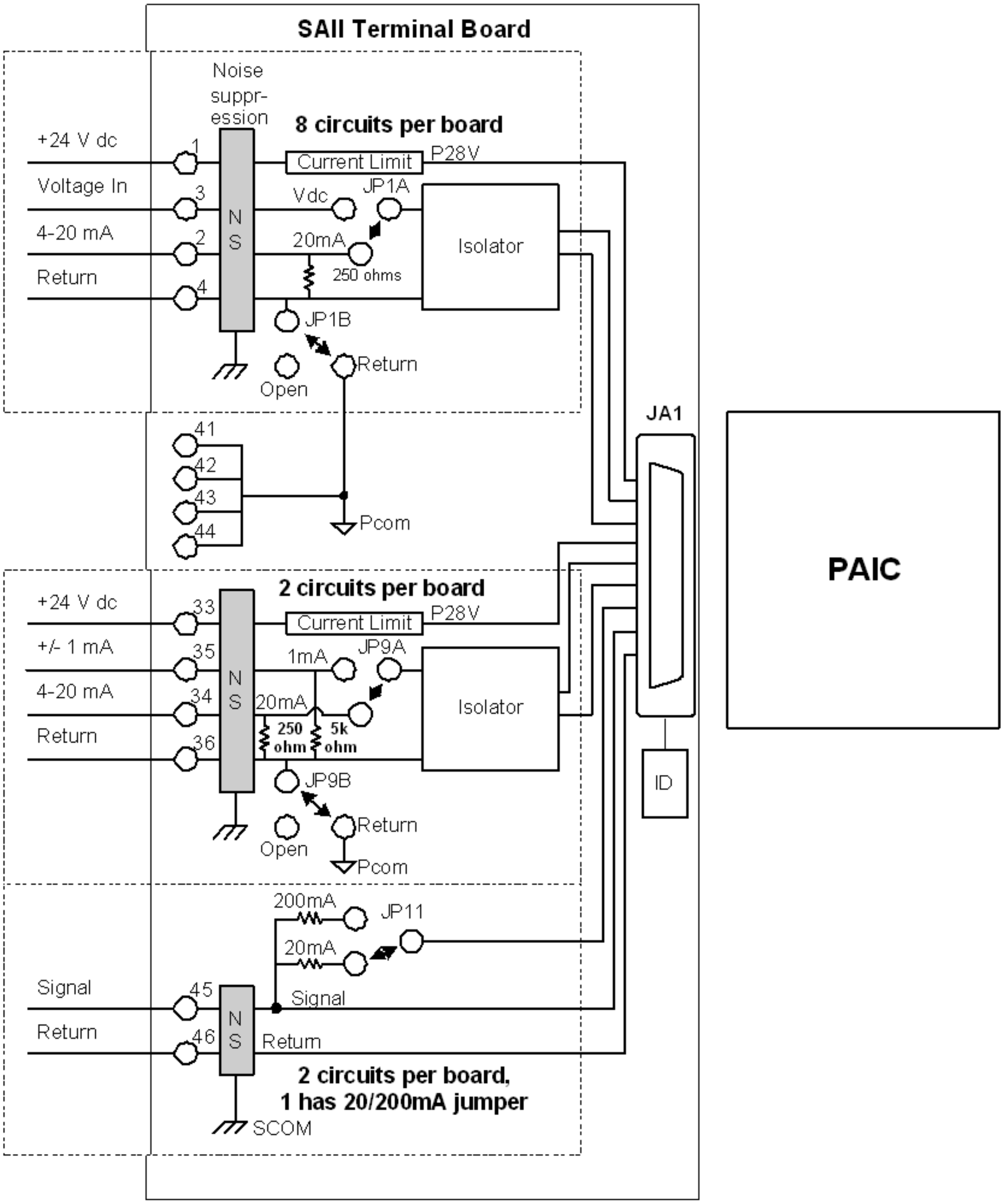
SAII Terminal Board

2.6.2 Operation

24 V dc power is available on the terminal board for all the transmitters (transducers). There is a choice of current or voltage inputs using jumpers. One of the two analog output circuits is 4-20 mA, and the other can be jumper configured for 4-20 mA or 0-200 mA (only with the Mark VIe PAICH2).

The following table displays the analog input/output capacity of the SAII terminal board.

Quantity Inputs	Analog Input Types	Quantity Outputs	Analog Output Types
8	±10 V dc, or ±5 V dc, or 4-20 mA†	1	0-20 mA or 0-200 mA (only with the Mark VIe PAICH2)
2	4-20 mA, or ±1 mA†	1	0-20 mA
† The input must be within the valid input range and not exceed more than 10% of the full scale value. For example, in a ±10 V input configuration the input cannot exceed ±11 V.			



SAII Terminal Board

2.6.3 Specifications

Item	SAII Specification
Number of channels	12 channels with 10 Analog Inputs (AI) and 2 Analog Outputs (AO)
AI types supported	Inputs 1 to 8: ±5 V dc, ±10 V dc, or 4–20 mA Inputs 9 to 10: 4–20 mA or ±1 mA
Maximum lead resistance	15 Ω maximum two-way cable resistance, cable length up to 300 m (984 ft).
Outputs	24 V dc outputs rated at 21 mA each
Load on output currents	800 Ω max burden for 4-20 mA output with PAIC pack 50 Ω max burden for 200 mA output (only with PAICH2)
Input accuracy	Typical accuracy ±0.15% Worst case accuracy ±0.4% Point isolation introduces an additional 0.3% error to analog inputs and so PAIC/SAII total accuracy is ±0.4% of full scale over the operating temperature range.
Isolation	Each analog input is isolated with rating of 1500 V rms
Maximum input range	The input must be within the valid input range and not exceed more than 10% of the full scale value. For example, in a ±10 V input configuration the input cannot exceed ±11 V.
Size	15.9 cm high x 17.8 cm wide (6.25 in x 7.0 in)
Technology	Surface mount

2.6.4 Diagnostics

Diagnostic tests are made on the terminal board as follows:

- The board provides the voltage drop across a series resistor to indicate the output current. The I/O processor creates a diagnostic alarm (fault) if any one of the two outputs goes unhealthy.
- The PAIC connector on the terminal board has its own ID device that is interrogated by the I/O controller. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the JR, JS, JT connector location. When this chip is read by the I/O controller and a mismatch is encountered, a hardware incompatibility fault is created.

2.6.5 Jumper Configuration

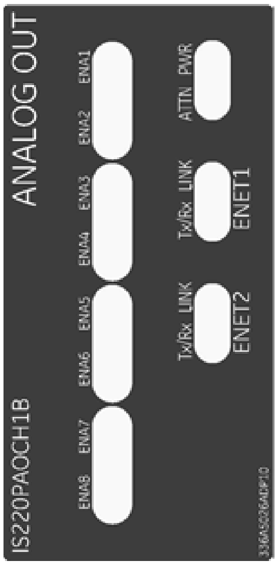
Jumpers configure the terminal board. The JP1B through JP10B jumpers determine the common connection, and provide ample voltage clearance to preserve isolation voltage rating when they are removed. For convenience, the SAII board provides storage locations for jumpers that are not providing a path to common. The jumper choices are as follows:

- Jumpers JP1A through JP8A select either current input or voltage input.
- Jumpers JP9A and JP10A select either 1 mA or 20 mA input current.
- Jumpers JP1B through JP10B select whether the return is connected to common or is left open. When any of the JP1B to JP10B is in place and the return is connected to common, then that respective channel will not be point isolated.
- Jumper JP11 sets output 1 to either 20 mA or 200 mA when used with PAICH2.

Note For the location of these jumpers, refer to the section *Analog Inputs and Outputs*.

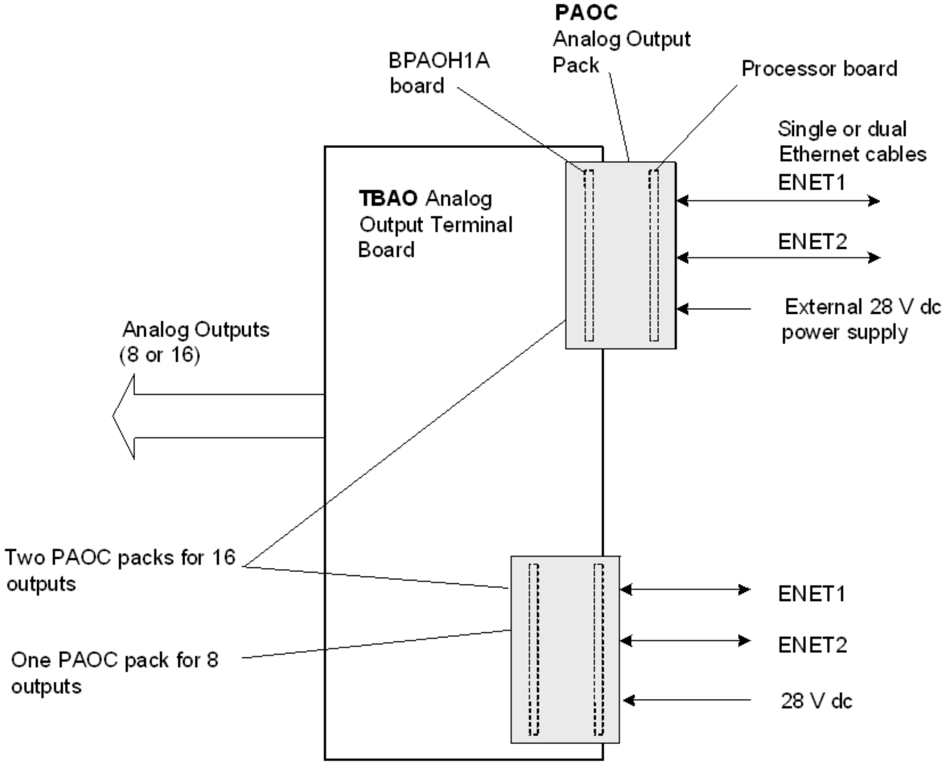
3 PAOC Analog Output Module

3.1 PAOC Analog Output Pack



The Analog Output (PAOC) provides the electrical interface between one or two I/O Ethernet networks and an analog output terminal board. The PAOC contains a BPPx processor board and an acquisition board pair specific to the analog output function. The PAOC is capable of providing up to eight simplex 0-20 mA current loop outputs and includes an analog to digital converter for current feedback from each output.

Input to the PAOC is through dual RJ-45 Ethernet connectors and a three-pin power input. Output is through a DC-37 pin connector that connects directly with the associated terminal board connector. Visual diagnostics are provided through indicator LEDs.



3.1.1 Compatibility

The PAOC I/O pack includes one of the following compatible BPPx processor boards:

- The PAOCH1A contains a BPPB processor board.
- The PAOCH1B contains a functionally compatible BPPC that is supported in the ControlST* software suite V04.06 and later.

The PAOC is only compatible with the analog output terminal boards TBAOH1C and STAOH1A/H2A as listed in the following table.

Terminal Board	Redundancy	# of I/O Packs	# of Analog Outputs
TBAOH1C	Simplex only	2	16
STAOH1A/H2A	Simplex only	1	8

3.1.2 Installation

➢ **To install the PAOC I/O pack**

1. Securely mount the desired terminal board.
2. Directly plug the PAOC I/O pack(s) into the terminal board connector(s).
3. Mechanically secure the I/O pack(s) using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right-angle force applied to the DC-37 pin connector between the I/O pack and the terminal board. The adjustment should only be required once in the service life of the product.

Note The PAOC mounts directly to the terminal board DC-37 pin connector(s). The PAOC is a simplex-only I/O pack.

4. Plug in one or two Ethernet cables depending on the system configuration. The I/O pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
5. Apply power to the I/O pack by plugging in the connector on the side of the PAOC. It is not necessary to remove power from the cable before plugging it in because the I/O pack has inherent soft-start capability that controls current inrush on power application.
6. Use the ToolboxST* application to configure the I/O pack as necessary. From the Component Editor, press F1 for help.

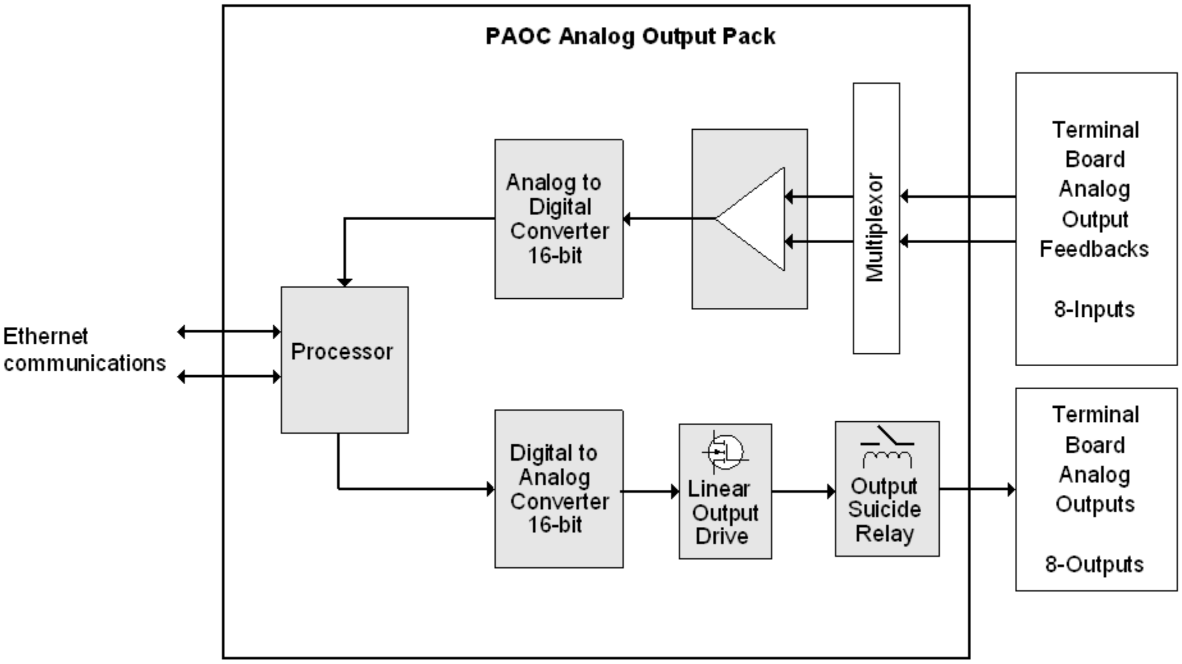
3.1.3 Operation

The following features are common to the distributed I/O modules:

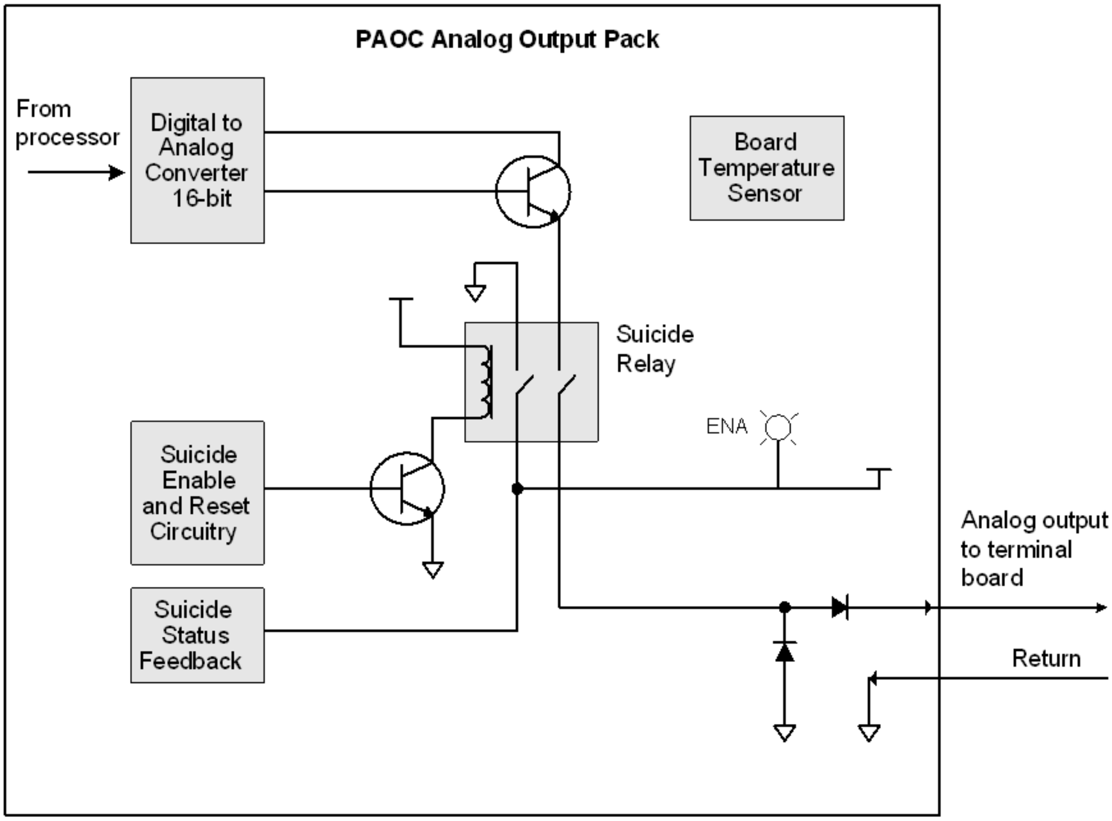
- *BPPx Processor*
- *Processor LEDs*
- *Power Management*
- *ID Line*
- *I/O Module Common Diagnostic Alarms*

3.1.3.1 Analog Output Hardware

The PAOC includes eight simplex 0-20 mA analog outputs capable of 18 V compliance. A 16-bit digital-to-analog converter (DAC) commands and drives the output current with an external transistor amplifier. A board temperature sensor is included to warn the control if the pack's internal temperature becomes excessive.

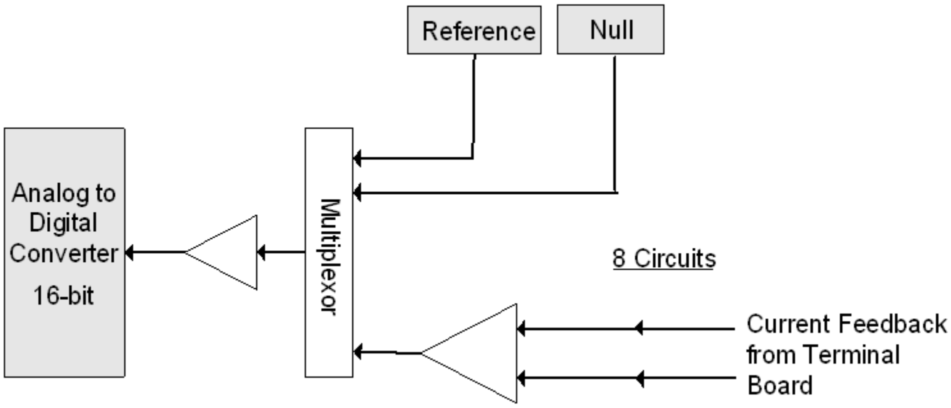

PAOC Analog Output Pack
Ethernet communications
Processor
Analog to Digital Converter 16-bit
Multiplexor
Terminal Board Analog Output Feedbacks
8-Inputs
Digital to Analog Converter 16-bit
Linear Output Drive
Output Suicide Relay
Terminal Board Analog Outputs
8-Outputs

Each analog output circuit also includes a normally open mechanical relay to enable or disable operation of the output. When the disable relay is de-activated, the output opens through the relay, open-circuiting that PAOC's analog output from the customer load that is connected to the terminal board. The mechanical relay's second normally-open contact is used as a status signal to indicate position of the relay with an LED.



3.1.3.2 Current Feedback Hardware

The PAOC includes current feedback monitoring for each of the eight simplex 0-20 mA analog outputs. A 50 Ω resistor on the terminal board and a 16-bit analog to digital converter is used to sense and monitor the output current.


Reference
Null
Analog to Digital Converter 16-bit
Multiplexor
8 Circuits
Current Feedback from Terminal Board

3.1.3.3 Thermal De-rating Guidelines

Note This is the I/O pack external temperature inside the cabinet, not cabinet external temperature.

With eight linear, high-compliance analog outputs, the PAOC I/O pack is subject to application limitations depending on its potential ambient environment. PAOCH1B packs are specified to have an operating temperature range of -40 to as high as 70ºC (-40 to 158 ºF), as measured external to the pack.

Depending on the application, and due to its dense triple board configuration, the PAOC's ambient environment maximum must be de-rated. The following is a list of output configurations and the appropriate de-rating that must be applied. The minimum output impedance is defined as the minimum series equivalent resistance of the customers load, as seen by the terminal board screws across the output range of 0-20 mA.

Maximum PAOCH1B I/O pack ambient temperature in degrees Celsius (degrees Fahrenheit) inside cabinet:

PAOCH1B Derating

Number of outputs	Minimum Output Resistance (per output, ohms)			
	0	250	500	1000
1	70º (158 ºF)	70º (158 ºF)	70º (158 ºF)	70º (158 ºF)
2	66º (151 ºF)	68º (154 ºF)	69º (156 ºF)	70º (158 ºF)
3	62º (144 ºF)	64º (147 ºF)	66º (151 ºF)	70º (158 ºF)
4	58º (136 ºF)	61º (142 ºF)	64º (147 ºF)	69º (156 ºF)
5	54º (129 ºF)	58º (136 ºF)	61º (142 ºF)	67º (153 ºF)
6	50º (122 ºF)	54º (129 ºF)	59º (138 ºF)	66º (151 ºF)
7	46º (115 ºF)	51º (124 ºF)	56º (133 ºF)	64º (147 ºF)
8	42º (108 ºF)	48º (118 ºF)	53º (127 ºF)	63º (145 ºF)

Maximum PAOCH1A I/O pack ambient temperature in degrees Celsius (degrees Fahrenheit) inside cabinet:

PAOCH1A Derating

Number of outputs	Minimum Output Resistance (per output, ohms)			
	0	250	500	1000
1	65º (149 ºF)	65º (149 ºF)	65º (149 ºF)	65º (149 ºF)
2	60º (140 ºF)	65º (149 ºF)	65º (149 ºF)	65º (149 ºF)
3	60º (140 ºF)	60º (140 ºF)	60º (140 ºF)	65º (149 ºF)
4	55º (131ºF)	60º (140 ºF)	60º (140 ºF)	65º (149 ºF)
5	55º (131 ºF)	55º (131 ºF)	60º (140 ºF)	60º (140 ºF)
6	50º (122 ºF)	55º (131 ºF)	55º (131 ºF)	60º (140 ºF)
7	50º (122 ºF)	50º (122 ºF)	55º (131 ºF)	60º (140 ºF)
8	45º (113 ºF)	50º (122 ºF)	55º (131 ºF)	55º (131 ºF)

3.1.3.4 Connectors

The I/O pack contains the following connectors:

- A DC-37 pin connector on the underside of the I/O pack connects directly to the Analog output terminal board. The connector contains the eight analog output signals, ID signal, and analog output feedback signals.
- An RJ-45 Ethernet connector named ENET1 on the side of the pack is the primary system interface.
- A second RJ-45 Ethernet connector named ENET2 on the side of the pack is the redundant or secondary system interface.
- A 3-pin power connector on the side of the I/O pack is for 28 V dc power for the I/O pack and terminal board.

3.1.4 Specifications

The following table provides information specific to the PAOC.

Item	Specification
Number of channels	Eight current output channels, single-ended (one side connected to common)
Analog outputs	0-20 mA, up to 900 Ω burden (18 V compliance) Response better than 50 rad/sec
Accuracy	±0.5% over -30 to 65ºC (-22 to 149 ºF) temperature and 0 to 900 Ω load impedance ±0.25% typical at 25ºC (77 ºF) and 500 Ω load
D/A converter resolution	16-bit resolution
Frame rate	100 Hz on all eight outputs
Size	8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in x 1.65 in x 4.78 in)
Technology	Surface mount
Ambient rating for enclosure design †	PAOCH1B is rated from -40 to as high as 70°C (-40 to 158°F). PAOCH1A is rated from -30 to as high as 65°C (-22 to 149°F). Follow the *Thermal De-rating Guidelines*.

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

3.1.5 Diagnostics

The PAOC I/O pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set
- Analog output current is sensed on the terminal board using a small burden resistor. The I/O pack conditions this signal and compares it to the commanded current to confirm health of the digital to analog converter circuits.
- The analog output suicide relay is continuously monitored for agreement between commanded state and feedback indication.

Details of the individual diagnostics are available from the ToolboxST application. The diagnostic signals can be individually latched, and then reset with the RSTDIAG signal if they go healthy.

3.1.6 Configuration

3.1.6.1 Outputs

Parameter	Description	Choices
AnalogOutput01 - AnalogOutput08	First of eight analog outputs - Board Point	Point Edit (Output FLOAT)
Output_MA	Output current, mA selection	Unused, 0-20 mA
Low_MA	Output mA at low value	0 to 20 mA
Low_Value	Output in engineering units at low mA	-3.4082e + 038 to 3.4028e + 038
High_MA	Output mA at high value	0 to 20 mA
High_Value	Output value in engineering units at high mA	-3.4082e + 038 to 3.4028e + 038
D/A_ErrLimit	DA error threshold in percent	0 to 100 %
Suicide_Enab	Suicide enable for faulty output	Enable, disable
OutputState	The state of the outputs when offline. When the PAOC loses communication with the controller, this parameter determines how it drives the outputs: PwrDownMode - Open the output relay and drive outputs to zero current HoldLastVal - Hold the last value received from the controller Output_Value - Go to the configured output value set by the parameter Output_Value	PwrDownMode, HoldLastVal, Output_Value
Output_Value	Pre-determined value for the outputs	
DitherAmpl	Dither in % current of scaled output mA	0 to 10
Dither_Freq	Dither rate in Hertz	Unused, 12.5, 25.033.33, 50.0, 100.0

3.1.6.2 Variables

Variable	Description	Direction Type
L3DIAG_PAOC	I/O diagnostic indication	Input BIT
LINK_OK_PAOC	I/O link okay indication	Input BIT
ATTN_PAOC	I/O attention indication	Input BIT
IOPackTmpr	I/O pack temperature	Input FLOAT
OutSuicide1	Status of suicide relay for output 1	Input BIT
↓	↓	Input BIT
Out1MA	Measure output current in mA	Input FLOAT
↓	↓	Input FLOAT

3.2 PAOC Specific Alarms

The following alarms are specific to the PAOC I/O pack.

32-39

Description Output [ ] feedback unhealthy

Possible Cause

- Analog output is being driven beyond the valid output range.
- Analog output feedback is out of range.
- Possible hardware failure in pack or terminal board

Solution

- Verify that the analog output command is within the range of 0-20mA.
- Verify that the analog output feedback matches the expected command.
- Verify analog output connections and field wiring.
- If all active analog output feedbacks are unhealthy with a valid command, a board failure is probable. Replace the I/O pack, replace the terminal board.

46-53

Description Output [ ] feedback current varies from reference current

Possible Cause

- **D/A_ErrLimit** is not configured properly (set too low)
- **DitherAmpl** is not configured properly
- Field wiring problem
- Open-circuit on output or total loop resistance is too high
- Possible hardware failure in pack

Solution

- Check the **D/A_ErrLimit** settings.
- Check the **DitherAmpl** settings.
- Check the field wiring and device.
- Replace the I/O pack.

54-61

Description Output [ ] feedback current is excessive

Possible Cause The analog output current feedback is greater than 30mA. This will typically cause the output to suicide.

- Field wiring problem
- Possible hardware failure in pack

Solution

- Verify the analog output connections and field wiring.
- Replace the I/O pack.

62-69

Description Output [ ] Suicide relay non-functional

Possible Cause The analog output suicide relay command doesn't match the feedback.

- Possible relay failure on the acquisition board
- Possible hardware failure in pack

Solution Replace the I/O pack.

70-77

Description Output [ ] Suicide Active

Possible Cause

- Suicide is enabled (**Suicide_Enab**) for analog output.
- Review any additional diagnostics for possible causes.
- Analog output current feedback is too high (30 mA).
- Field wiring problem
- Command is beyond the range of the output.

Solution

- Verify that the commanded output is within output range.
- Verify the analog output connections and field wiring.

78

Description Output Driver Temperature [ ] deg °F exceeds the max limit ([ ] deg °F)

Possible Cause The output driver temperature on the PAOC has exceeded the maximum temperature limit of:

- 194 °F (90°C) for PAOCH1B
- 185 °F (85°C) for PAOCH1A

Solution

- Review pack derating guidelines in help documentation.
- Environmental controls applied to the cabinet containing the I/O pack should be checked. Pack operation will continue correctly beyond these temperature limits but long-term operation at elevated temperatures may reduce equipment life.

79

Description Internal +15V Power Supply status Not OK

Possible Cause The internal power supply that provides analog circuit control power is not operating correctly.

Solution

- Check the I/O pack ground quality through mounting bolts.
- Confirm that the 28 V input power is within 26.6 - 29.4 V range.
- Replace the I/O pack.

80

Description Internal -15V Power Supply status Not OK

Possible Cause The internal power supply that provides analog circuit control power is not operating correctly.

Solution

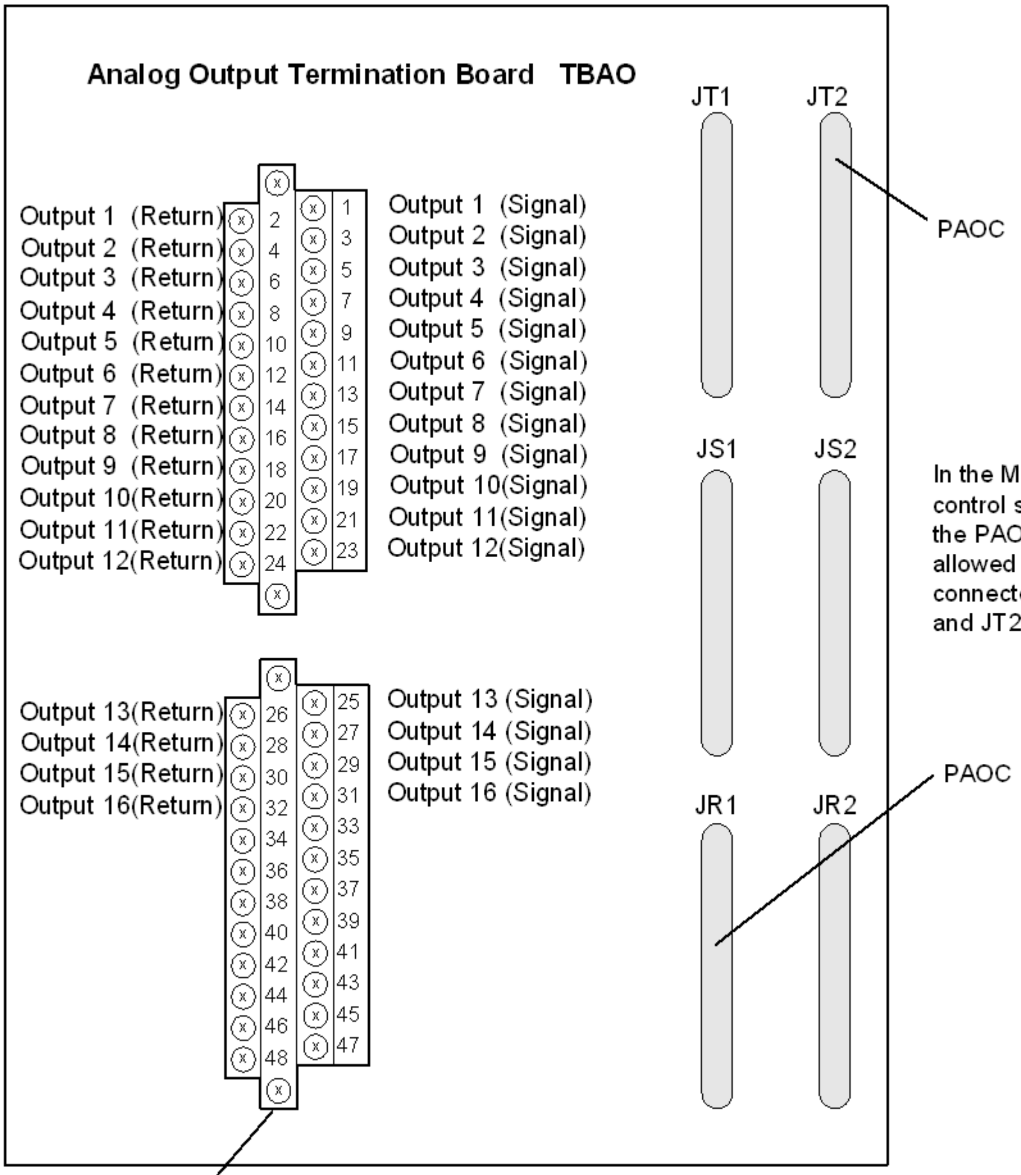
- Check the I/O pack ground quality through mounting bolts.
- Confirm that the 28 V input power is within 26.6 - 29.4 V range.
- Replace the I/O pack.

3.3 TBAOH1C Analog Output

The Analog Output (TBAO) terminal board supports 16 analog outputs with a current range of 0-20 mA. Current outputs are generated by the PAOC I/O pack. The outputs have noise suppression circuitry to protect against surge and high-frequency noise. The TBAO has two barrier-type terminal blocks for customer wiring and six D-type cable connectors.

3.3.1 Installation

Attach the TBAO to a vertical mounting plate. Connect the wires for the 16 analog outputs directly to the two I/O terminal blocks mounted on the left of the board. Each point can accept two 3.0 mm (#12AWG) wires with 300 V insulation per point using spade or ring type lugs. Each block is held down with two screws and has 24 terminals. A shield terminal strip attached to chassis ground is located immediately to the left of each terminal block. TBAOH1C works with PAOC I/O pack(s) and supports simplex applications only. The I/O pack(s) plug into the D-type connectors and communicate over IONet Ethernet with the Mark VIe controller. Special side mounting brackets support the I/O pack(s).



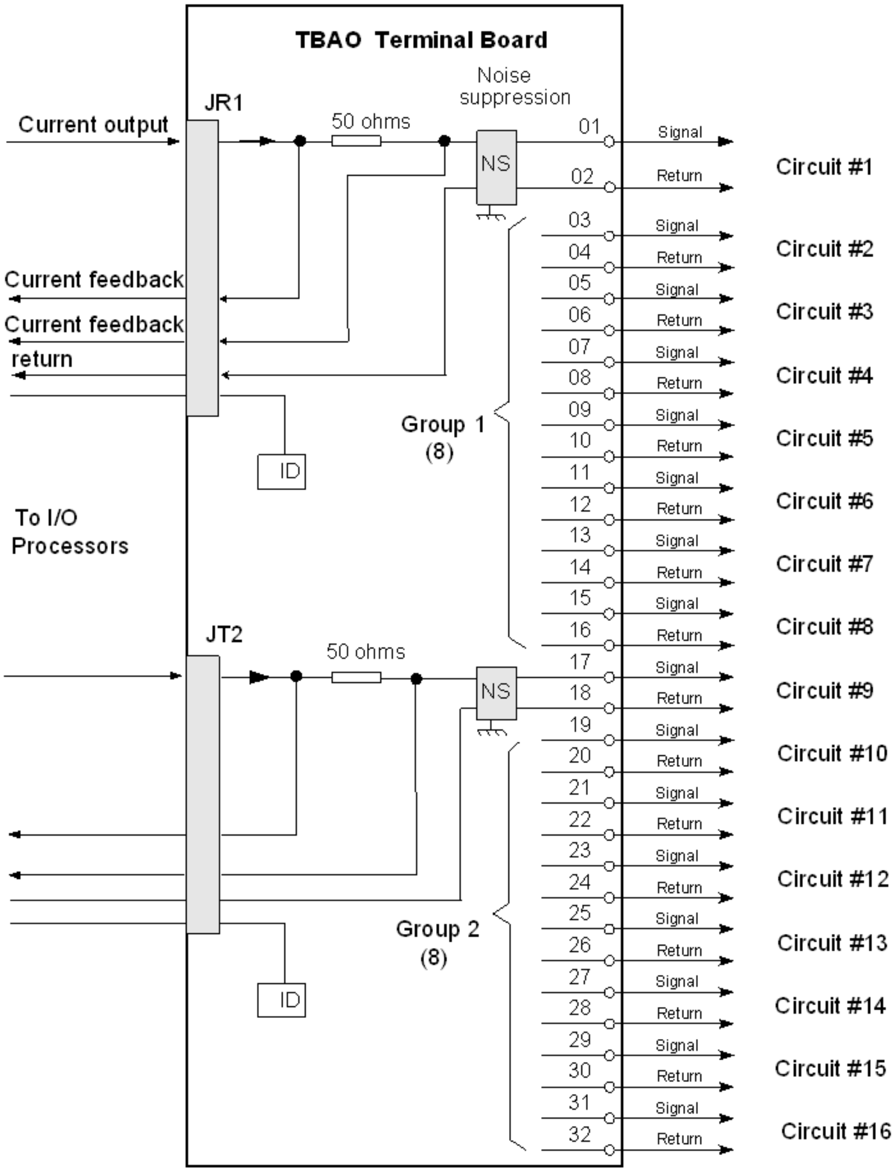
In the Mark VIe control system, the PAOC is allowed on connectors JR1 and JT2 only.

I/O Terminal block with barrier terminals
Terminal blocks can be unplugged from terminal board for maintenance

Up to two #12 AWG wires per point with 300 volt insulation

3.3.2 Operation

The TBAO supports 16 analog control outputs. Driven devices should not exceed a resistance of 900 Ω and can be located up to 300 m (984 ft) from the control cabinet. The PAOC contains the D/A converter and drivers that generate the controlled currents. The output current is measured by the voltage drop across a resistor on the terminal board. Filters reduce high-frequency noise and suppress surge on each output near the point of signal exit. The following figure displays TBAO in a simplex system.



Analog Outputs, Simplex

3.3.3 Specifications

Item	Specification
Number of channels	16 current output channels, single-ended (one side connected to common)
Analog output current	0-20 mA
Customer load resistance	Up to 900 Ω burden (18 V compliance) with PAOC and TBAOH1C
Size	10.16 cm wide x 33.02 cm high (4.0 in x 13.0 in)

3.3.4 Diagnostics

Diagnostic tests are made on the terminal board as follows:

- The board provides the voltage drop across a series resistor to indicate the output current. The I/O pack creates a diagnostic alarm (fault) if any one of the eight outputs goes unhealthy.
- Each cable connector on the terminal board has its own ID device that is interrogated by the I/O pack. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the JR, JS, JT connector location. When this chip is read by the I/O pack and a mismatch is encountered, a hardware incompatibility fault is created.

3.4 STAO Simplex Analog Output

3.4.1 Functional Description

The Simplex Analog Output (STAO) terminal board is a compact analog output terminal board, designed for DIN-rail or flat mounting. STAO has eight 0-20 mA analog outputs driven by the PAOC I/O pack. The on-board circuits and noise suppression are the same as those on TBAO terminal board. High-density Euro-block type terminal blocks are mounted on the board for wiring to the customer’s devices. An on-board ID chip identifies the board to the I/O processor for system diagnostic purposes. The I/O pack plugs into the D-type connector and communicates with the controller over Ethernet.

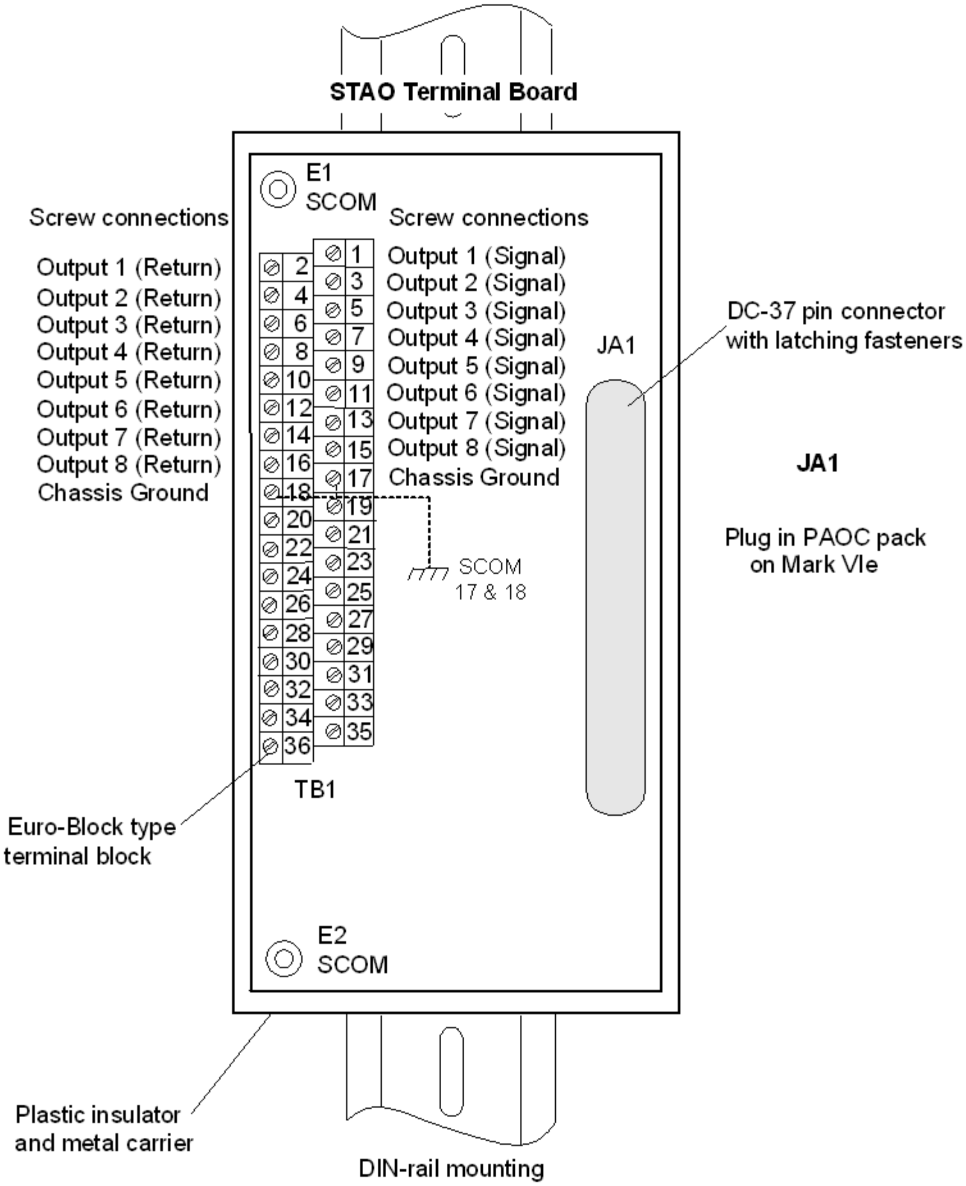
3.4.2 Installation

The STAO plus a plastic insulator mounts in a panel or on a sheet metal carrier that then mounts on a DIN-rail. Optionally, the STAO plus insulator mount on a sheet metal assembly that then bolts directly to a cabinet. Driven devices should not exceed a resistance of 900 Ω and can be located up to 300 m (984 ft) from the control cabinet. Two types of Euro-block terminal blocks are available:

- STAOH1 has a permanently mounted terminal block with 36 terminals.
- STAOH2 has a removable terminal block with 36 terminals.

Note There is no shield terminal strip with this design.

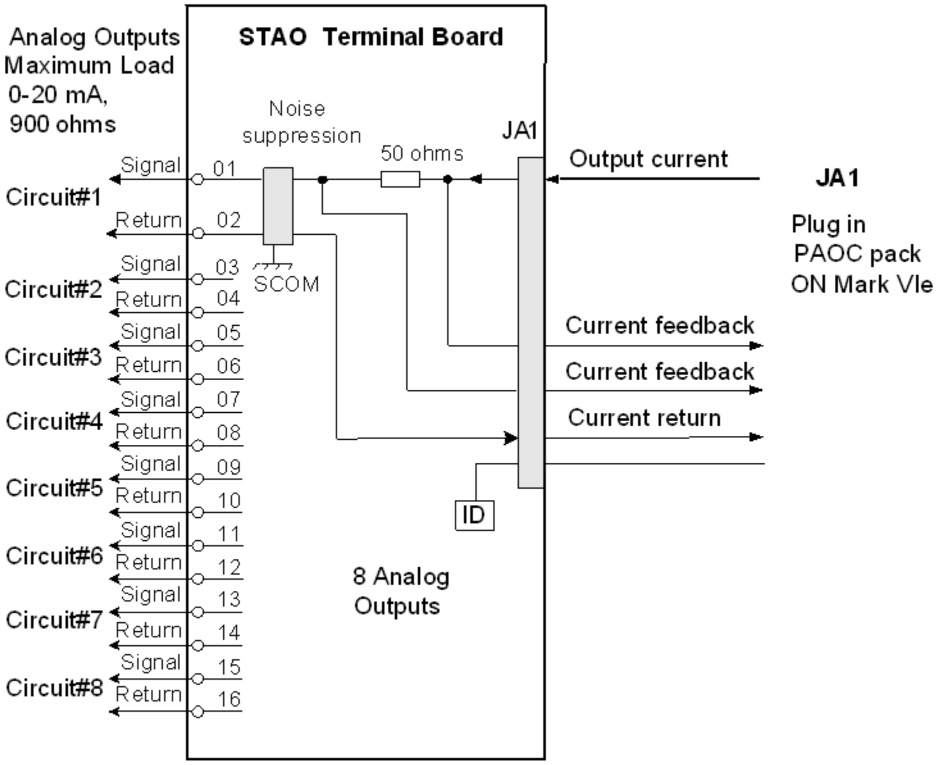
The eight analog outputs are wired directly to the terminal block as displayed in the following figure. There are two screws for the SCOM connection. Typically #18 AWG wires (shielded twisted pair) are used. I/O cable shield terminal uses an external mounting bracket supplied by GE or the customer. E1 and E2 are mounting holes for the chassis ground screw connection (SCOM). DIN-type terminal boards can be stacked vertically on the DIN-rail to conserve cabinet space.



STAO Wiring and Cabling

3.4.3 Operation

STAO supports eight analog control current outputs. On each output, the voltage drop across the local loop current sense resistor is measured and the signal is fed back to the I/O processor that controls the current. Filters reduce high-frequency noise and suppress surge on each output near the point of signal exit. The I/O processor contains the D/A converter and drivers that generate the controlled currents.



STAO Terminal Board

3.4.4 Specifications

Item	Specification
Number of channels	Eight current output channels, single-ended (one side connected to common)
Analog output current	0-20 mA
Customer load resistance	Up to 900 Ω burden with PAOC pack
Size	15.9 cm high x 10.2 cm wide (6.25 in x 4.0 in)
Technology	Surface mount

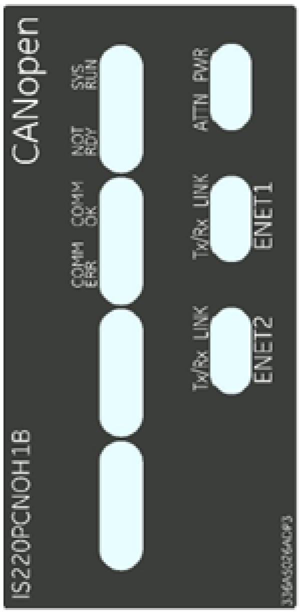
3.4.5 Diagnostics

Diagnostic tests are made on the terminal board as follows:

- The board provides the voltage drop across a series resistor to indicate the output current. The I/O pack creates a diagnostic alarm (fault) if any one of the eight outputs goes unhealthy.
- Each cable connector on the terminal board has its own ID device that is interrogated by the I/O pack. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the JR, JS, JT connector location. When this chip is read by the I/O pack and a mismatch is encountered, a hardware incompatibility fault is created.

4 PCNO CANopen® Master Gateway

4.1 PCNO CANopen Gateway I/O Pack



The CANopen I/O pack (PCNO) is a network management master that maps I/O from CANopen devices to Mark* VIe controllers on the IONet.

Only the following devices are currently supported on the PCNO CANopen network:

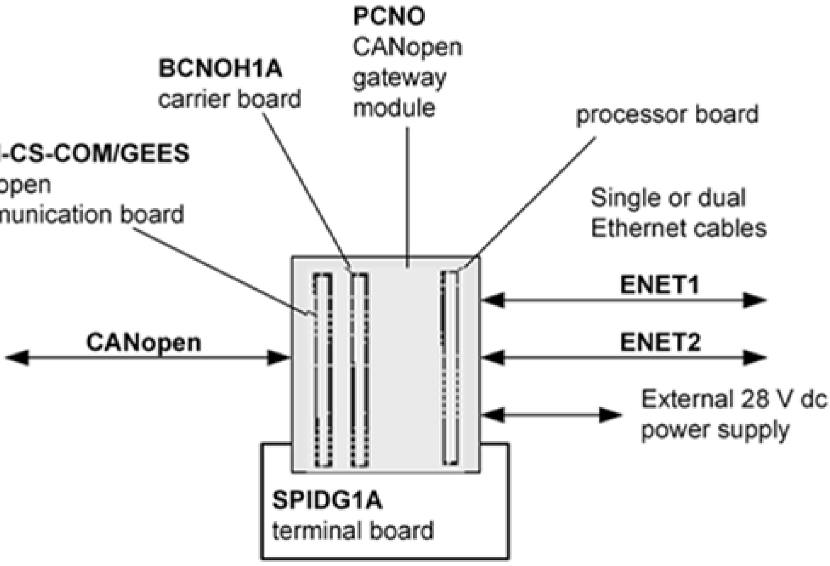
- Woodward™ GS6 and GS16 valves
- Woodward Digital Valve Positioners (DVPs) and Dual DVPs
- Woodward Liquid DLE Fuel Metering System (LFMS)
- GE Sensing DPS 8000 pressure transducers
- Moog Digital Valve Positioner (DVP)

Mixing the above devices on the same CANopen network is not supported.

The PCNO I/O pack contains a BPPx processor board and an acquisition carrier board fitted with a COM-C CANopen communication module supplied by Hilscher GmbH. The COM-C module provides a CANopen fieldbus interface through a DE-9 D-sub receptacle connector. It serves as a CANopen master supporting a maximum transmission rate of 500 kbps.

The PCNO supports the following redundancy options:

- Single I/O pack with single I/O Ethernet connection
- Single I/O pack with dual I/O Ethernet connections



4.1.1 Compatibility

The following are PCNO I/O pack versions and minimum software requirements:

- The PCNOH1A contains a BPPB processor board. These processors are reaching end of life. With ControlST* software suite V04.04 and later, the PCNOH1A can be replaced with a PCNOH1B.
- The PCNOH1B contains a BPPC processor board that is supported in the ControlST* software suite V04.04 and later.
- With PCNOH1B and ControlST V05.02 or later, the PCNO module can go online without all of the configured devices physically attached to the CANopen network.
- Woodward Dual DVPs require PCNOH1B with ControlST V05.02 or later.
- Moog DVPs require PCNOH1B with ControlST V06.00 or later.
- Woodward LFMS requires PCNOH1B with ControlST V06.02 or later.

4.1.2 Installation

➢ **To install the PCNO I/O pack**

Note The SPIDG1A terminal board is only used to mount a single PCNO I/O pack and to supply an electronic ID. No other connects are made to the terminal board.

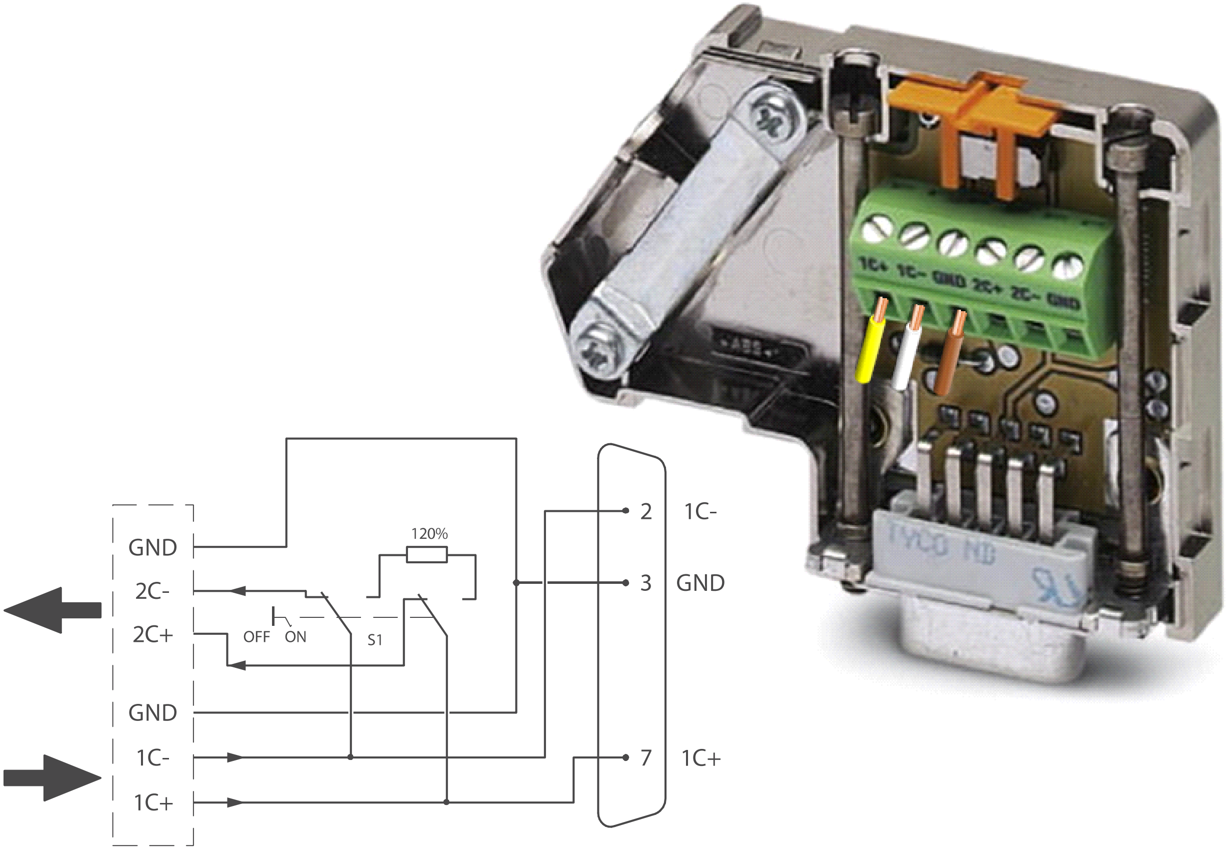
---

1. Securely mount the SPID terminal board to the panel.
2. Directly plug the PCNO into the terminal board DC-37 pin connector.
3. Mechanically secure the I/O pack using the threaded inserts adjacent to the Ethernet ports. The inserts connect to a mounting bracket specific to the terminal board type. The bracket should be adjusted so there is no right angle force applied to the DC-37 pin connector between the I/O pack and the terminal board. The adjustment should only be required once in the service life of the product.
4. Plug in one or two Ethernet cables depending on the system configuration. The I/O pack operates over either port. If dual connections are used, standard practice is to hook ENET1 to the network associated with the R controller; however, the PCNO is not sensitive to Ethernet connections and will negotiate proper operation over either port.
5. Install a 9-pin D-SUB bus connector onto the end of the CAN conductor line.
   a. If using the Phoenix Contact D-SUB bus connector - SUBCON-PLUS-CAN - 2744694, attach the CAN conductor line to the connector as indicated by the labels on the screws.

Note The terminator must be used in the connector because the I/O pack does not contain a terminating resister.

Phoenix Connector Pin Definitions

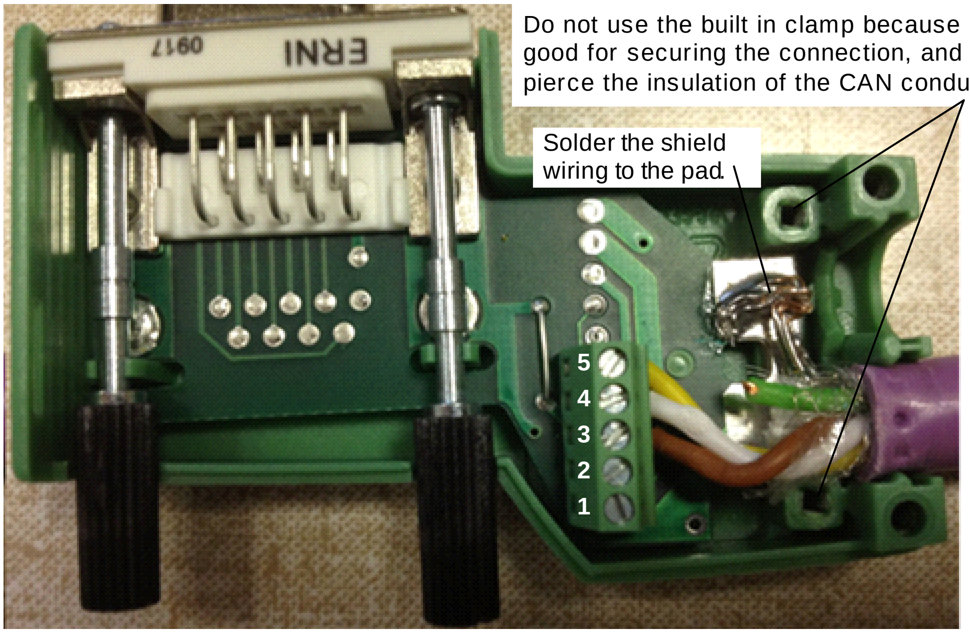
Conductor Wire Color	Phoenix Pin	Signal line	Type	D-Sub
Yellow	1C+	CAN-H	CANbus line	7
White	1C-	CAN-L	CANbus line	2
Brown	GND (third from left)	CAN-GND	CAN ground	3
Green	not used, clip			
Shield wiring (not insulated)	No soldering required if the cable bare shield mesh is clamped well under the shield clamp			



Phoenix Contact Connector

Note Refer to this website for more information on the Phoenix Contact connector:https://www.phoenixcontact.com/online/portal/us?uri=pxc-oc-itemdetail:pid=2744694&library=usen&pcck=P-08-07-02-05&tab=2

b. If using the ERNI® D-SUB bus connector, the shield wiring must be soldered to the pad, which also secures the cable.



Do not use the built in clamp because it is not good for securing the connection, and it can pierce the insulation of the CAN conductors.

Solder the shield wiring to the pad.

Ernie Connector

Ernie Connector Pin Definitions

Conductor Wire Color	ERNI pin (terminated)	ERNI pin (non-terminated)	Signal line	Type	D-Sub
Yellow	5	5,7	CAN-H	CANbus line	7
White	4	4,6	CAN-L	CANbus line	2
Brown	3	3,8	CAN-GND	CAN ground	3
Shield wiring not insulated	**must be soldered to pad**		Shield	Shield	Shell
Green	not used, clip				

6. Connect and secure the D-SUB bus connector to the DE-9 D-SUB receptacle connector on the I/O pack.

Attention

The CANbus shield should only be connected onto the PCNO I/O pack. This shield should not be connected onto the communication device. At any junction box along the way, pass the shield through without grounding it. The shell of the PCNO DE-9 D-sub receptacle is connected to the metal chassis of the I/O pack. It is then passed to the panel chassis when the I/O pack is securely mounted to the terminal board with the mounting nuts tightened.

7. It is recommended that a service loop/strain relief be applied to the CANopen cable within 10.16 cm (4 in) of the CAN connector to provide increased protection and cable support.

Note CiA® specification manuals can be ordered from the following website:*http://www.can-cia.org/index.php?id=440&L=http%253A%252F%252Fwww.wamp company.cz%252Fobchod%252Fipim%252Fqucu%252F*

8. As per CANopen requirements, the CANopen must be terminated on both ends of the network, using a 120 ohm resistor across CAN-H and CAN-L. Additional details may be found in the CANopen Additional specification *Cabling and connector pin assignment* (CiA 303-1), which is available from the *Can-in-Automation e.V* user organization.

9. Apply power to the connector on the side of the I/O pack. It is not necessary to insert the connector with power removed from the cable. The PCNO has inherent soft-start capability that controls current inrush on power application.

10. From the ToolboxST application, add the PCNO, and attach and configure the CANopen devices as needed. Refer to the following table for baud rates.

Supported Devices Per Network

Device	Baud Rate (kbps)	PCNO-H1A Max Devices	PCNO-H1B Max Devices	Frame Rate (ms)	Distance (meters)
Woodward GS6/16	500	5	5	10, 20, 40	100
	250	5	5	10, 20, 40	225
	125	1	1	10, 20, 40	500
GE Sensing DPS Sensor	500	15	25	10, 20, 40	100
	250	15	18	10, 20, 40	250
	125	8	8	10, 20, 40	500
Woodward DVP	500	8†	9	10	100
	500	4‡	9	10	100
	500	8	9	20, 40	100
	250	4	7	10, 20, 40	250
	125	1	1	10, 20, 40	500
	†PCNOH1A supports 8 Woodward DVPs with only 1 IONet connection at a 10 ms frame rate. ‡PCNOH1A supports 4 Woodward DVPs with 2 IONet connections at a 10 ms frame rate.				
Woodward Dual DVP	500	Not compatible	4	20, 40	100
	250		4	20, 40	250
Moog DVP	500	Not compatible	9	10, 20, 40	100
	250		7	10, 20, 40	250
	125		1	10, 20, 40	500
Woodward Liquid FMS	500	Not compatible	1	10, 20, 40	100
	250		1	10, 20, 40	250
	From the ToolboxST Component Editor, the Woodward FMS can only be attached to Device_125.				

4.1.2.1 PCNO I/O Pack Connectors

- ENET1 IONet connection
- ENET2 IONet connection
- 28 V dc power input
- DC-37 pin connector to terminal board
- DE-9 D-sub receptacle connector, COM-C interface to CANopen device

4.1.2.2 PCNO Replacement

Follow the procedures in the chapter, *Maintenance and Replacement* found in *GEH-6721_Vol_II.pdf* file. For more information on BPPB to BPPC upgrades, refer to *GEH-6721_Vol_I*, the section, *Migrating to BPPC-based I/O Packs*.

4.1.3 Operation

The following features are common to the distributed I/O modules:

- *BPPx Processor*
- *Processor LEDs*
- *Power Management*
- *ID Line*
- *I/O Module Common Diagnostic Alarms*

4.1.3.1 CANopen Gateway Hardware

The PCNOs COM-C module is built on a CANopen core, which is based on the Hilscher GmbH family of communication network interface modules. The COM-C's firmware, residing in a flash memory, is released as part of the PCNO firmware and downloaded to the COM-C's flash at I/O pack startup time only if necessary (for instance when the PCNO firmware is released with an updated COM-C firmware).

The COM-C module requires a CANopen configuration file that is loaded from the ToolboxST application. The configuration file specifies the PCNO master parameter set as well as other standard I/O pack configuration files and requires a PCNO reboot following the load if changed. As is the case with the COM-C firmware file, the CANopen configuration file is stored in COM-C flash and only downloaded from PCNO flash if necessary.

4.1.3.2 Online Loads

Most changes to the PCNO configuration (baud rate, adding or removing devices) do not support online loads because they fundamentally affect the nature of the CANopen network. The PCNO and COM-C module must be rebooted and reconfigured to accept these types of changes. Other changes (such as modifying the **DeviceRequired** parameter) support online loads to facilitate faster troubleshooting and commissioning.

4.1.3.3 Dataflow

Control data is passed between the PCNO I/O pack and the Mark VIe controller through IONet Ethernet Global Data (EGD). The PCNO uses multiple Class 1 data exchanges for inputs and outputs.

The PCNO sends outputs to the Woodward GS6 or GS16 valves in multiple Receive Process Data Objects (RPDOs) and receives inputs in multiple Transmit Process Data Objects (TPDOs). Fast Request with Demand and Command Bits messages (Receive PDO 1) are sent each frame to all connected valves with a synchronization jitter of up to 1 ms. Actual Position and Status from Valve messages (Transmit PDO 1) are received in response with a possible 1 frame period jitter.

Note DPS pressure transducers do not transmit any special diagnostics.

The PCNO receives inputs from the GE Sensing DPS pressure transducers in one TPDO. This family of devices does not support outputs or RPDOs. For every Mark VIe controller frame, the PCNO sends a CANopen Sync message to each GE sensing DPS pressure transducer. The transducers in turn respond with pressure and acquisition time (Transmit PDO 1).

Note Moog or Woodward DVPs support two CANopen interfaces. Use one PCNO per CANopen interface for redundancy considerations.

The PCNO sends outputs to Moog DVPs, Woodward DVPs, or Dual DVPs in multiple RPDOs and receives inputs in multiple TPDOs. Fast Request with Demand and Command Bits messages (Receive PDO 1) are sent each frame to all connected DVPs with a synchronization jitter of up to 1 ms. Actual Position and Status from DVP messages (Transmit PDO 1) are received in response to a SYNC CANopen message with a possible 1 frame period jitter.

The PCNO sends outputs to the Woodward LFMS in multiple RPDOs and receives inputs in multiple TPDOs. All RPDOs to the Woodward LFMS are sent each frame to the connected device with a synchronization jitter of up to 1 ms. Feedback messages (TDPOs) are received in response to a SYNC CANopen message with a possible 1 frame period jitter.

4.1.3.4 PCNO CANbus PDO Counters

Note PCNO counters originate within the PCNO itself. These counters are not marked as unhealthy when the attached device is offline since they belong to the PCNO and not the attached device.

For each attached device, the PCNO maintains counter variables. These counter variables increment whenever the associated message is transmitted by the attached device (Transmit Process Data Objects received by the PCNO) or transmitted by the PCNO (Receive Process Data Objects). These counters can be used by the Mark VIe controller application as indications of attached device health. In particular, all TPDO counters should be monitored for activity by the Mark VIe controller application.

Number of Counters Per Device

Attached Device	Number of TPDOs	Number of RPDOs
GS6 / GS16	6	3
DPS sensors	1	None
Moog DVPs, Woodward DVPs, or Dual DVPs	8	8
Woodward Liquid FMS	8	5

Note Refer to the section, *Configuration* for the attached device type.

GS6, GS16, Woodward DVP, Dual DVP, and Moog DVP devices use *extended* PDOs, which must be enabled as part of their internal configuration. If these extended PDOs are not enabled, then the associated PCNO counters for the extended TPDOs will be zero. *Fast* PDOs are transmitted/received at Mark VIe controller frame rate. TPDO1 and RPDO1 are *Fast* PDOs, but DPS sensor devices do not have an RPDO1.

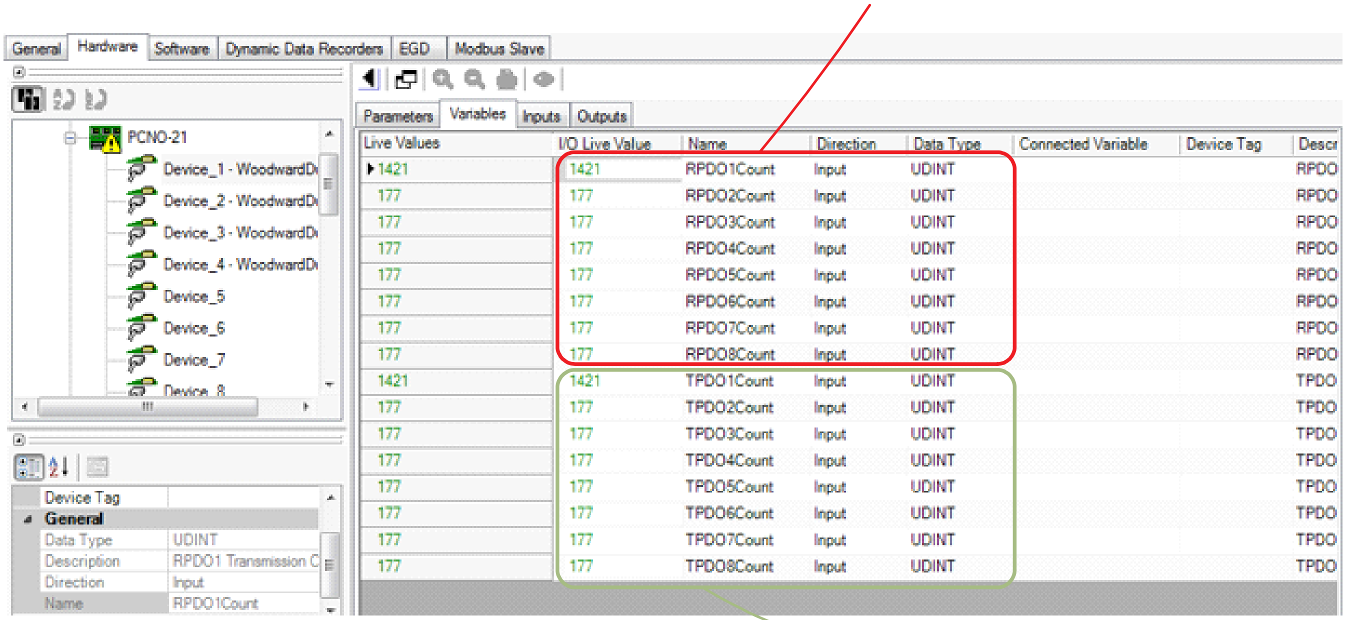
All other PDOs are *slow*. These messages are updated as slowly as 160 ms (for quantity eight DVP configurations). Therefore, the counters associated with slow PDOs may update at a rate as low as 1/16th the rate of fast PDOs.

Note These counters are maintained by the PCNO for each attached device.

In the following ToolboxST Component Editor, the Mark VIe controller frame rate is 20 ms, fast PDOs update every 20 ms, and the slow PDOs update at a nominal rate of 20 ms multiplied by the number of DVPs attached, which equals 80 ms. Therefore, in this example, the slow PDOs update at 1/4th the rate of fast PDOs.

For the Woodward LFMS device, all RPDOs and TPDOs are considered *Fast* PDOs and are transmitted/received at the Mark VIe controller frame rate.

RPDO counters increment when each message is transmitted by the PCNO. These values will continue to increment when the device is offline.



Live Values	I/O Live Value	Name	Direction	Data Type	Connected Variable	Device Tag	Descr
1421	1421	RPDO1Count	Input	UDINT			RPDO
177	177	RPDO2Count	Input	UDINT			RPDO
177	177	RPDO3Count	Input	UDINT			RPDO
177	177	RPDO4Count	Input	UDINT			RPDO
177	177	RPDO5Count	Input	UDINT			RPDO
177	177	RPDO6Count	Input	UDINT			RPDO
177	177	RPDO7Count	Input	UDINT			RPDO
177	177	RPDO8Count	Input	UDINT			RPDO
1421	1421	TPDO1Count	Input	UDINT			TPDO
177	177	TPDO2Count	Input	UDINT			TPDO
177	177	TPDO3Count	Input	UDINT			TPDO
177	177	TPDO4Count	Input	UDINT			TPDO
177	177	TPDO5Count	Input	UDINT			TPDO
177	177	TPDO6Count	Input	UDINT			TPDO
177	177	TPDO7Count	Input	UDINT			TPDO
177	177	TPDO8Count	Input	UDINT			TPDO

Device Tag	
General	
Data Type	UDINT
Description	RPDO1 Transmission C
Direction	Input
Name	RPDO1Count

TPDO counters increment when messages are received by PCNO from the device. These values will be stationary when device is offline.

Sample Display with Counter Variables

4.1.3.5 CANopen Device Health

Note With PCNO firmware version 4.06 and higher, there is a three second delay between when the I/O pack determines that the CANopen device input is no longer unhealthy and when it sets the input health bit to healthy.

Each CANopen input has an associated I/O pack health bit. The I/O pack sets input health to unhealthy when any of the following conditions occur:

- Loss of communication between the associated CANopen devices and the CANopen master
- Loss of COM-C module READY/RUN status
- Standard I/O Ethernet input validation error

Tip ➪ *Connect each variable to a VAR_HEALTH block so that the health of variables are propagated to Live Values and then on to Connected Variables and controller blocks, Trender, and Live Views.*

4.1.3.6 CANopen Network Health

The PCNO implements an advanced algorithm to determine health of the CANopen network. A healthy network has at least one configured device that is present and transmitting TPDO1 to the PCNO. If no devices are present or transmitting, the PCNO stops all output data (RPDO, SYNC) and generates a diagnostic alarm. This effectively stops all communication on the CANopen network and defines an unhealthy network. To restart communication, all devices marked **DeviceRequired** must be present. Once the PCNO has revalidated the devices, it restarts PDO communication, and clears or sets the appropriate diagnostics.

Note PCNOH1A does not support the **DeviceRequired** parameter. A ToolboxST build error is generated if the **DeviceRequired** parameter is changed to FALSE with PCNOH1A.

The **DeviceRequired** parameter controls the check for device presence on the network, which in turn determines if the PCNO starts (or restarts) PDO communication to the CANopen network. The default value of *TRUE* is the most restrictive. When a device is marked required, it must be present and validated before the PCNO will begin communication with any devices connected to the network. If the device is not present, the PCNO generates a diagnostic alarm indicating the missing device id.

One of the following scenarios must be satisfied before the PCNOH1B will begin communication with the CANopen network:

- If **DeviceRequired** is *TRUE*, then the device must be present and a valid device
- If **DeviceRequired** is *FALSE* and the device is not connected, then the device is ignored.
- If **DeviceRequired** is *FALSE* and the device is connected, then the device must be a valid device
- If **DeviceRequired** is *FALSE* for every device, then at least one device must be present and a valid device

Specifications

Item	PCNO Specification
CANopen connection ‡	RS-485 interface through DE-9 D-sub receptacle connector
Transmit time	For all devices, CANopen output data from the Mark VIe controller is received by the PCNO once per frame, up to 100 times per second.
	Woodward GS6 or GS16 valve: RPDO1 messages for all valves are transmitted each frame, and RPDO2 and RPDO3 messages are transmitted per valve on a round robin basis each frame.
	Woodward DVP, Dual DVP or Moog DVP: RPDO1 messages for all devices are transmitted each frame, and RPDO2-RPDO8 messages are transmitted per device on a round robin basis every even frame (2 frames used per device).
	Woodward LFMS: RPDO1-RPDO5 messages are transmitted each frame.
Receive time	CANopen inputs are then scanned by the PCNO firmware and transmitted to the Mark VIe controller once per frame, up to 100 times per second.
	For Woodward GS6 or GS16 valves: TPDO1 received synchronously each frame from all valves as a response to the receipt of RPDO messages. TPDO2-6 received per valve on a round robin basis.
	For GE sensing DPS pressure transducers: CANopen inputs are received as a response to the CANopen SYNC message. TPDO1 received synchronously each frame from all sensors.
	For Moog DVP, Woodward DVP, or Dual DVP: Fast inputs (TPDO1 messages) are in response to the CANopen SYNC message, received each frame. Slow inputs (TPDO2-TPDO8) are in response to the RPDO2 output message, received on a round robin basis.
	For Woodward LFMS: TPDO1-TPDO8 are in response to the CANopen SYNC message, received each frame.
Supported frame rates	Refer to the table, *Supported Devices Per Network*.
Size	8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in x 1.65 in x 4.78 in)
Technology	Surface mount
† Ambient rating for enclosure design	-20 to 55ºC (-4 to 131 ºF)
‡ Connecting more than one slave type on the same CANopen network is not supported.	

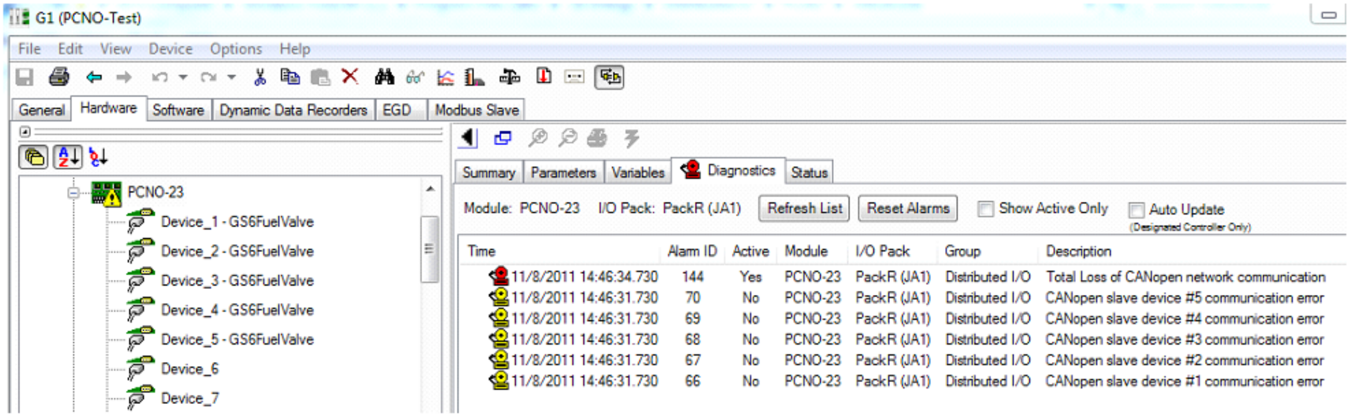
Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

4.1.4 Diagnostics

4.1.4.1 Device Offline Conditions

Note Refer to the section, *CANopen Network Health* for more information on setting devices to not be required.

When one or more required CANbus devices go offline, the PCNO will generate communication error diagnostic alarms. When that happens, the device TPDO counters will stop updating, and all input variables for the device will be marked unhealthy. However, the PCNO will still attempt to transmit outputs to the offline device. Therefore, the RPDO counters will continue to increment at the nominal rates defined for fast and slow PDOs. The PDO counters are PCNO variables, which are not marked unhealthy when an attached device is offline.



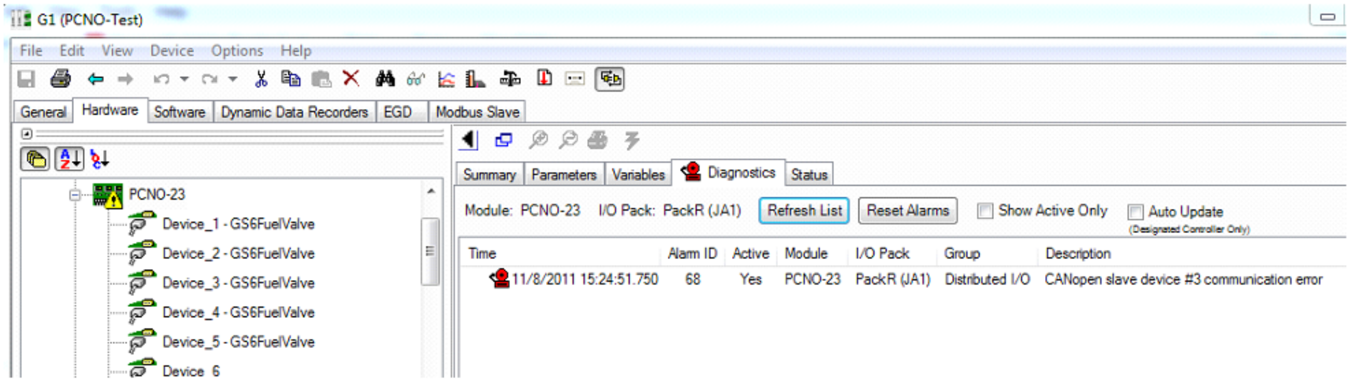
Module: PCNO-23 I/O Pack: PackR (JA1)

Time	Alarm ID	Active	Module	I/O Pack	Group	Description
11/8/2011 14:46:34.730	144	Yes	PCNO-23	PackR (JA1)	Distributed I/O	Total Loss of CANopen network communication
11/8/2011 14:46:31.730	70	No	PCNO-23	PackR (JA1)	Distributed I/O	CANopen slave device #5 communication error
11/8/2011 14:46:31.730	69	No	PCNO-23	PackR (JA1)	Distributed I/O	CANopen slave device #4 communication error
11/8/2011 14:46:31.730	68	No	PCNO-23	PackR (JA1)	Distributed I/O	CANopen slave device #3 communication error
11/8/2011 14:46:31.730	67	No	PCNO-23	PackR (JA1)	Distributed I/O	CANopen slave device #2 communication error
11/8/2011 14:46:31.730	66	No	PCNO-23	PackR (JA1)	Distributed I/O	CANopen slave device #1 communication error

If the CANbus cable is removed from the PCNO or if all configured devices are powered off, the following symptoms will be present:

- Communication error diagnostic alarms may be signaled for all defined devices.
- A diagnostic alarm will be signaled indicating a total loss of CANbus communications.
- All TPDO and RPDO counters will stop incrementing.

Normal operation will resume when the CANbus cable is reconnected and all required devices are revalidated by the PCNO.



Module: PCNO-23 I/O Pack: PackR (JA1)

Time	Alarm ID	Active	Module	I/O Pack	Group	Description
11/8/2011 15:24:51.750	68	Yes	PCNO-23	PackR (JA1)	Distributed I/O	CANopen slave device #3 communication error

If some but not all configured devices are powered off, then the following symptoms will be present:

- Communication error diagnostic alarms will be signaled for each device that is powered down.
- TPDO counters belonging to the powered down device will stop incrementing
- The RPDO counters belonging to the powered down device will increment very slowly. This is because the PCNO’s CANbus communications (COM-C) module is attempting to reestablish communications.
- All counters belonging to healthy CANbus devices will continue to update normally.

4.1.4.2 Woodward GS6 and GS16 Valve Diagnostics

A number of diagnostic inputs are returned from the Woodward GS6 and GS16 valves. For example, an *InputVoltageLowErr* Boolean input is returned to provide an indication that the GS6/GS16 supply voltage is below nominal limits. Details on the meanings of these diagnostic inputs and associated troubleshooting actions can be found in the Woodward Installation and Operation Manual for the GS6 Gas Metering System (Manual 26171) and Installation and Operation Manual for the GS16 Gas Metering System (Manual 26228). As part of the valve purchase, the manual for corresponding valve is provided to the customer.

4.1.4.3 Woodward Digital Valve Positioner (DVP) and Dual DVP Diagnostics

A number of diagnostic inputs are returned from the Woodward Digital Valve Positioners. For example, *DigitalComErr1* and *DigitalComErr2* Boolean inputs are returned to provide an indication of CAN communications health for each CANopen network. Details on the meanings of these diagnostic inputs and associated troubleshooting actions can be found in the Woodward Installation and Operation Manual for the Digital Value Positioner (DVP) [Manual 26329]. As part of the purchase, the manual for the Digital Valve Positioner (DVP) is provided to the customer.

4.1.4.4 Moog Digital Valve Positioner (DVP) Diagnostics

A number of diagnostic inputs are returned from Moog Digital Valve Positioners. For example, *FbusFault* and *FbusFault1* Boolean inputs are returned to provide an indication of CAN communications health for CANopen Network 1 and Network 2 respectively. Details on the meanings of these diagnostic inputs and associated troubleshooting actions can be found in the *Moog Installation and Operation Manual for the Digital Valve Positioner (DVP)*. The following is a *Link to Moog Manuals Webpage*.

4.1.4.5 Woodward Liquid DLE Fuel Metering System (LFMS) Diagnostics

A number of diagnostic inputs are returned from Woodward Liquid Fuel Metering System. For example, CAN_NTWK1FLT and CAN_NTWK5FLT Boolean inputs are returned to provide an indication of CAN communications health for CANopen Network 1 and Network 5 respectively. Details on the meanings of these diagnostic inputs and others can be found in the *Woodward Liquid DLE FMS [Manual 35049]*. As part of the LFMS purchase, this manual is provided to the customer.

4.1.4.6 PCNO CANopen Status LEDs

A green LED labeled SYS RUN indicates three different conditions as follows:

- LED solid on – the COM-C module has established communication with at least one CANopen device.
- LED flashing fast cyclically (5 Hz) – CANopen master is configured and ready to communicate with CANopen devices, but is not connected or otherwise unable to communicate
- LED flashing non-cyclically (3 times at 5 Hz then 8 times between 0.5 Hz and 1 Hz) – the COM-C module is either missing a CANopen configuration or its watchdog timer maintained with the I/O pack firmware has timed out (120 ms timeout)

A yellow LED labeled NOT RDY indicates three different conditions as follows:

- LED flashing slowly cyclically (1 Hz) – COM-C module is waiting for a firmware load
- LED flashing fast cyclically (5 Hz) – COM-C firmware download in progress
- LED flashing non-cyclically (3 times at 5 Hz then 8 times between 0.5 Hz and 1 Hz) – serious COM-C hardware for firmware error

Note If both the SYS RUN and NOT RDY LEDs are off at the same time, either power is not applied or the COM-C module is being reset. In all other conditions, one or the other LED will be on (though maybe flashing). The SYS RUN LED lights when the COM-C module's SYS LED is green; the NOT RDY LED lights when the COM-C module's SYS LED is yellow.

A green LED labeled COMM OK mimics the COM-C COM LED when it is yellow:

- LED solid on – the COM-C module is holding the CANopen token and is able to transmit CANopen telegrams to CANopen devices.
- LED out – the COM-C is not communicating on the CANopen network

A red LED labeled COMM ERR mimics the COM-C COM LED when it is red:

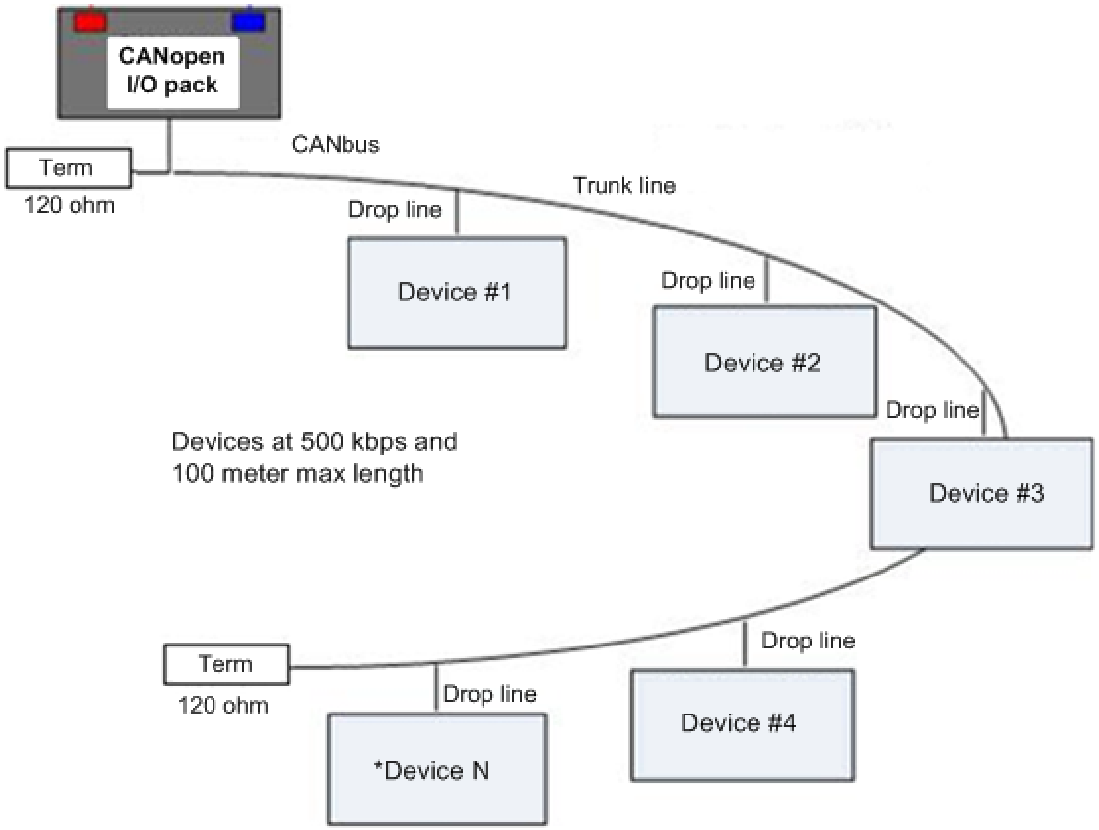
- LED solid on – the COM-C module has encountered a communication
- LED out – check COMM OK LED for communication status

4.1.4.7 Advanced Diagnostics

The ToolboxST application provides an Advanced Diagnostics command to display the diagnostic bytes that are generated by CANopen slave devices. From the Component Editor, right-click a PCNO and select Troubleshoot, Advanced Diagnostics, then press F1 for help on this topic.

4.1.5 Configuration

In general, a CANbus network consists of a single *trunk line*, which is terminated with 120Ω at each end. The trunk line may be comprised of DeviceNet thin cable (such as TURCK® 5732), thick cable (such as TURCK 5730), or a combination of both types of cable. CANbus devices are attached to the trunk line using adapters. The device must be attached to the trunk line with a maximum distance of 6 m (20 ft). The cabling from the CANbus device to the trunk line is referred to as a *drop line*.



Note The drop line maximum length is 20 m (66 ft). Any individual drop line can be zero. Refer to the table, Supported Devices Per Network.

The maximum length of the trunk line is a function of the baud rate used and the type of cable used. This maximum allowable trunk line length may be reduced if DeviceNet thin cable is used at baud rates less than 500 kbps. In addition, the calculated maximum distance must also take into account the longest distance between any two devices, inclusive of the PCNO, on the trunk line and/or any drop line. The following table lists the maximum CANbus network length for each baud rate for combinations of thin or thick DeviceNet cable:

Bit Rate	Maximum CANbus Network Lengths
125 kbps	500 m (1640 ft) = $\text{Length}_{\text{thick}}$ + 5 * $\text{Length}_{\text{thin}}$
250 kbps	250 m (820 ft) = $\text{Length}_{\text{thick}}$ + 2.5 * $\text{Length}_{\text{thin}}$
500 kbps	100 m (328 ft) = $\text{Length}_{\text{thick}}$ + $\text{Length}_{\text{thin}}$
$\text{Length}_{\text{thick}}$ is the length of thick cable.	
$\text{Length}_{\text{thin}}$ is the length of thin cable.	

The drop line length is the cable distance measured from the tap on the trunk line to the transceiver on each device. This length must not exceed 6 m (20 ft). The total length of all drop lines (cumulative) on the network depends upon the bit rate and must not exceed the values in the following table:

Bit Rate	** Cumulative Drop Line Length
125 kbps	156 m (512 ft)
250 kbps	78 m (256 ft)
500 kbps	39 m (128 ft)
** The cumulative drop line limits are independent of the type of DeviceNet cable in use.	

4.1.5.1 Woodward GS6 and GS16 Valves

Note Configuration is accomplished using the Woodward configuration tool. Refer to the Woodward Installation and Operation Manual for the GS6 Gas Metering System (Manual 26513) or for the GS16 Gas Metering System (Manual 26514). As part of the valve purchase, a manual is provided to the customer.

The Woodward GS6/GS16 valve configuration includes the following:

- *Baud Rate* default is 500 kbps and should be changed to match the configured BaudRate parameter of the PCNO.
- *Node ID* should be set equal to the attached PCNO device number in the ToolboxST application.
- *CAN Timeout* is the maximum sync rate time. The default value is 40. The suggested value is at least twice the Mark VIe controller frame rate plus 10 ms.
- *Enable PDO5 and PDO6* is disabled by default, but must be enabled to receive status bits.

4.1.5.2 DPS Pressure Transducer

Note The configuration of the DPS device needs to be set by a GE Sensing approved CANopen configuration tool prior to being installed on the CANopen bus.

The following sensor parameters must be configured before the PCNO can communicate with the device:

- *Baud Rate* default is 250 kbps and must be changed to match the configured BaudRate parameter of the PCNO.
- *Node ID* should be set equal to the attached PCNO device number in the ToolboxST application.

The following optional sensor parameters change the desired operation of the device:

- *Tag* contains ten characters of descriptive text.
- *Calibration Data* includes Date of last calibration, Gain, and Offset values.
- *Scaling Data* includes non-SI units, Engineering unit scale, and so forth.

Note Special handling is required for offline maintenance of DPS Pressure Transducers.

All DPS Pressure Transducers on the CANbus are powered by a single power source. Power is supplied within the CANbus cable and daisy-chained from one sensor to the next sensor.

Note Refer to the GE Measurement & Control DPS Series CANbus Pressure Transducer User Manual for the specific DPS Transducer (K0533 or other manual as appropriate).

The DPS sensors are not intended to be individually powered down and hot-swapping with power on is not supported. Removing power from any single DPS sensor may have adverse effects on measurements from other sensors on the same network. When performing maintenance on any DPS sensor, always remove power from all sensors on the CANbus for at least four seconds. Perform offline maintenance using the precautions listed in the DPS User Manual and then restore power to all DPS sensors.

4.1.5.3 Woodward Digital Valve Positioner (DVP) and Dual DVP Configuration

Note Configuration is accomplished using the Woodward configuration tool. Refer to the Woodward Installation and Operation Manual for the Digital Value Positioner (Manual 26329). As part of the valve purchase, this manual is provided to the customer.

The Woodward DVP configuration includes the following:

- *Baud Rate* default is 500 kbps and should be changed to match the configured BaudRate parameter of the PCNO.
- *CAN Port #1 Node ID and CAN Port #2 Node ID* should be set equal to each attached PCNO device number in the ToolboxST application.
- *CAN Timeout* is the maximum sync rate time. The default value is 40. The suggested value is at least twice the Mark VIe controller frame rate plus 10 ms.
- *Enable Extended PDOs* must be enabled to receive all DVP data.
- *Mode* should be set as follows:
  - For DVPs: *CANOPEN SINGLE W/WO ANALOG BACKUP* or *CANOPEN DUAL* as appropriate
  - For Dual DVPs: *CAN_OPEN_DUAL_DVP*

4.1.5.4 Moog Digital Valve Positioner (DVP) Configuration

Note Link to Moog Manuals Webpage

Configuration is accomplished using Hex switch settings on Moog Control Head or using the Moog Configuration Tool. Refer to the *Moog Installation and Operation Manual for the Digital Valve Positioner (DVP)*. As part of the valve purchase, this manual is provided to the customer. The Moog DVP configuration includes the following:

- *Baud Rate* default is 500 kbps and should be changed (using the Moog Configuration Tool) to match the configured BaudRate parameter of the PCNO.
- CAN Port #1 Node ID and CAN Port #2 Node ID are set via Hex ID1 Switch on the front of the Moog Control Head. The same ID is used for both channels. This should be set equal to each attached PCNO device number in the ToolboxST application. A change to the Hex Switch requires a power cycle of the Moog DVP for the change to take place.
- CAN Frame Time should be set to match the Frame rate of the Mark VIe controller and has valid values of 10 ms, 20 ms, and 40 ms. The default value is 40 ms. The Moog Configuration Tool can be used to change this configuration.
- Hex ID2 Switch on the front of the Moog Control Head selects the valve type. Refer to the *Moog Installation and Operation Manual* for the proper selection.

4.1.5.5 Woodward Liquid DLE Fuel Metering System (LFMS) Configuration

Note Configuration is accomplished using the Woodward configuration tool. Refer to the Woodward Liquid DLE FMS [Manual 35049]. As part of LFMS purchase, this manual is provided to the customer.

The Woodward LFMS configuration includes the following:

- Baud Rate default is 500 kbps and should be changed to match the configured BaudRate parameter of the PCNO. (Only 500 kbps and 250 kbps are supported.)
- CAN Port #1 Node ID and CAN Port #5 Node ID are fixed to **125**. This is enforced in the PCNO by only allowing the Woodward LFMS to be configured on Device_125 in the ToolboxST application.
- CAN Network Timeout is the maximum sync rate time. The default value is 40. The suggested value is at least twice the Mark VIe controller frame rate plus 10 ms.

4.2 PCNO Specific Alarms

The following alarms are specific to the PCNO I/O pack.

33

Description CANopen module upgrade failure

Possible Cause A malfunction occurred when a new CANopen module firmware file was being loaded to the CANopen module.

Solution

- Rebuild and download firmware to the PCNO.
- If the issue persists, replace the I/O pack.

34

Description CANopen module access failure - Unable to download configuration

Possible Cause A malfunction occurred when a new CANopen configuration was being loaded to the CANopen module.

Solution

- Rebuild and download firmware to the PCNO.
- If the issue persists, replace the I/O pack.

35

Description Bad configuration loaded to CANopen module

Possible Cause Invalid CANopen configuration files were downloaded to the CANopen module. This causes the CANopen module to not reach the RUN status, which is generally reached when a valid configuration has been processed.

Solution

- Power cycle the I/O pack.
- Reload the PCNO firmware with updated CANopen configuration files.

36

Description Unable to communicate with CANopen module

Possible Cause The CANopen host watchdog (a heartbeat between the pack processor and CANopen module) could not be activated.

Solution

- Rebuild and download the firmware to the PCNO.
- If the issue persists, replace the I/O pack.

37

Description CANopen module failure

Possible Cause From the PCNO firmware perspective, the CANopen watchdog timed out (indicating failure of the CANopen firmware).

Solution

- Rebuild and download the firmware to the PCNO.
- If the issue persists, replace the I/O pack.

38

Description CANopen module failure - Module shutdown

Possible Cause The CANopen module has shut down, indicated by a loss of READY/RUN. CANopen READY indicates that the firmware is running, and RUN indicates that a valid configuration has been processed. Loss of READY/ RUN implies that the CANopen module has shut down.

Solution

- Power cycle the I/O pack.
- If the issue persists, replace the I/O pack.

39-64

Note This alarm is obsolete.

Description Unknown CANopen device #[ ] identified on CANopen network

Possible Cause An identity check for one of the connected devices has failed. During startup, and when a new device is detected, the I/O pack confirms the identity of expected devices before starting normal operation.

Solution Verify that the (re)connected device is the same as the ToolboxST configuration.

65

Note This alarm is obsolete.

Description Waiting for all CANopen devices to connect

Possible Cause

- Not all required slaves are connected to the CANopen network.
- During startup, the I/O pack requires all slaves to be connected to confirm the identity of all required devices before starting normal operation.
- During normal operation, the I/O pack generates this alarm if a disconnected device is reconnected with a duplicate ID.

Solution

- Verify that the number of connected devices matches the number configured in the ToolboxST application.
- Verify that all connected devices have power applied and are operating correctly.
- Verify that the connected devices are configured correctly (for example, the device ID and baud rate).
- Check if any devices are configured with the same CANopen device ID.

66-91

Description CANopen slave device #[ ] communication error

Possible Cause

- Connected device is powered off or rebooting
- Failed CANopen bus connection between I/O pack and controller.
- Connected device has not communicated or sent heartbeat message on CANbus over at least five consecutive Mark VIe controller frames.

Solution

- Verify that the connected device has power applied.
- Verify that the CANopen cable is properly connected.
- Cycle power on the slave device.
- Troubleshoot the connected device for internal errors, referring to its manual. If the problem persists, replace the connected device.

92-117

Description Device #[ ] identification failure. Configured Model [ ], Found [ ]

Possible Cause An identity check for one of the connected devices has failed. During startup, and when a new device is detected, the I/O pack confirms the identity of expected devices before starting normal operation.

Solution Verify that the connected or reconnected device is the same as the ToolboxST configuration.

118-143

Description Waiting for CANopen device #[ ] to connect

Possible Cause

- Not all required slaves are connected to the CANopen network.
- During startup, the I/O pack requires all slaves to be connected to confirm the identity of all required devices before starting normal operation.
- During normal operation, the I/O pack generates this alarm if a disconnected device is reconnected with a duplicate ID.

Solution

- Verify that the number of connected devices matches the number configured in the ToolboxST application.
- Verify that all connected devices have power applied and are operating correctly.
- Verify that the connected devices are configured correctly (for example, the device ID and baud rate).
- Check if any devices are configured with the same CANopen device ID.

144

Description Total Loss of CANopen network communication

Possible Cause

- None of the required devices are connected to the CANopen network.
- The CANopen cable is disconnected from the I/O pack.
- The CANopen cable is not terminated properly.

Solution

- Verify that all connected devices have power applied and are operating correctly.
- Verify that the connected devices are configured correctly (for example, the device ID and baud rate).
- Verify the integrity of the CANopen cable, all connections points, and terminating resistors.

145-170

Description Device #[ ] identification failure. Configured VendorId [ ], Found [ ]

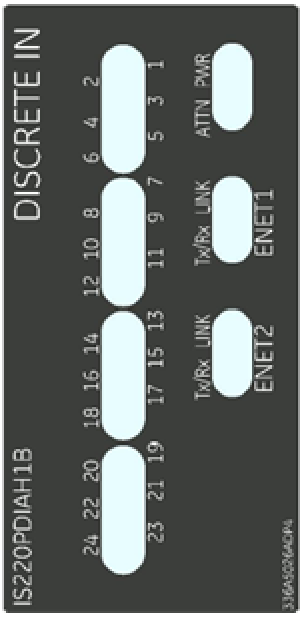
Possible Cause An identity check for one of the connected devices has failed. During startup, and when a new device is detected, the I/O pack confirms the identity of expected devices before starting normal operation.

Solution Verify that the connected or reconnected device is the same as the ToolboxST configuration.

Notes

5 PDIA, YDIA Discrete Input Modules

5.1 Mark VIe PDIA Discrete Input Pack

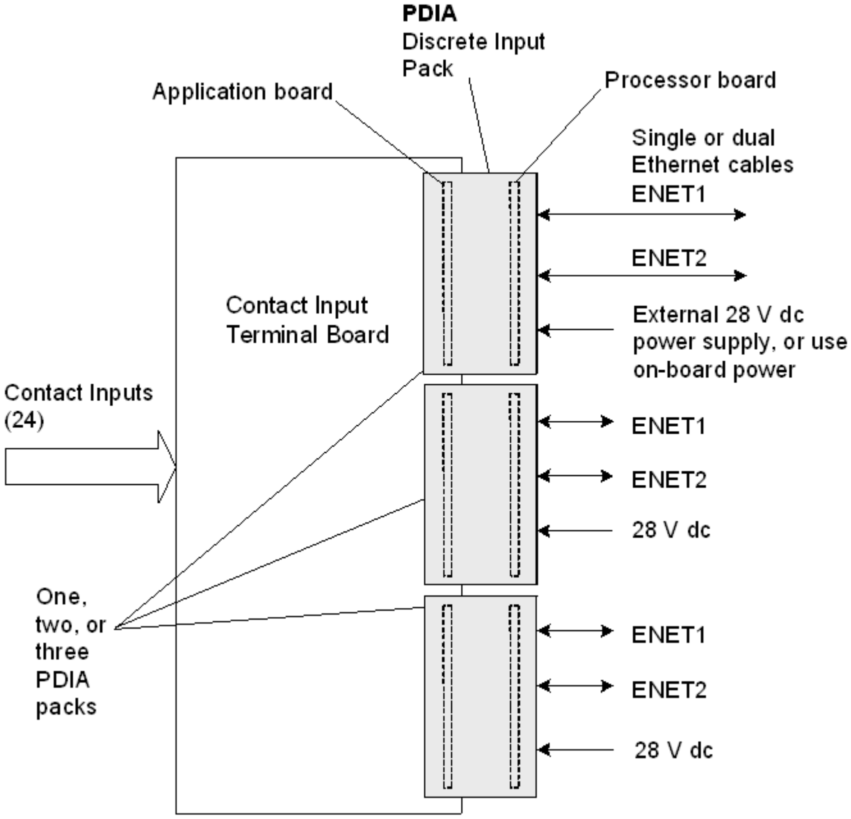


The Discrete Input (PDIA) I/O pack provides the electrical interface between one or two I/O Ethernet networks and a discrete input terminal board. The PDIA contains a BPPx processor board and an acquisition board specific to the discrete input function. The I/O pack accepts up to 24 contact inputs and terminal board specific feedback signals. Three different wetting voltages are available, and isolated discrete input voltage sensing is also available when using a supported terminal board.

System input to the I/O pack is through dual RJ-45 Ethernet connectors and a three-pin power input. Discrete signal input is through a DC-37 pin connector that connects directly with the associated terminal board connector. Visual diagnostics are provided through indicator LEDs.

Contact input terminal board types provide the following options:

- 24, 48, or 125 V dc wetting voltage options
- Simplex, dual, and TMR options
- Isolated input with ac wetting voltage options


PDIA
Discrete Input Pack
Application board
Processor board
Single or dual Ethernet cables
ENET1
ENET2
External 28 V dc power supply, or use on-board power
Contact Input Terminal Board
Contact Inputs (24)
ENET1
ENET2
28 V dc
One, two, or three PDIA packs
ENET1
ENET2
28 V dc

5.1.1 Compatibility

The PDIA I/O pack includes one of the following compatible BPPx I/O processor boards:

- The PDIAH1A contains a BPPB processor board.
- The PDIAH1B contains a functionally compatible BPPC that is supported in the ControlST* software suite V04.04 and later.

The following is an explanation of redundancy options:

- Simplex uses one I/O pack with one or two network connections.
- Dual uses two I/O packs with one network connection on each.
- TMR uses three I/O packs with one network connection on each.

The PDIA I/O pack is compatible with the discrete contact input terminal boards listed in the following table. The DIN-rail mounted DTCI board is not compatible with the PDIA.

Terminal Board	Wetting Voltage	Simplex	Dual	TMR	Terminal Blocks
TBCIH1C	125 V dc	Yes	Yes	Yes	Barrier-type
TBCIH2C	24 V dc				
TBCIH3C	48 V dc				
TBCIH4C [1]	24 V dc				
TBCIS1C[2]	125 V dc				
TBCIS2C[2]	24 V dc				
TBCIS3C[2]	48 V dc				
TICIH1A	125 or 250 V dc 115 or 230 V ac				
TICIH2A	24 V dc				
STCIH1A	24 V dc	Yes	No	No	Euro style box-type, fixed
STCIH2A	24 V dc				Euro style box-type, pluggable
STCIH4A	48 V dc				
STCIH6A	125 V dc				
STCIH8A [1]	24 V dc				
STCIS1A [2]	24 V dc				Euro style box-type, fixed
STCIS2A [2]	24 V dc				Euro style box-type, pluggable
STCIS4A [2]	48 V dc				
STCIS6A [2]	125 V dc				

[1] These terminal boards were specifically designed for use in hazardous locations.

[2] These terminal boards are IEC 61508 safety certified when used with the YDIA I/O pack. *Refer to GEH-6722, Mark VIeS Safety Control System Guide*.

5.1.2 Installation

Caution

Some panels contain a mixture of ac and dc wetting voltages. Care must be taken to avoid connecting the ac wetting voltages to the terminal board wetting voltage inputs because this causes misoperation and can damage these terminal boards. Furthermore, verify that the ac wetting voltages and the dc wetting voltages are not inadvertently cross-connected because this causes misoperation and can damage the terminal boards.

➢ **To install the PDIA I/O pack**

1. Securely mount the desired terminal board.
2. Directly plug the PDIA I/O pack into the terminal board connectors.
3. Mechanically secure the I/O pack(s) using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right-angle force applied to the DC-37 pin connector between the I/O pack and the terminal board. The adjustment should only be required once in the service life of the product.

Note The PDIA I/O pack mounts directly onto a Mark VIe control terminal board. Simplex terminal boards have a single DC-37 pin connector that receives the PDIA. TMR-capable terminal boards have three DC-37 pin connectors, one used for simplex operation, two for dual operation, and three for TMR operation. The PDIA directly supports all of these connections.

4. Plug in one or two Ethernet cables depending on the system configuration. The I/O pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
5. Apply power to the I/O pack by plugging in the connector on the side of the pack. It is not necessary to remove power from the cable before plugging it in because the I/O pack has inherent soft-start capability that controls current inrush on power application.
6. Use the ToolboxST* application to configure the I/O pack as necessary. From the Component Editor, press F1 for help.

5.1.2.1 Connectors

The I/O pack contains the following connectors:

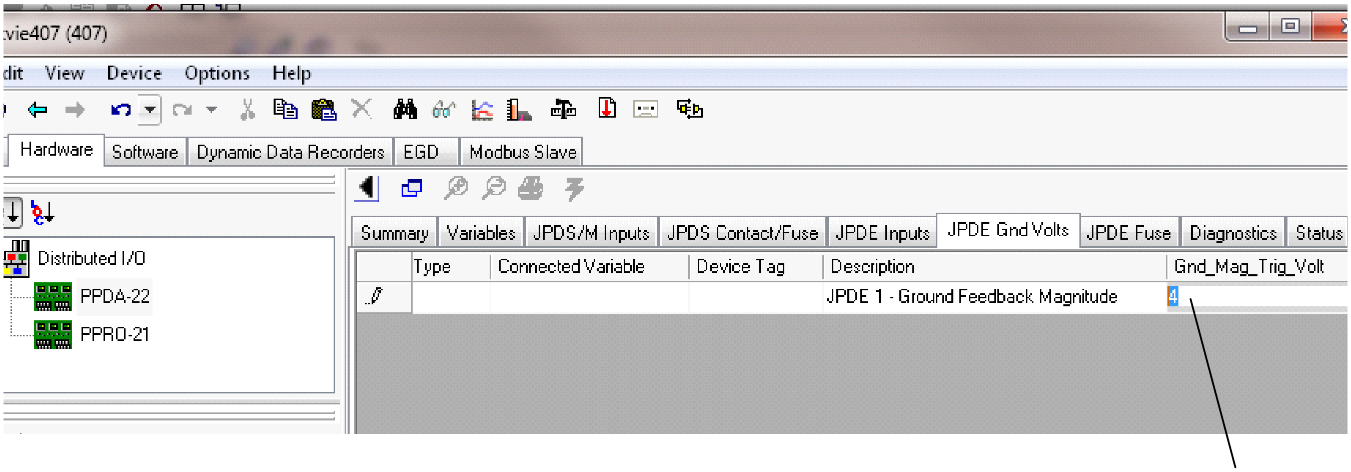
- A DC-37 pin connector on the underside of the I/O pack connects directly to the discrete input terminal board. The connector contains the 24 input signals, ID signal, relay coil power, and feedback multiplex command.
- An RJ-45 Ethernet connector named ENET1 on the side of the pack is the primary system interface.
- A second RJ-45 Ethernet connector named ENET2 on the side of the pack is the redundant or secondary system interface.
- A 3-pin power connector on the side of the I/O pack is for 28 V dc power for the I/O pack and terminal board.

5.1.2.2 Ground Fault Detection

If using TBCIH4C or STCIH8A terminal boards, set the PPDA I/O pack, JPDE Gnd Volts, Ground Fault Threshold Feedback Magnitude (GND_Mag_Trig_Volt) limit at 4 V dc. Ground faults are annunciated when an excitation voltage output is grounded. The current limiting resistor in series with each excitation voltage output requires a lower threshold for ground fault detection.

➢ To set the ground fault threshold

1. From the ToolboxST application, Component Editor, Hardware Tab, Tree View, select the PPDA I/O pack that is attached to the JPDE power distribution board.
2. From the Summary View, select the **JPDE Gnd Volts** tab.


vie407 (407)
dit View Device Options Help
Hardware Software Dynamic Data Recorders EGD Modbus Slave
Distributed I/O
PPDA-22
PPRO-21
Summary Variables JPDS/M Inputs JPDS Contact/Fuse JPDE Inputs JPDE Gnd Volts JPDE Fuse Diagnostics Status

Type	Connected Variable	Device Tag	Description	Gnd_Mag_Trig_Volt
			JPDE 1 - Ground Feedback Magnitude	4

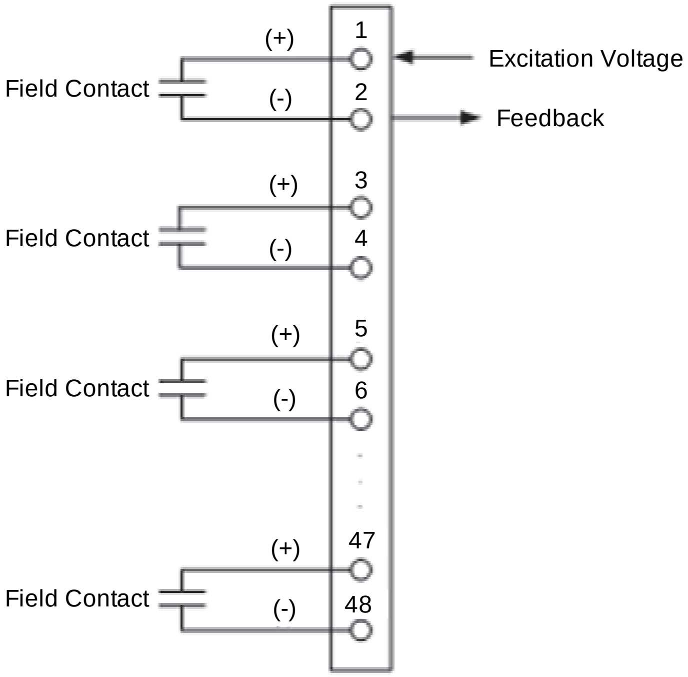
Change the value to 4.

5.1.2.3 Excitation Channels

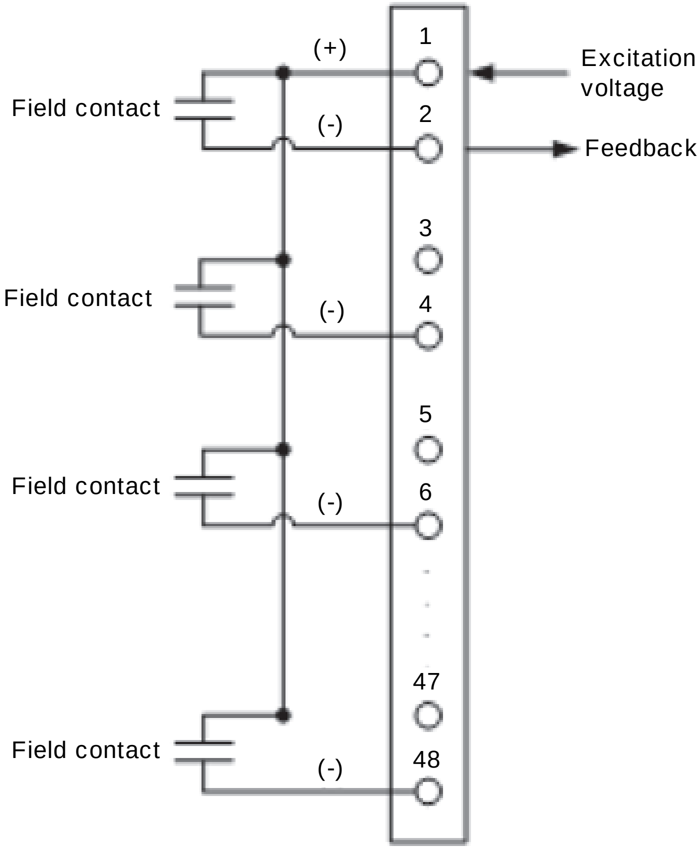
Warning

For TBCIH4C and STCIH8A, each excitation voltage output can connect to only one field contact. In the application world, this is known as *home run* wiring. Branching one excitation voltage output to multiple contacts will cause misoperation and is not allowed. Grounding multiple excitation voltage outputs is not allowed as this will result in self-test failures or diagnostic alarms, as well as overheating of the terminal board.

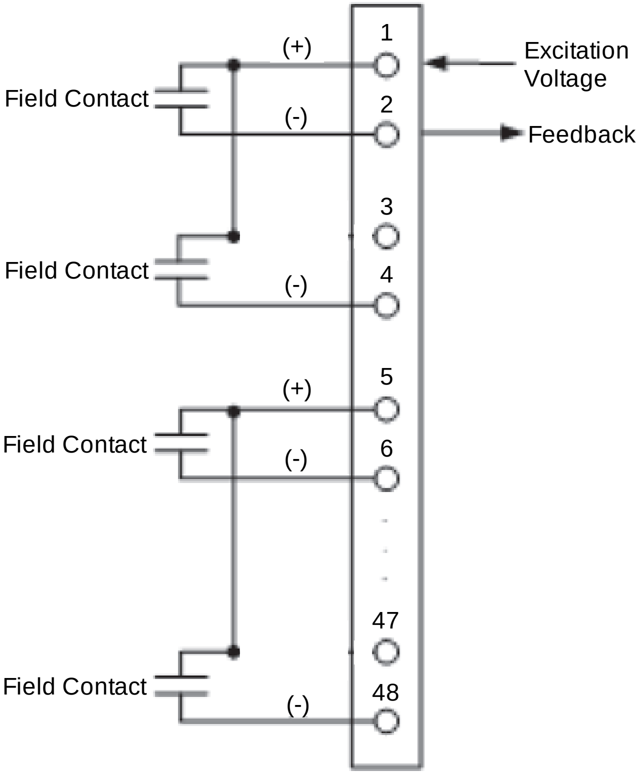
The following figures display correct configuration of excitation voltage channels based on compatible terminal board.



Correct Excitation Voltage Channels with TBCIH4C and STCIH8A



One Excitation Voltage Channel for Multiple Field Contacts with TBCI_1C, 2C, 3C, and STCI_1A, 2A, 4A, 6A



Mixed Excitation Voltage of Different Channels with TBCI_1C, 2C, 3C, and STCI_1A, 2A, 4A, 6A

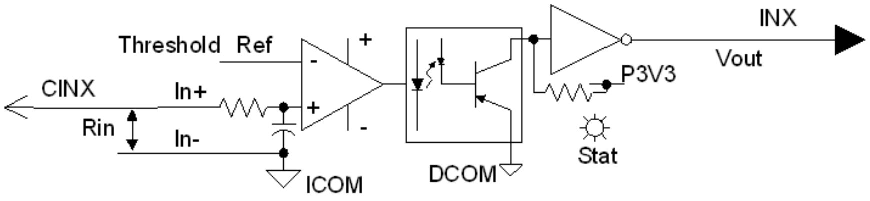
5.1.3 Operation

The following features are common to the distributed I/O modules:

- *BPPx Processor*
- *Processor LEDs*
- *Power Management*
- *ID Line*
- *I/O Module Common Diagnostic Alarms*

5.1.3.1 Input Signals

The discrete input acquisition board provides the second stage of signal conditioning and level shifting to interface the terminal board inputs to the control logic. Initial signal conditioning is provided on the terminal board. The discrete input acquisition input circuit is a comparator with a variable threshold. Each input is isolated from the control logic through an opto-coupler and an isolated power supply. The inputs are not isolated from each other. Each of the twenty-four inputs has filtering, hysteresis, and a yellow status LED, that indicates when an input is picked up. The LED will be OFF when the input is dropped-out.



5.1.3.2 Variable Threshold

The input threshold is derived from the contact wetting voltage input terminal. In most applications this voltage is scaled to provide a 50% input threshold. This threshold is clamped to 13% to prevent an indeterminate state if the contact wetting voltage drops to zero. If the contact wetting voltage drops below 40% of the nominal voltage, the under-voltage detector annunciates this condition to the control. A special test mode is provided to force the inputs from the control pack. Every four seconds, the threshold is pulsed high and then low and the response of the opto-couplers is checked. Non-responding inputs are alarmed.

5.1.4 Specifications

Item	PDIA Specification
Number of channels	24 dry contact voltage input channels
Input isolation in I/O pack	Optical isolation to 1500 V on all inputs
Input Filter	Hardware filter, 4 ms
Ac voltage rejection	60 V rms at 50/60 Hz at 125 V dc excitation
Frame rate	System dependent scan rate for control purposes 1,000 Hz scan rate for sequence of events monitoring
Fault detection	Loss of contact input excitation voltage Non-responding contact input in test mode Incorrect terminal board
† Ambient rating for enclosure design	PDIAH1B is rated from -40 to 70°C (-40 to 158 °F) PDIAH1A is rated from -30 to 65°C (-22 to 149 °F)

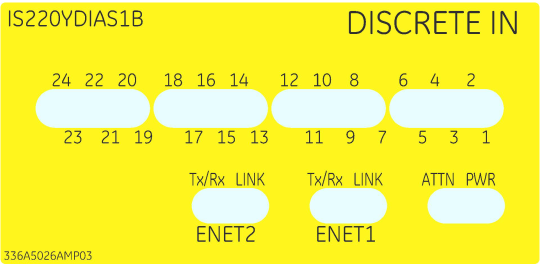
Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

5.1.5 Diagnostics

The I/O pack performs the following self-diagnostic tests:

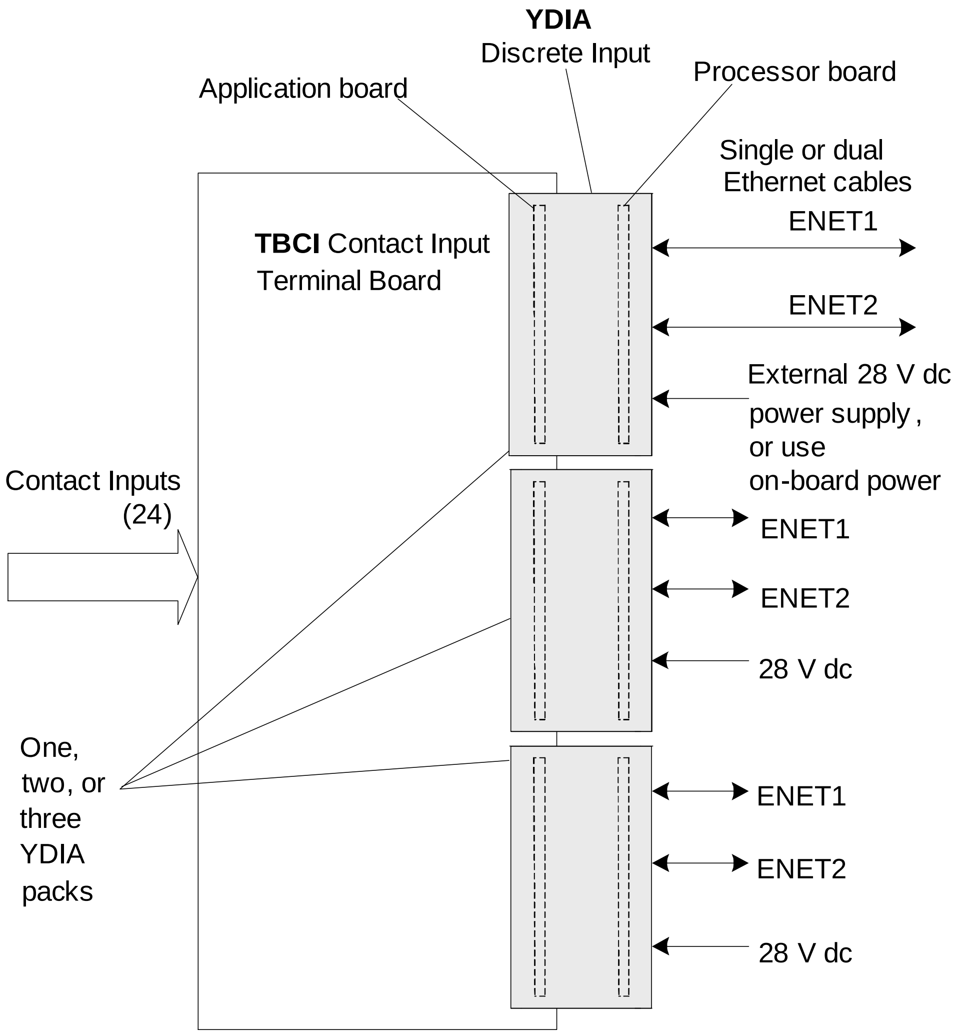
- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set
- Monitoring for loss of contact input excitation voltage on the terminal board
- Detecting a non-responding contact input during diagnostic test. In this test, the threshold is pulsed high and low and the response of the opto-couplers is checked.

5.2 Mark VIeS YDIA Discrete Input Pack



The Discrete Input (YDIA) pack provides the electrical interface between one or two I/O Ethernet networks and a discrete input terminal board. The YDIA contains a common processor board and an acquisition board specific to the discrete input function. The YDIA I/O pack accepts up to 24 contact inputs and terminal board specific feedback signals, and supports three different voltage levels.

System input to the pack is through dual RJ-45 Ethernet connectors and a three-pin power input. Discrete signal input is through a DC-37 pin connector that connects directly with the associated terminal board connector. Visual diagnostics are provided through indicator LEDs.



5.2.1 YDIA Compatibility

The YDIA I/O pack contains an internal processor board. The following table lists the available versions of the YDIA.

YDIA Version Compatibility

I/O Pack	Processor Board	Compatible (Supported) Firmware	ControlST Software Suite Versions
YDIAS1A	BPPB	V04.06	Supported in V04.06 and all later versions
YDIAS1B	BPPC	V05.01 and later	Supported in V06.01 and later versions

Attention

YDIAS1A and YDIAS1B I/O pack versions cannot be mixed on the same T-type terminal board.

All YDIA I/O packs in a Dual or TMR set must be the same hardware form.

To upgrade or replace the YDIA, refer to the following replacement procedures for specific instructions:

- *Replace Mark VIeS Safety I/O Pack with Same Hardware Form*
- *Replace Mark VIeS Safety I/O Pack with Upgraded Hardware Form*

The YDIA I/O pack is compatible with seven discrete contact input terminal boards, including the TBCI and STCI boards.

YDIA Terminal Board Compatibility

Terminal Board	Description	I/O Pack Redundancy		
		Simplex	Dual	TMR
TBCIS1, S2, S3	TMR Contact input terminal board with group isolation	Yes	Yes	Yes
STCIS1A, S2A, S4A, and S6A	Simplex Contact input terminal board	Yes	No	No

I/O pack redundancy refers to the number of I/O packs used in a signal path, as follows:

- Simplex uses one I/O pack.
- Dual uses two I/O packs.
- TMR uses three I/O packs.

5.2.2 Installation

➢ **To install the YDIA pack**

1. Securely mount the desired terminal board.
2. Directly plug one YDIA for simplex or three YDIAs for TMR into the terminal board connectors.
3. Mechanically secure the pack(s) using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right-angle force applied to the DC-37 connector between the pack and the terminal board. The adjustment should only be required once in the life of the product.
4. Plug in one or two Ethernet cables depending on the system configuration. The pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
5. Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to insert this connector with the power removed from the cable as the YDIA has inherent soft-start capability that controls current inrush on power application.
6. Use the ToolboxST application to configure the YDIA as necessary.

Note The YDIA mounts directly on a TBCI or STCI terminal board. Simplex terminal boards have a single DC-37 pin connector that receives the YDIA. TMR-capable terminal boards (TBCI) have three DC-37 pin connectors, with the JR1 connector used for Simplex operation; JR1 and JS1 are used for Dual operation; JR1, JS1, and JT1 are used for TMR operation.

5.2.2.1 Connectors

YDIA contains the following connectors:

- A DC-37 pin connector on the underside of the YDIA pack connects directly to the discrete input terminal board. The connector contains the 24 input signals, ID signal, relay coil power, and feedback multiplex command.
- An RJ45 Ethernet connector named ENET1 on the side of the pack is the primary system interface.
- A second RJ45 Ethernet connector named ENET2 on the side of the pack is the redundant or secondary system interface.
- A 3-pin power connector on the side of the pack is for 28 V dc power for the pack and terminal board.

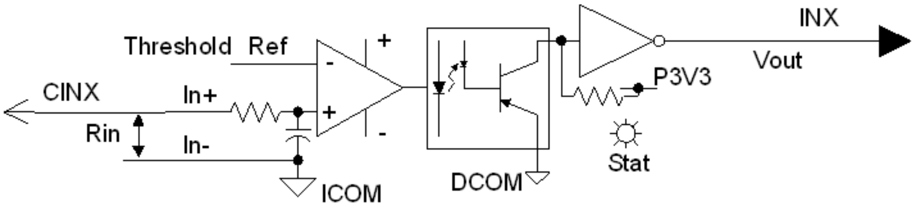
5.2.3 Operation

The following features are common to the distributed I/O modules:

- *BPPx Processor*
- *Processor LEDs*
- *Power Management*
- *ID Line*
- *I/O Module Common Diagnostic Alarms*

5.2.3.1 Input Signals

The discrete input acquisition board provides the second stage of signal conditioning and level shifting to interface the terminal board inputs to the control logic. Initial signal conditioning is provided on the terminal board. The discrete input acquisition input circuit is a comparator with a variable threshold. Each input is isolated from the control logic through an opto-coupler and an isolated power supply. The inputs are not isolated from each other. Each of the twenty-four inputs has filtering, hysteresis, and a yellow status LED, which indicates when an input is picked up. The LED will be OFF when the input is dropped-out.



5.2.3.2 Variable Threshold

The input threshold is derived from the contact wetting voltage input terminal. In most applications this voltage is scaled to provide a 50% input threshold. This threshold is clamped to 13% to prevent an indeterminate state if the contact wetting voltage drops to zero. If the contact wetting voltage drops below 40% of the nominal voltage, the under-voltage detector annunciates this condition to the control. A special test mode is provided to force the inputs from the control pack. Every four seconds, the threshold is pulsed high and then low and the response of the opto-couplers is checked. Non-responding inputs are alarmed.

5.2.4 Specifications

Item	YDIA Specification
Number of relay channels	24 dry contact voltage input channels
Input isolation in pack	Optical isolation to 1500 V on all inputs
Input filter ac voltage rejection	Hardware filter, 4 ms 60 V rms, 50/60 Hz at 125 V dc excitation
Frame rate	System dependent scan rate for control purposes 1,000 Hz scan rate for sequence of events monitoring
Fault detection	Loss of contact input excitation voltage Non-responding contact input in test mode Incorrect terminal board
Size	8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in. x 1.65 in. x 4.78 in.)
Technology	Surface-mount
† Ambient rating for enclosure design	-30 to 65°C (-22 to 149 °F)

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

5.2.5 Diagnostics

The I/O pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set
- Monitoring for loss of contact input excitation voltage on the terminal board
- It detects a non-responding contact input during the diagnostic test. In this test, the threshold is pulsed high and low and the response of the opto-couplers is checked.

Details of the individual diagnostics are available in the ToolboxST application. The diagnostic signals can be individually latched, and then reset with the RSTDIAG signal if they go healthy.

5.2.5.1 YDIA Status LEDs

Discrete Input LEDs

LED	Label	Description
Yellow	Input #	Provided for each of the 24 inputs to indicate when they are energized

Note Refer to the Common I/O Module Functionality, *Processor LEDs* section.

5.3 PDIA or YDIA Configuration

5.3.1 Parameters

Parameter	Description	Choices
ContactInput	Mark a specific contact input as Used or Unused.	Used, Unused
SignalInvert	Inversion makes signal true if contact is open	Normal, Invert
SeqOfEvents	Record contact transitions in sequence of events	Enable, Disable
DiagVoteEnab	Enable voting disagreement diagnostic	Enable, Disable
Signal Filter	Contact input filter in milliseconds	Zero, Ten, Twenty, Fifty, Hundred

5.3.2 Inputs

Input	Direction	Type
Contact01	Input	BOOL
↓	↓	↓
Contact24	Input	BOOL

5.3.3 Variables

Note The following variable names are displayed differently depending on redundancy of I/O pack (R, S, or T) and if this is a PDIA or YDIA pack.

Variable	Description	Direction	Type
L3DIAG_PDIA_x L3DIAG_YDIA_x	I/O diagnostic indication, where x is R, S, or T	Input	BOOL
LINK_OK_PDIA_x LINK_OK_YDIA_x	I/O link okay indication, where x is R, S, or T		BOOL
ATTN_PDIA_x ATTN_YDIA_x	I/O attention indication, where x is R, S, or T		BOOL
IOPackTmpr_x	I/O pack temperature, where x is R, S, or T		REAL
PS18V_PDIA_x PS18V_YDIA_x	I/O 18 V power supply indication, where x is R, S, or T		BOOL
PS28V_PDIA_x PS28V_YDIA_x	I/O 28 V power supply indication, where x is R, S, or T		BOOL

5.4 PDIA or YDIA Specific Alarms

The following alarms are specific to the PDIA or YDIA I/O pack.

56-79

Description Contact Input [ ] not responding to self-test mode

Possible Cause The input hardware internal to the I/O pack has experienced a failure.

Solution Replace the I/O pack.

80-143

Description Logic Signal [ ] Voting Mismatch

Possible Cause

- In a TMR application, the values for the specified contact do not agree between the R, S, and T I/O packs.
- A contact input is toggling at the same rate as the configured input filter.

Solution

- Verify that R, S, and T I/O packs are equal with ToolboxST configuration.
- Check the I/O pack power and networking.
- Check the I/O pack mounting on terminal board.
- Check to see if a contact input is toggling at the same rate as the input filter. If so, resolve the cause of the toggling contact input.
- Replace the I/O pack.

240

Description Excitation Voltage not valid, Contact Inputs not valid

Possible Cause The contact excitation voltage applied to the terminal board is not within the acceptable range for the board.

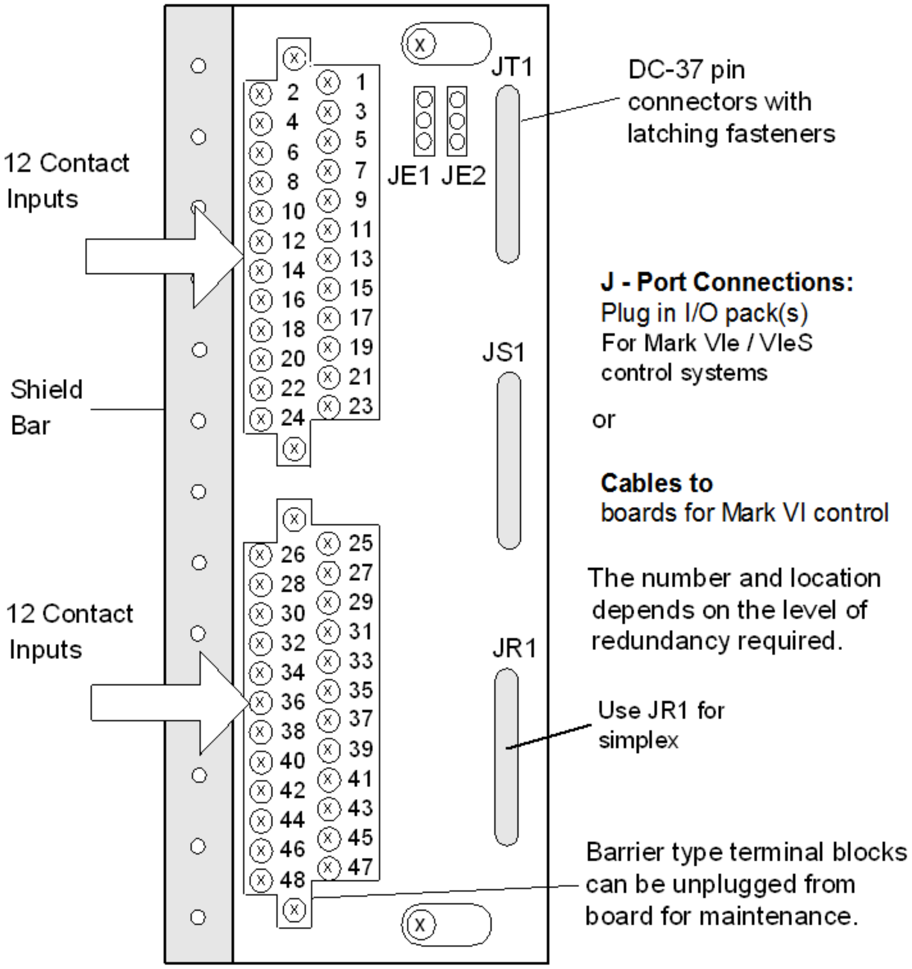
Solution Check power distribution and wiring to ensure that the correct excitation voltage is applied to the terminal board.

5.5 TBCIH#C, S#C Contact Input with Group Isolation

The Contact Input with Group Isolation (TBCI) terminal board accepts 24 dry contact inputs wired to two barrier-type terminal blocks. For contact excitation, dc power is wired to TBCI. The contact inputs have noise suppression circuitry to protect against surge and high-frequency noise.

Caution

Some panels contain a mixture of ac and dc wetting voltages. To prevent misoperation and damage these terminal boards, care must be taken to avoid connecting the ac wetting voltages to the terminal board wetting voltage inputs. Furthermore, verify that the ac wetting voltages and the dc wetting voltages are not inadvertently cross-connected.



12 Contact Inputs
Shield Bar
12 Contact Inputs
1
2
3
4
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14
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16
17
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47
48
JT1
JE1
JE2
JS1
JR1
DC-37 pin connectors with latching fasteners
J - Port Connections:
Plug in I/O pack(s)
For Mark VIe / VIeS control systems
or
Cables to
boards for Mark VI control
The number and location depends on the level of redundancy required.
Use JR1 for simplex
Barrier type terminal blocks can be unplugged from board for maintenance.

Contact Input Terminal Board

5.5.1 Compatibility

The TBCI supports simplex, dual, and TMR redundancy. One, two, or three I/O packs can be plugged directly into the TBCI.

Version	Wetting Voltage	Hazloc certified	IEC61508 certified with YDIA pack
TBCIH1A †	125 V dc	No	No
TBCIH1B †			
TBCIH1C			
TBCIH2B †	24 V dc		
TBCIH2C			
TBCIH3C	48 V dc		
TBCIH4C	24 V dc	Yes	
TBCIS1C	125 V dc	No	Yes
TBCIS2C	24 V dc		
TBCIS3C	48 V dc		
† These terminal board revisions are legacy so they are no longer in production			

5.5.2 TBCI Installation

Connect the wires for the 24 dry contact inputs directly to two I/O terminal blocks on the terminal board. These blocks are held down with two screws and can be unplugged from the board for maintenance. Each block has 24 terminals accepting up to #12 AWG wires. A shield terminal strip attached to chassis ground is located immediately to the left of each terminal block.

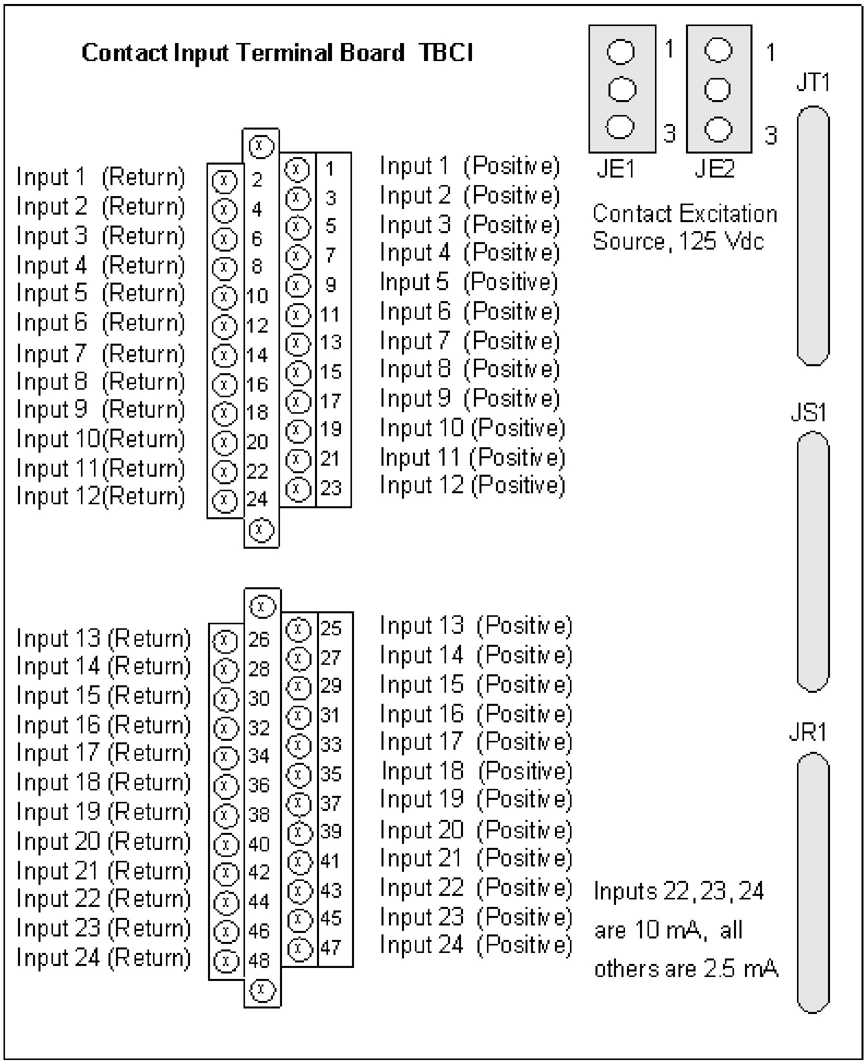
In a Simplex system, connect the I/O pack into the TBCI connector JR1. In a Dual system, plug the I/O packs into JR1 and JS1. In a TMR system, plug the I/O packs into JR1, JS1, and JT1. The I/O pack(s) attach to side-mounting brackets. One or two Ethernet cables plug into the I/O packs. Connect TBCI to the contact excitation voltage source using plugs JE1 and JE2.

Caution

Do not replace TBCIH2C with TBCIH4C unless having ControlST software suite 4.05 or higher.

Attention

The TBCIH4C should not be used with external intrinsic safety barriers.



J-port Connections
Use all three for TMR

Use JR1 and JS1 for dual

Use JR1 for simplex

Terminal Blocks can be unplugged from terminal board for maintenance

Up to two #12 AWG wires per point with 300 volt insulation

TBCI Wiring and Cabling

5.5.3 Operation

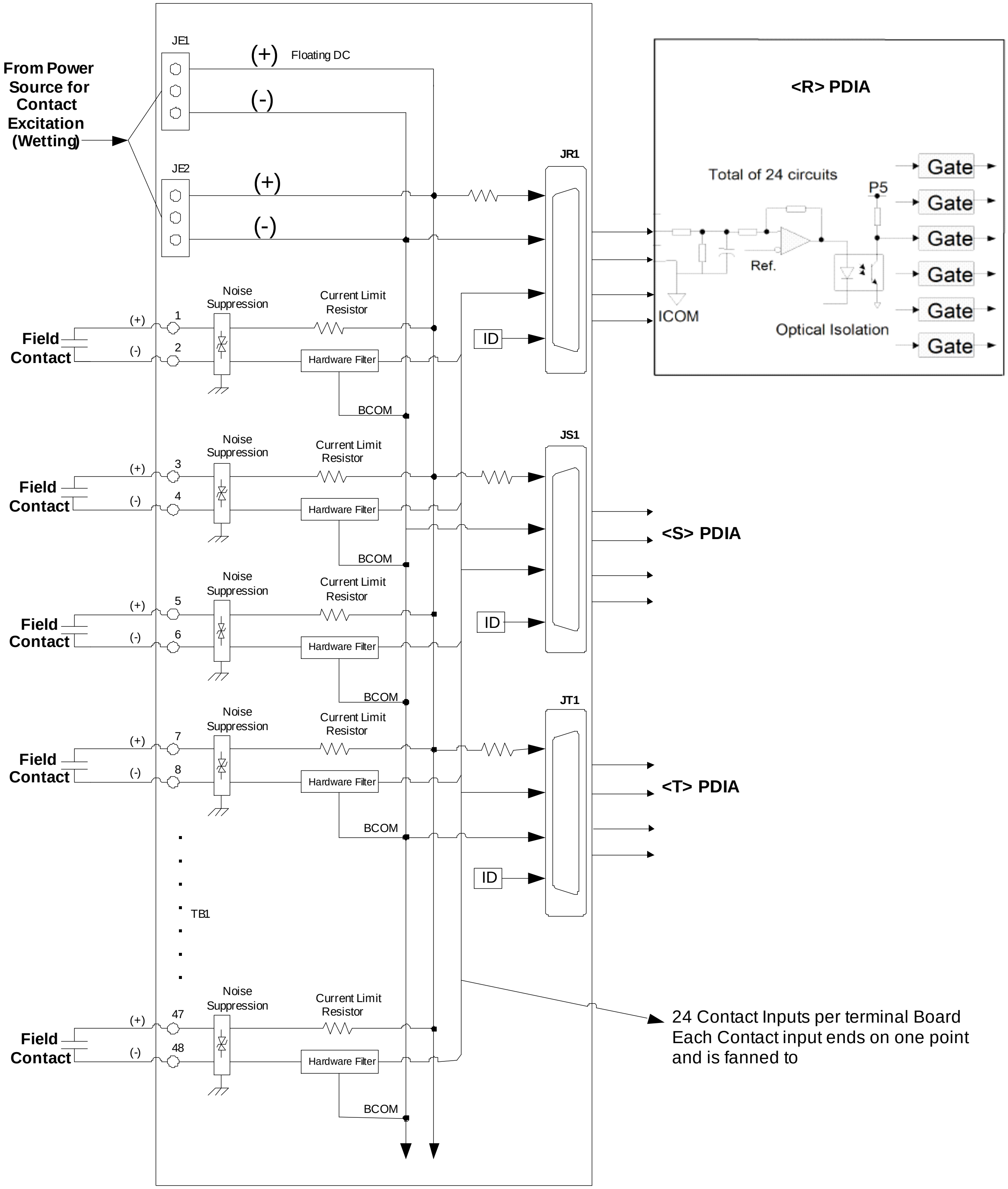
Filters reduce high-frequency noise and suppress surge on each input near the point of signal entry. The dry contact inputs on TBCIH1C and S1C are powered from a floating 125 V dc (100-140 V dc) supply from the control cabinet. The 125 V dc bus is current limited in the power distribution module prior to feeding each contact input. The other terminal board versions use lower voltages. Refer to the section, *TBCI Specifications*.

Note A current limit resistor is only available on the Mark VIe TBCIH4C.

Discrete input voltage signals pass to the I/O pack, which sends them through optical isolators providing group isolation, and transfers the signals to the Mark VIe or Mark VIeS controller. The reference voltage in the isolation circuits sets a transition threshold that is equal to 50% of the applied floating power supply voltage. The tracking is clamped to go no less than 13% of the nominal rated supply voltage to force all contacts to indicate open when voltage dips below this level.

A pair of terminal points is provided for each input, with one point (screw) providing the positive dc source and the second point providing the return (input) to the board. The current loading is 2.5 mA per point for the first 21 inputs on each terminal board. The last three have a 10 mA load to support interface with remote solid-state output electronics. Contact input circuitry is designed for NEMA Class G creepage and clearance.

In the following figure, the Mark VIe TBCIH4C contact input section has a current limit resistor on each wetting voltage output.



Mark VIe TBCIH4C Contact Input Circuits

5.5.4 TBCI Specifications

Item	TBCI Specification
Number of channels	24 contact voltage input channels
Excitation voltage	H1 and S1: Nominal 125 V dc, floating, ranging from 100 to 140 V dc
	H2 and S2: Nominal 24 V dc, floating, ranging from 18.5 to 32 V dc H4: Nominal 24 V dc, floating or grounded, ranging from 18.5 to 31 V dc
	H3 and S3: Nominal 48 V dc, floating, ranging from 32 to 60 V dc
Input current	H1 and S1 (for 125 V dc applications): First 21 circuits draw 2.5 mA (50 kΩ) Last three circuits draw 10 mA (12.5 kΩ)
	H2, S2 , H4 (for 24 V dc applications): First 21 circuits draw 2.5 mA (10 kΩ) Last three circuits draw 9.9 mA (2.40 kΩ)
	H3 and S3 (for 48 V dc applications): First 21 circuits draw 2.5 mA Last three circuits draw 10 mA
Input filter	Hardware filter, 4 ms
Power consumption	20.6 W on the terminal board
Fault detection	Loss of contact input excitation voltage Non-responding contact input in test mode Unplugged cable or loss of communication with I/O board: contact status is displayed as False and Unhealthy.
Size	33.02 cm high x 10.16 cm wide (13.0 in x 4.0 in)

5.5.5 TBCI Diagnostics

Diagnostic tests to components on the terminal boards are as follows:

- The excitation voltage is monitored. If the excitation drops to below 40% of the nominal voltage, a diagnostic alarm is set and latched by the I/O pack.
- PDIA or YDIA I/O pack performs periodic self test of all contact inputs. In a alternative sequence each contact is forced open or closed and reads the status, if any contact fails the test a fault is created.
- If the input from this board does not match the TMR voted value from all three boards, a fault is created.
- Each terminal board connector has its own ID device that is interrogated by the I/O pack. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the JR1/JS1/JT1 connector location. When the chip is read by the I/O pack and a mismatch is encountered with what is configured in the ToolboxST application, a hardware incompatibility fault is created.

5.6 TICIH#A Contact Input with Point Isolation

The Contact Input with Point Isolation (TICI) terminal board provides 24 point isolated voltage detection circuits to sense a range of voltages across relay contacts, fuses, and switches.

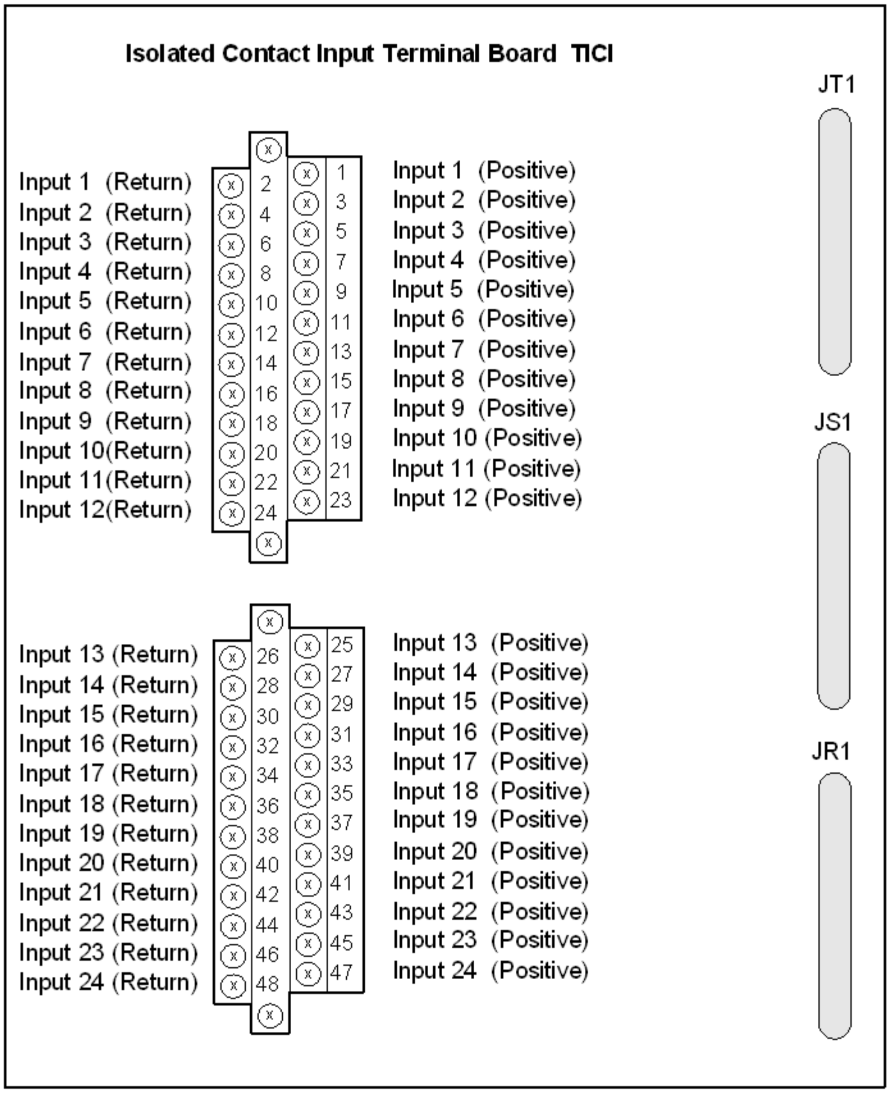
Caution

Some panels contain a mixture of ac and dc wetting voltages. To prevent misoperation and damage these terminal boards, care must be taken to avoid connecting the ac wetting voltages to the terminal board wetting voltage inputs. Furthermore, verify that the ac wetting voltages and the dc wetting voltages are not inadvertently cross-connected.

5.6.1 Installation

Connect the wires for the 24 isolated digital inputs directly to two I/O terminal blocks on the terminal board. These blocks are held down with two screws and can be unplugged from the board for maintenance. Each block has 24 terminals accepting up to #12 AWG wires. A shield terminal strip attached to chassis ground is located immediately to the left of each terminal block.

In a Simplex system, connect the PDIA I/O pack to TICI using connector JR1. In a Dual system, connect PDIA I/O packs using connectors JR1 and JS1. In a TMR system, connect the PDIAs to TICI using connectors JR1, JS1, and JT1.



J - Port Connections:

Plug in PDIA I/O Pack(s)
for Mark VIe control

or

Cables to VCCC board(s)
in the Mark VI control

The number and location
depends on the level of
redundancy required.

Terminal Blocks can be unplugged
from terminal board for maintenance

Up to two #12 AWG wires per
point with 300 volt insulation

TICI Terminal Board Wiring and Cabling

5.6.2 Operation

The TICI is similar to other discrete input boards except for the following items:

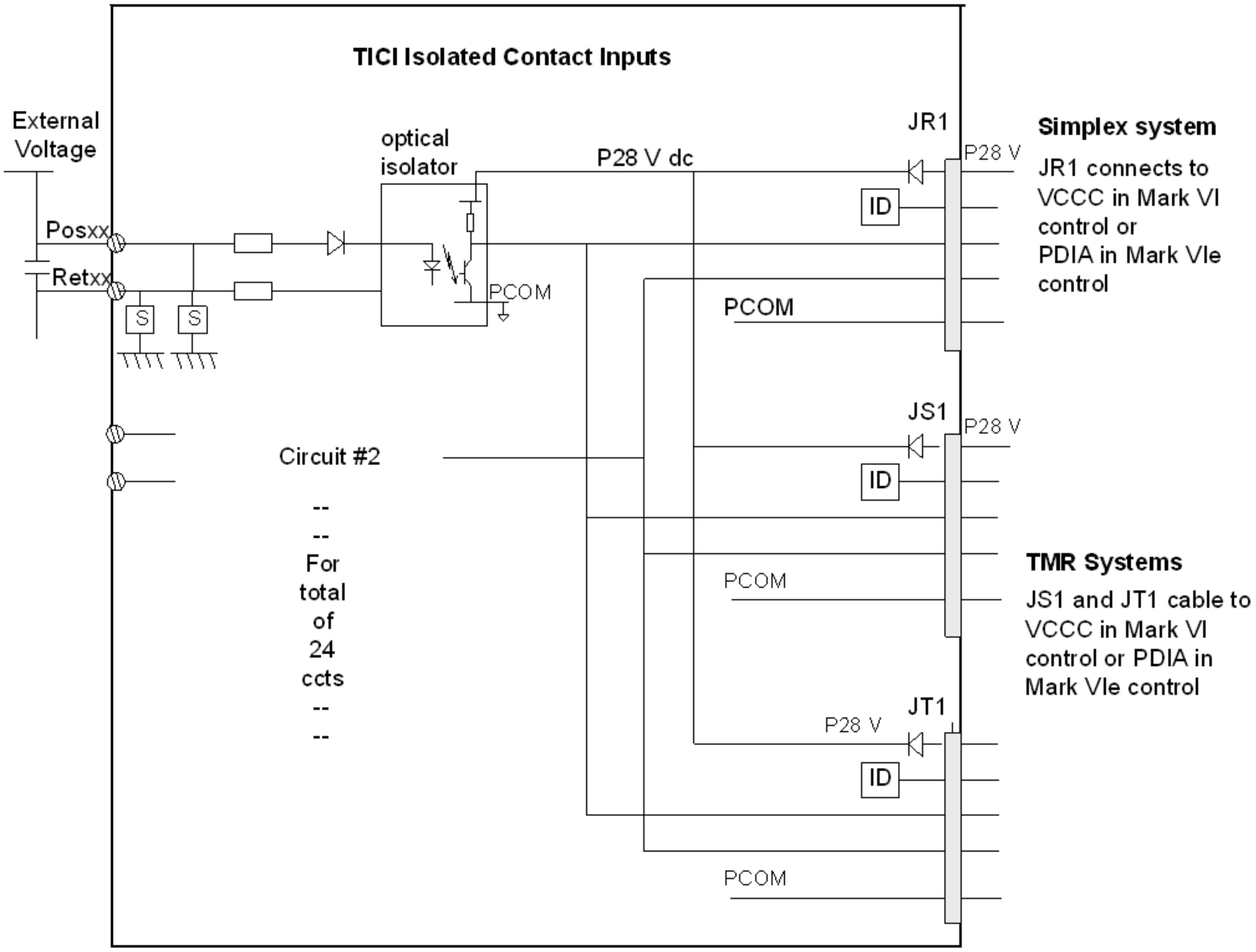
- No contact excitation is provided on the terminal board.
- Each input is electrically isolated from all others and from the active electronics.

There are two groups of the TICI with different nominal voltage thresholds: TICIH1A and TICIH2A. Refer to the section, *TICI Specifications* for input voltage ranges. TICI provides input hardware filtering with time delays of 15 ms, nominal:

- For dc applications the time delay is 15 ±8 ms
- For ac applications the time delay is 15 ±13 ms

In addition to hardware filters, the contact input state is software-filtered, using configurable time delays selected from 0, 10, 20, 50, and 100 ms. For ac inputs, a filter of at least 10 ms is recommended. The following restrictions should be noted regarding creepage and clearance on the 230 V rms application:

- For NEMA requirements: 230 V single-phase
- For CE Certification: 230 V single or 3-phase


TICI Isolated Contact Inputs
External Voltage
Posxx
Retxx
S
S
optical isolator
P28 V dc
PCOM
PCOM
Circuit #2
--
--
For total of 24 ccts
--
--
JR1
P28 V
ID
Simplex system
JR1 connects to VCCC in Mark VI control or PDIA in Mark VIe control
JS1
P28 V
ID
PCOM
TMR Systems
JS1 and JT1 cable to VCCC in Mark VI control or PDIA in Mark VIe control
JT1
P28 V
ID
PCOM

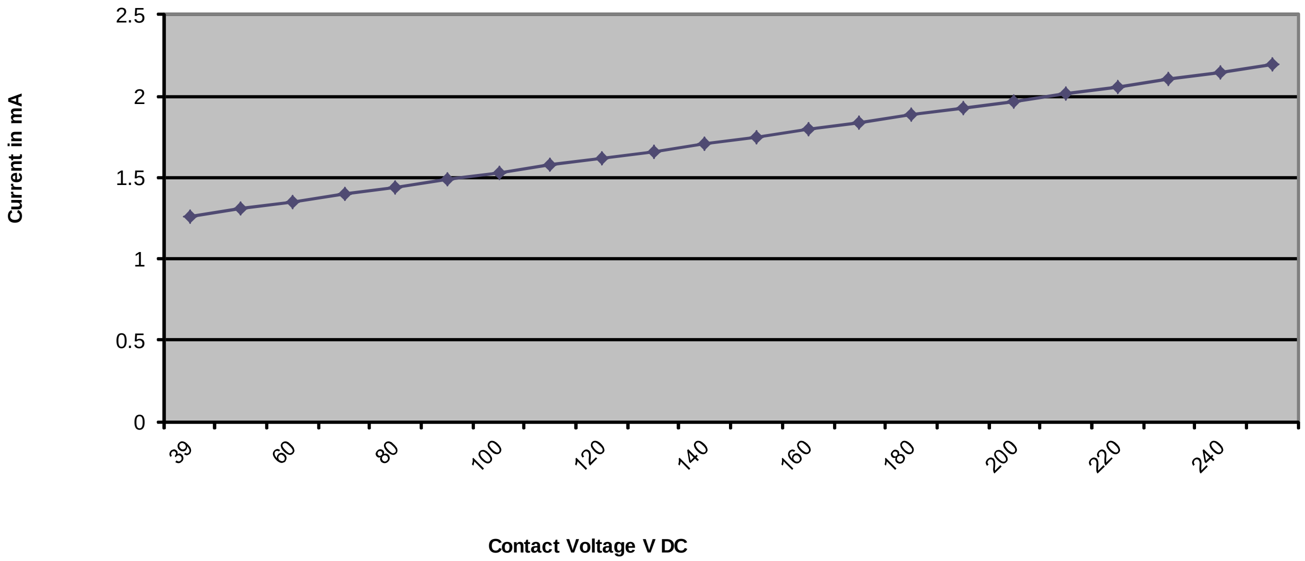
TICI Circuits for Sensing Voltage across Typical Device

5.6.3 Specifications

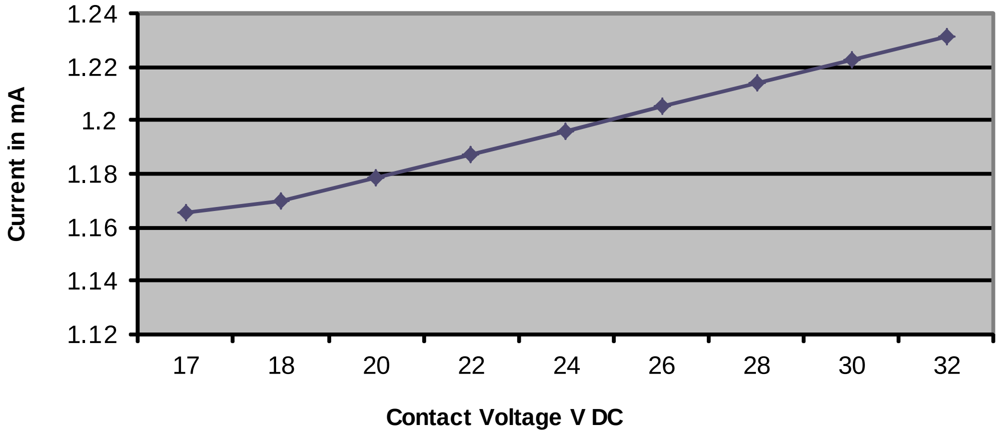
Item	**TICI Specification**
Number of channels	24 input channels for isolated voltage sensing
Input voltage	TICIH2A: 16-32 V dc, nominal 24 V dc, with a detection threshold of 9.5 to 15 V dc
	TICIH1A: 70 -145 V dc, nominal 125 V dc, with a detection threshold of 39 to 61 V dc 200 -250 V dc, nominal 250 V dc, with a detection threshold of 39 to 61 V dc 90 -132 V rms, nominal 115 V rms, 47-63 Hz, with a detection threshold of 35 to 76 V ac 190-264 V rms, nominal 230 V rms, 47-63 Hz, with a detection threshold of 35 to 76 V ac
Fault detection in I/O board	Non-responding contact input in test mode Loss of contact input excitation voltage Unplugged cable or loss of communication with I/O board: contact status is displayed as False and Unhealthy.
Size	17.8 cm high x 33.02 cm wide (7.0 in x 13.0 in)

5.6.3.1 Contact Current

TICIH1A Contact Current



TICIH2A Contact Current



5.6.4 TICI Diagnostics

Diagnostic tests to components on the terminal boards are as follows:

- The excitation voltage is monitored. If the excitation drops to below 40% of the nominal voltage, a diagnostic alarm is set and latched by the PDIA.
- PDIA performs periodic self test of all contact inputs. In a alternative sequence each contact is forced open or close and reads the status, if any contact fails the test a fault is created.
- If the input from this board does not match the TMR voted value from all three boards, a fault is created.
- Each terminal board connector has its own ID device that is interrogated by the PDIA. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the JR1/JS1/JT1 connector location. When the chip is read by the PDIA and a mismatch is encountered with what is configured in the ToolboxST application, a hardware incompatibility fault is created.

5.7 STCIH#A, S#A Simplex Contact Input

The Simplex Contact Input (STCI) terminal board is a compact contact input terminal board designed for DIN-rail or flat mounting. The STCI board accepts 24 contact inputs that are supplied with a nominal 24, 48, and 125 V dc excitation from an external source. The contact inputs have noise suppression to protect against surge and high-frequency noise. The I/O pack plugs into the D-type connector and communicates with the controller over Ethernet.

STCI Compatibility

Terminal Board	Wetting Voltage	Euro Style Box-type Terminals Blocks
STCIH1A	24 V dc	Fixed
STCIH2A	24 V dc	Pluggable
STCIH4A	48 V dc	
STCIH6A	125 V dc	
STCIH8A [1]	24 V dc	
STCIS1A [2]	24 V dc	Fixed
STCIS2A [2]	24 V dc	Pluggable
STCIS4A [2]	48 V dc	
STCIS6A [2]	125 V dc	
[1] This terminal board was designed specifically for use in hazardous locations.		
[2] These terminal boards are IEC 61508 safety certified when used with the Mark VIeS YDIA I/O pack.		

5.7.1 Installation

The STCI plus a plastic insulator mounts on a sheet metal carrier that then mounts on a DIN rail. Optionally, the STCI plus insulator mounts on a sheet metal assembly that then bolts in a cabinet. The contact inputs are wired directly to the terminal block, typically using #18 AWG wires. Shields should be terminated on a separate bracket. 52 terminals inputs are available.

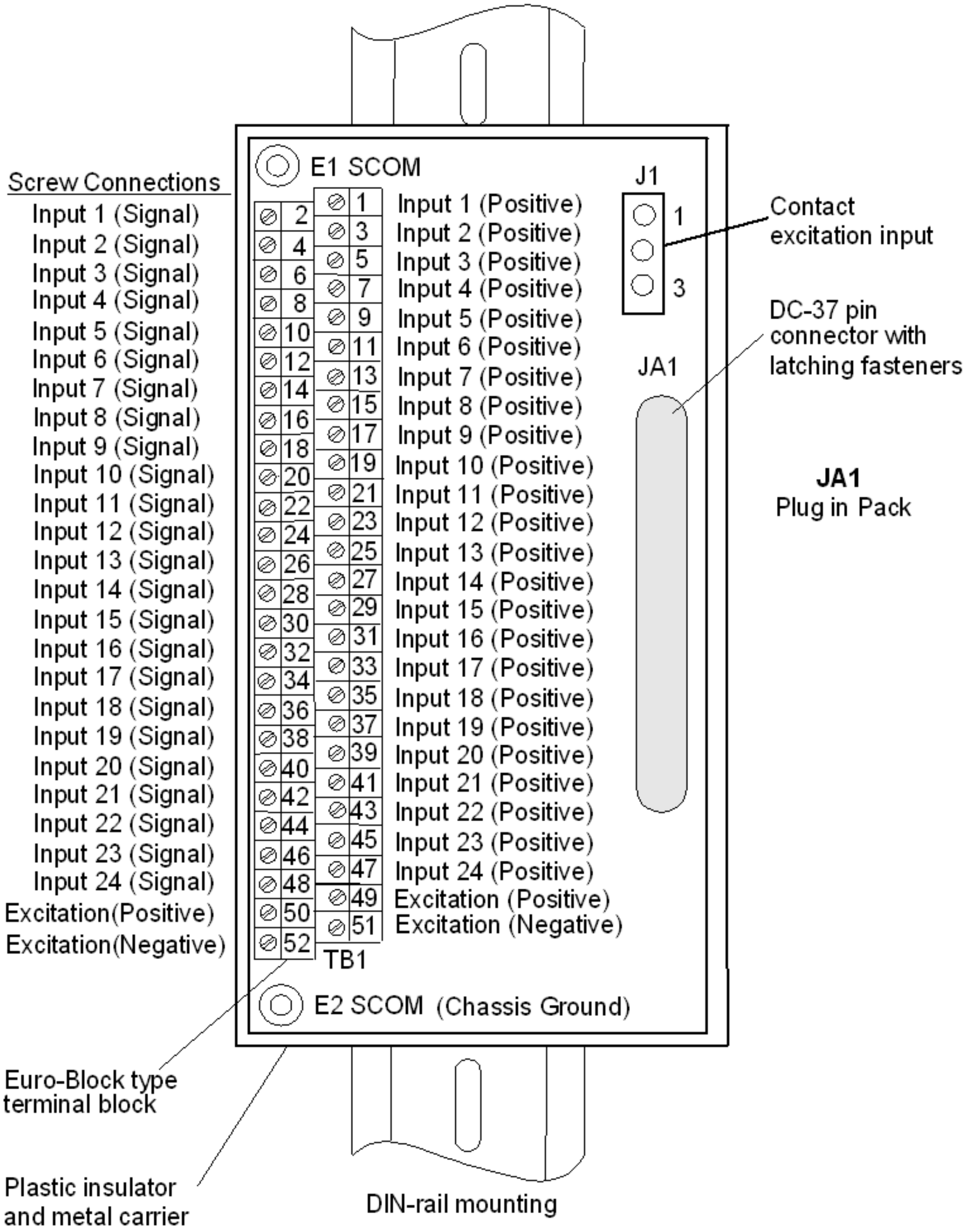
Note E1 and E2 are chassis grounding screws for SCOM.

Caution

Do not replace a Mark VIe STCIH2A with STCIH8A unless having ControlST software suite 4.05 or higher.

Attention

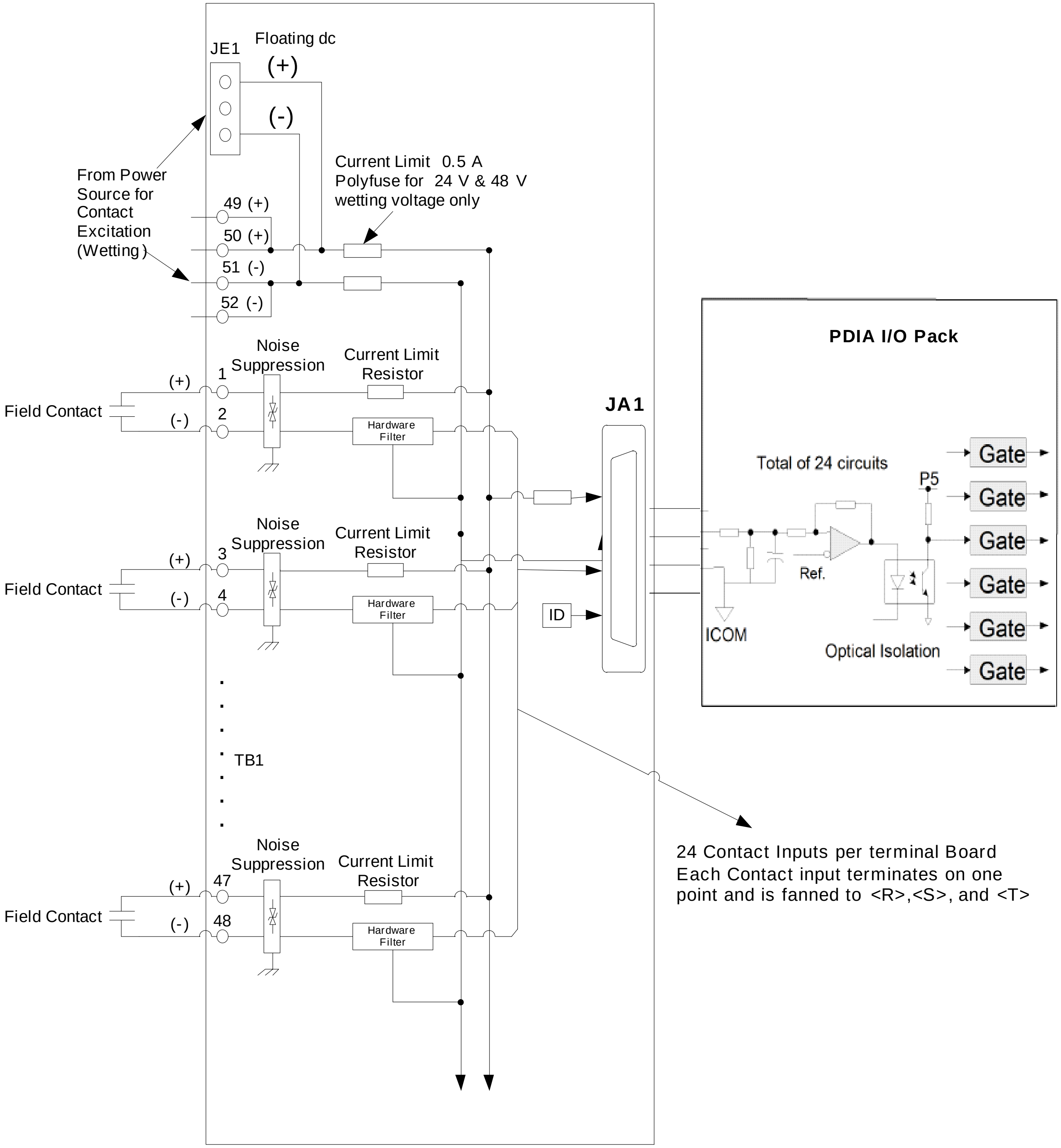
The Mark VIe STCIH8A terminal board should not be used with external intrinsic safety barriers.



Wiring to STCI Terminal Board

5.7.2 Operation

The function and on-board signal conditioning are the same as those on TBCI. The threshold voltage is 50% of the excitation voltage. A current limit resistor is only available on the Mark VIe STCIH8A. In the following figure, the Mark VIe STCIH8A contact input section has a current limit resistor on each wetting voltage output.



Mark VIe STCIH8A Contact Input Circuits

Contact input currents are resistance limited to 2.5 mA on the first 21 circuits, and 10 mA on circuits 22 through 24. The combined contact excitation current is current limited to 0.5 A using polymer positive temperature coefficient fuses that can be reset. Filters reduce high-frequency noise and suppress surge on each input near the point of signal entry. The discrete input voltage signals go to the I/O pack, which passes them through optical isolators, converts them to digital signals, and transfers them to the controller.

5.7.3 Specifications

Item	STCI Specification
Number of channels	24 dry contact voltage input channels
Excitation voltage	H1 and S1: Nominal 24 V dc, floating, ranging from 18.5 to 32 V dc (Fixed TB) H2 and S2: Nominal 24 V dc, floating, ranging from 18.5 to 32 V dc (Pluggable TB) H4 and S4: Nominal 48 V dc, floating, ranging from 32 to 60 V dc (Pluggable TB) H6 and S6: Nominal 125 V dc, floating, ranging from 100 to 140 V dc (Pluggable TB) H8: Nominal 24 V dc, floating or grounded, ranging from 18.5 to 31 V dc (Pluggable TB)
Input current	H1 and S1: For 24 V dc applications: First 21 circuits each draw 2.5 mA (50 kΩ) Last three circuits each draw 10 mA (12.5 kΩ)
	H2, S2, H8: For 24 V dc applications: First 21 circuits draw 2.5 mA Last three circuits draw 10 mA
	H4 and S4: For 48 V dc applications: First 21 circuits draw 2.5 mA Last three circuits draw 10.4 mA
	H6 / S6: For 125 V dc applications: First 21 circuits draw 2.55 mA Last three circuits draw 10 mA
Input filter	Hardware filter, 4 ms
Fault detection in I/O board	Loss of contact input excitation voltage Non-responding contact input in test mode Unplugged cable or loss of communication with I/O board: contact status is displayed as False and Unhealthy.
Ac voltage rejection	12 V rms at 24 V dc excitation (H1, S1, H2, S2, H8) 24 V rms at 48 V dc excitation (H4 and S4) 60 V rms at 125 V dc excitation (H6 and S6)
Size	15.9 cm high x 10.2 cm wide (6.25 in x 4.0 in)
Technology	Surface-mount

5.7.4 Diagnostics

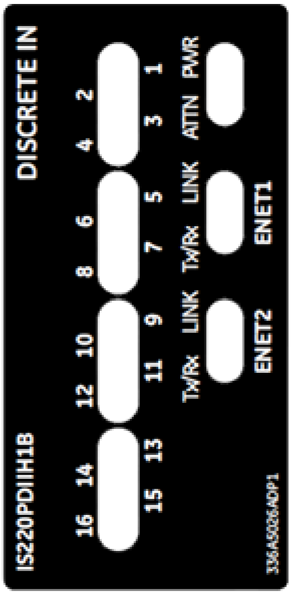
The I/O pack monitors the following functions on STCI:

- The contact excitation voltage is monitored. If the excitation drops to below 40% of the nominal voltage, a diagnostic alarm (fault) is set and latched.
- PDIA or YDIA performs periodic self test of all contact inputs. In a alternative sequence each contact is forced open or close and reads the status, if any contact fails the test a fault is created.
- The terminal board connector has an ID device that is interrogated by the I/O pack. The connector ID is coded into a read-only chip containing the board serial number, board type, and revision number. If a mismatch is encountered with what is configured in the ToolboxST application, a hardware incompatibility fault is created.

Notes

6 PDII Isolated Discrete Input Module

6.1 PDII Isolated Discrete Input Pack



The Isolated Discrete Input (PDII) provides the electrical interface between one or two I/O Ethernet networks (IONet) and a point/group isolated discrete input terminal board. The PDII contains a BPPx processor board and an acquisition board specific to the isolated discrete input function. The PDII accepts up to 16 isolated contact inputs that can be point isolated, group isolated, or a mix based on the terminal and optional board configurations. Each channel can accept different voltage levels as follows: 24 V dc/ 48 V dc/ 125 V dc/ 250 V dc/ 115 V ac rms / 230 V ac rms.

System input to the I/O pack is through dual RJ-45 Ethernet connectors and a three-pin power input. Discrete signal input is through a DC-37 pin connector that connects directly with the associated terminal board connector. Network, I/O pack, and contact input status is displayed on the I/O pack front LEDs.

6.1.1 Compatibility

The PDII includes one of the following compatible BPPx processor boards.

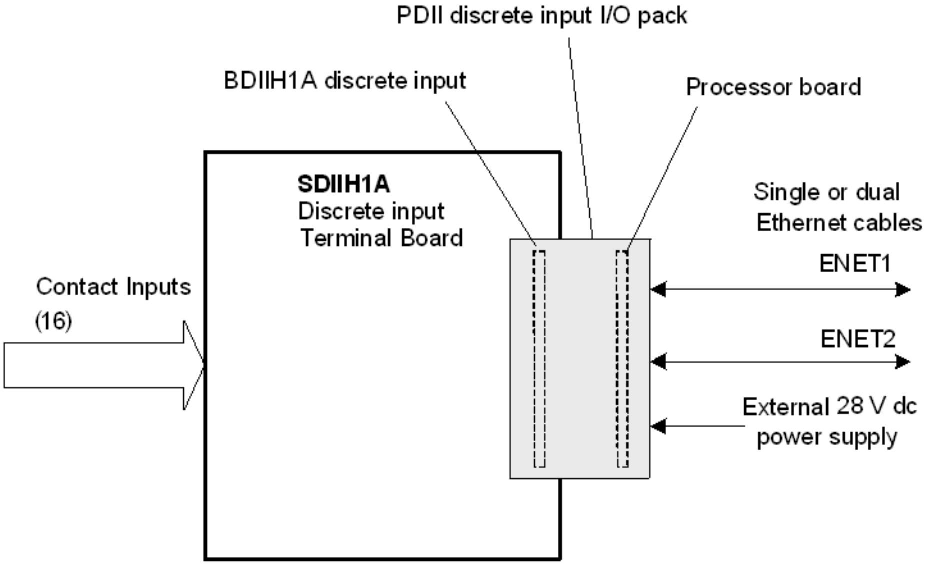
- The PDIIH1A contains a BPPB processor board.
- The PDIIH1B contains a functionally compatible BPPC that is supported in the ControlST***** software suite V04.03 and later.

If the PDII is used with terminal board SDII and the optional board WDIIH1, all 16 channels can be system wetted with 24 V dc, 115 V ac rms, or 230 V ac rms. When using WDIIH1, each of the 16 channels can be individually set and configured as point isolated and each channel can accept a different voltage level as needed. A mix of point isolation and group isolation is possible in this configuration.

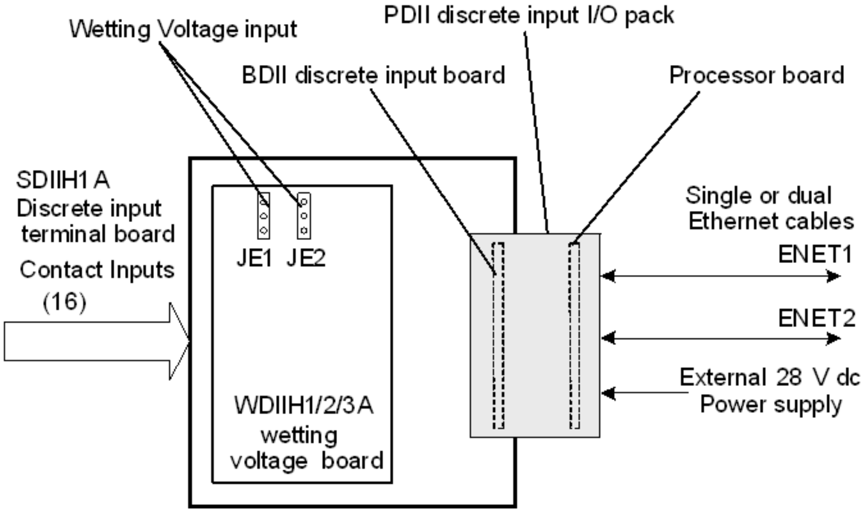
If the PDII is used with terminal board SDII and the optional board WDIIH2, all 16 channels can be system wetted with 48 V dc. When using WDIIH2, each of the 16 channels can be individually set and configured as point isolated and each channel can accept a different voltage level as needed. A mix of point isolation and group isolation is possible in this configuration.

If the PDII is used with terminal board SDII and the optional board WDIIH3, all 16 channels can only be system wetted with 125 V dc. With WDIIH3, there is no option provided to configure channels as point isolated.

The following figures display the PDII module with and without the optional WDII.



Point Isolated Representation –SDII+PDII



System Wetted Representation – SDII +WDII+PDII

6.1.2 Installation

➢ **To install the PDII**

1. Securely mount the desired terminal board.
2. Directly plug one PDII into the SDII simplex terminal board connectors. The terminal board can be with or without optional board as per the user requirement.
3. Mechanically secure the PDII using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that the right-angle force applied to the DC-37 pin connector between the PDII and the terminal board. The adjustment should only be required once in the service life of the product.

Note The PDII mounts directly on a SDII simplex terminal board, which has a single DC-37 pin connector to receive the PDII.

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4. Plug in one or two Ethernet cables depending on the system configuration. The pack operates over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
5. Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to remove power from the cable before plugging it in because the I/O pack has inherent soft-start capability that controls current inrush on power application.
6. Use the ToolboxST* application to configure the I/O pack as necessary. Refer to the diagrams in the section, *SDII Simplex Contact Input with Point Isolation, Functional Description* for the required configuration.

6.1.2.1 Connectors

The PDII contains the following connectors:

- The DC-37 pin connector on its underside connects directly to the discrete input terminal board. The connector contains the 16 input signals, ID signal and Wetting voltage signal (From WDII when connected).
- An RJ-45 Ethernet connector named ENET1 on the side of the pack is the primary system interface.
- A second RJ-45 Ethernet connector named ENET2 on the side of the pack is the redundant or secondary system interface.
- A 3-pin power connector on the side of the pack is for 28 V dc power for the pack and terminal board.

6.1.3 Operation

The following features are common to the distributed I/O modules:

- *BPPx Processor*
- *Processor LEDs*
- *Power Management*
- *ID Line*
- *I/O Module Common Diagnostic Alarms*

The PDII has an internal application specific circuit board that contains the hardware needed for the contact input function. The application board connects between the processor and the contact input terminal board. The application board provides the following functions:

- Provide electronic identification of the application board to the processor and support pass-through of the terminal board identification
- Receive 16 contact input signals from the terminal board and pass them to the processor board
- Provide 16 bi-color indicator LEDs for contact state and health indication

6.1.4 Specifications

Item	PDII Specification
Number of Channels	16 contact voltage input channels
Voltage Range for Point Isolated Inputs	14 to 32 V dc, nominal 24 V dc; 19 to 64 V dc, nominal 48 V dc; 50 to 156 V dc, nominal 125 V dc; 100 to 264 V dc, nominal 250 V dc; 90 to 143 V ac rms, nominal 115 ac V rms, 50 Hz ±3 Hz; 90 to 264 V ac rms, nominal 230 ac V rms, 50 Hz ±3 Hz; If the wetting voltage goes out of the ranges listed above (Configured), an invalid voltage alarm occurs. Contact status is not reported if there is invalid voltage. The wetting voltage is monitored only when it is present at the TB points.
Accuracy for Voltage Monitoring for Invalid Voltage Alarm	±6%
Channel Mix	When the terminal board is used in point isolated configuration, there can be a mix of ranges. Every channel can have a different input voltage within any of the ranges mentioned above.
Frame Rate	System dependent scan rate for control purposes (10 ms, 20 ms, 40 ms, 80 ms, 160 ms, 320 ms) 1,000 Hz scan rate for sequence of events monitoring
Sequence of Event (SOE) (*if enabled in configuration*)	SOE accuracy for contacts with dc voltage — ±1 ms SOE accuracy for contacts with ac voltage — ±3 ms
Fault Detection	Loss of contact input excitation voltage (Loss of system wetting voltage only when WDII is connected) Incorrect terminal board
Single Resistor Fault Detection Option (*as described with terminal board*)	WDIIH1, WDIIH2, WDIIH3 — Fuse Blown/ open field wire
Dual Resistor Fault Detection (*as described with terminal board*)	WDIIH2, WIIH3 — Fuse Blown/ open field wire Line to line short in the field
Contact Status Indication	Bi-color LEDs Green – Contact status true Off – Contact status false or unused RED – Line fault or invalid voltage
Ambient Rating for Enclosure Design†	PDIIH1B is rated from -40 to 70°C (-40 to 158 °F) PDIIH1A is rated from -30 to 65°C (-22 to 149 °F)

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

6.1.5 Diagnostics

The I/O pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, optional board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set

The I/O pack performs the following diagnostic tests for contact excitation voltage and field line monitoring:

- Monitors that contact input excitation voltage is in the valid range
- Monitors Fuse Blown/open field wire. Adds a resistor parallel to the contact in the field and configures the channel accordingly.
- Monitors Fuse Blown/open field wire and Line-to-line short in the field. Adds a resistor parallel to the contact and adds one resistor in series with the contact in the field and configures the channel accordingly.

6.1.6 Configuration

Parameter	Description	Choices
BoardWettingV	Set the board level wetting voltage. This voltage is connected at JE1 or JE2 of WDII board. This configuration is applicable only for WDIIH1.	24 V dc, 115 V ac, 230 V ac
Inputs		
ContactInput	To enable contact input	Used, Unused
SignalInvert	Inversion makes signal true if contact is open	Normal, Invert
SeqOfEvents	Record contact transitions in sequence of events	Enable, Disable
WettingV	The point level wetting voltage	SDIIH1: dc 24 V, dc 48 V, dc 125 V, dc 250 V, ac 115 V, ac 230 V SDIIH1+WDIIH1: SystemWetted, dc 24 V, dc 48 V, dc 125 V, dc 250 V, ac 115 V, ac 230 V SDIIH1+WDIIH2: SystemWetted, dc 24 V, dc 48 V, dc 125 V, dc 250 V, ac 115 V, ac 230 V SDIIH1+WDIIH3: WDII H3 cannot have point isolated channels – No option selectable. All channels are only system wetted
SignalFilter	The debounce filter to filter out very rapid transitions *If SOE is enabled and a SignalFilter time is selected, then the SOE accuracy changes to the filter time selected.*	Unfiltered, 10 ms, 20 ms, 50 ms, 100 ms

6.1.6.1 Signal Space Inputs

There are three tabs in the ToolboxST application to indicate contact health. These tabs display the real time health of the contact for the Signal Space Input to the Mark VIe controller from the PDII I/O pack. The display of these tabs is dependent on the boards used. When standalone SDII is used, only the **Wetting Voltage Health** tab is displayed. With SDII + WDIIH1A, or with SDII + WDIIH2A, all three tabs are displayed. If SDII + WDIIH3A is used, **Wetting Voltage Health** and **Line Fault** tabs are displayed.

Wetting Voltage Health tab is used only if the contact is configured for isolated/external wetting. For contacts configured for System wetting, this input always displays True. For all unused contacts, this input always displays True. The variables names are V_Wetting#.

- V_Wetting# is *True* if the point level wetting voltage is within the tolerance limits for the configured wetting voltage or contact is configured Unused.
- V_Wetting# is *False* if the point level wetting voltage is not within the tolerance limits for the configured wetting voltage.

Line Faults tab contains:

- LineFault# is *True* if the any of the line fault occurs on the channel.
- LineFault# is *False* if no line fault is present on the channel or contact is configured *Unused* or line fault monitoring is configured for *None*.

Fuses tab contains the names of the variables, *Fuse#Fdbk*.

- Fuse#Fdbk is *True* if the fuse for the contact is intact or contact is configured Unused or line fault monitoring is configured for None.
- Fuse#Fdbk is *False* if the fuse for the contact is blown.

6.2 PDII Specific Alarms

The following alarms are specific to the PDII I/O pack.

34-49

Description Contact Input [ ] Invalid excitation voltage

Possible Cause This diagnostic occurs for contact inputs that are configured as *Isolated* inputs or if configured with a standalone SDII terminal board.

- Configured excitation voltage for the contact input does not match the applied excitation voltage.
- Applied excitation voltage for the contact is outside its valid range.
- The contact input is toggling too fast for the wetting voltage to be measured properly.

Solution

- Verify that the contact input configuration matches the external excitation voltage.
- Verify that the external excitation voltage power supply voltage is within the expected voltage range.
- Refer to the PDII help documentation.
- Check the affected contact input for noise and proper wiring connections.

50-65

Description Line to line short on contact [ ]

Possible Cause This alarm is only valid for SDII+WDIIH2 or SDII+WDIIH3.

- ToolboxST configuration does not match the actual hardware.
- Parameter, **LineMonitoring/FuseDiag** (SDII+WDIIH2) or **LineMonitoring** (SDII+WDIIH3), is set incorrectly.
- Series and/or the parallel resistor have an incorrect resistance.
- Shorted wire between the contact and the terminal board screws

Solution

- Verify that the actual hardware matches the ToolboxST configuration.
- Verify the value and location of the connected series and parallel resistors with respect to the contact.
- Verify that **LineMonitoring** configuration is set to **SeriesParResistor**.
- Check and correct the wiring to clear the line fault.
- Refer to the PDII help documentation.

66-81

Description Open field wire for contact [ ]

Possible Cause This alarm is specific to WDIIH3.

- Parallel resistor is not connected across the contact.
- Open wire between the contact and the SDII screw connections

Solution

- Verify the parallel resistor values and connection across the contact.
- Verify the wiring connections between the SDII and the contact.
- Refer to the PDII help documentation.

98

Description Invalid Board excitation voltage connected to the WDII board

Possible Cause

- For WDIIH1: The **BoardWettingV** parameter does not match the actual excitation voltage applied to the WDII board.
- For WDIIH1/2/3: The board level excitation voltage applied to the WDII board is out of range.

Solution

- For WDIIH1: Verify that the **BoardWettingV** parameter matches the actual excitation voltage applied to the WDII board.
- Verify that the excitation voltage applied to the WDII board is within range.
- Refer to the PDII help documentation.

99

Description GROUND FAULT

Possible Cause A ground fault has occurred in the WDPC.

Solution Replace the WDPC.

100-115

Description Line fault monitoring not possible for contact [ ]

Possible Cause This alarm is specific to WDIIH1.

- Board level excitation voltage is configured for 24 V dc, but the actual excitation voltage connected is ac instead of dc.

Solution

- Verify that the **BoardWettingV** parameter matches the actual excitation voltage applied to the WDII board.
- Apply 24 V dc to the excitation voltage connector on the WDIIH1 board.
- Refer to the PDII help documentation.

116-131

Description Either wire open or fuse blown for contact [ ]

Possible Cause This alarm is specific to WDIIH1 and WDIIH2.

- Parallel resistor is not connected across the contact.
- Open wire between the contact and the SDII screw connections.
- Fuse of the associated contact input is blown.
- Isolated contact input (fuse pulled so that system excitation voltage is not applied) has been configured as **SystemWetted**.

Solution

- Verify the parallel resistor values and connection across the contact.
- Verify the wiring connections between the SDII and the contact.
- Replace the blown fuse. Refer to help documentation for the correct part number.
- Verify that the isolated contact input has the parameter **WettingV** configured to the proper external excitation voltage value (24 V dc, 48 V dc, 125 V dc, 250 V dc, 115 V ac, 230 V ac).
- Refer to the PDII help documentation.

6.3 SDII Simplex Contact Input with Point Isolation

The Contact Input with Point Isolation (SDII) terminal board provides 16 point isolated voltage detection circuits to sense a range of voltages across relay contacts, fuses, and switches and other contacts. IS200SDIIH1 has pluggable Euro style box-type terminal blocks and a connector that accepts different option boards. Three terminals are provided for each contact input channel. Each channel can accept different voltage levels as follows: 24 V dc/ 48 V dc/ 125 V dc/ 250 V dc/ 115 V ac rms / 230 V ac rms. If PDII is used with SDII only, then all 16 channels are point-isolated channels.

Note SDII has the same physical size, customer terminal locations, and I/O pack mounting as other S-type terminal boards.

There are three groups of WDII option boards that connect to SDII. If the option board WDII is connected, the point isolated channels become group isolated channels where the system wetting voltage is provided through WDII. WDII boards have an isolated voltage detector circuit similar to SDII to monitor the wetting voltage.

Using option board WDIIH1, all 16 channels can be system wetted with 24 V dc, 115 V ac rms, or 230 V ac rms. When using WDIIH1 each of the 16 channels can be individually set and configured as point isolated and each channel can accept a different voltage level as needed. A mix of point isolation and group isolation is possible in this configuration.

Using option board WDIIH2, all 16 channels can be system wetted with 48 V dc. When using WDIIH2, each of the 16 channels can be individually set and configured as point isolated and each channel can accept a different voltage level as needed. A mix of point isolation and group isolation is possible in this configuration.

Using option board WDIIH3, all 16 channels can only be system wetted with 125 V dc. With WDIIH3, there is no option provided to configure channels as point isolated.

6.3.1 Specifications

Item	SDII Specification
Number of Channels	16 contact voltage input channels
Input Isolation in Pack	Optical isolation to 1500 V on all inputs from inputs to system and channel to channel
Voltage Range for Point Isolated Inputs	nominal 14 to 32 V dc, 24 V dc; nominal 19 to 64 V dc, 48 V dc; nominal 50 to 156 V dc, 125 V dc; nominal 100 to 264 V dc, 250 V dc; nominal 90 to 143 V ac rms, 115 ac V rms, 50/60 Hz ±3 Hz; nominal 90 to 264 V ac rms, 230 ac V rms, 50/60 Hz ±3 Hz. If the wetting voltage goes out of the above ranges (Configured), then in that case an alarm is raised as invalid voltage. In case of invalid voltage, contact status is not reported. The wetting voltage is monitored only when it is present at the TB points
Accuracy for Voltage Monitoring for Invalid Voltage Alarm	±6%
Channel Mix	When the SDII is used in point isolated configuration, there can be a mix of ranges. That means every channel can have one of the ranges mentioned above.
Frame Rate	System dependent scan rate for control purposes 1,000 Hz scan rate for sequence of events (SOE) monitoring
Sequence of Event (SOE) (*if enabled in configuration*)	SOE accuracy for contacts with DC voltage ±1 ms SOE accuracy for contacts with AC voltage ±3 ms
System Wetting with WDII Connected	WDIIH1 – 24 V dc, 115 V ac rms 50/60 Hz, 230 V ac rms 50/60 Hz WDIIH2 – 48 V dc WDIIH3 – 125 V dc

Item	SDII Specification
Voltage Range for System Wetted Inputs-None and Parallel Resistor Configuration	Nominal 18.5 to 32 V dc, 24 V dc; (WDIIH1) Nominal 32 to 64 V dc, 48 V dc; (WDIIH2) Nominal 70 to 145 V dc, 125 V dc; (WDIIH3) Nominal 90 to 143 V rms ac, 115 V rms ac, 50/60 Hz ±3 Hz; (WDIIH1) Nominal 180 to 264 V rms ac, 230 V rms ac, 50/60 Hz ±3 Hz. (WDIIH1) 250 V dc range is not supported in this configuration as no WDII board can support 250 V dc range for system wetting. Accuracy for voltage monitoring for Invalid voltage alarm: ±6%
Voltage Range for System Wetted Inputs-Series Parallel Resistor Configuration	42 to 56 V dc, nominal 48 V dc; (WDIIH2) 90 to 145 V dc, nominal 125 V dc; (WDIIH3) 24 V dc, 250 V dc, 115 V ac and 230 V ac ranges are not supported in this configuration. Accuracy for voltage monitoring for Invalid voltage alarm: ±6%
Mix of Point Isolated and System Wetted Channels	Possible with WDIIH1 and WDIIH2
Fault Detection	Loss of contact input excitation voltage (Loss of system wetting voltage only when WDII is connected) Incorrect terminal board
Single Resistor Fault Detection Option-Parallel Resistor Configuration	WDIIH1, WDIIH2, WDIIH3 — Fuse Blown/ open field wire
Dual Resistor Fault Detection Series Parallel Resistor Configuration	WDIIH2, WDIIH3 — Fuse Blown/ open field wire Line to line short in the field
Fuse used in WDIIH1 and WDIIH2 for Each Channel	WDIIH1 and WDIIH2 have removable fuses one per channel in the supply line as per the following description. In case of replacement the exact part shall be used. Littelfuse –372 series, 200 mA, 250 V radial fuse (Part number 3720200051 or 37202000511) GE part number – 342A4908AFP1
Fuse used in WDIIH3	WDIIH3 has non-removable thermal fuse (PTC) in the supply line
Size	15.9 cm high x 17.8 cm wide (6.25 in x 7.0 in)
Technology	Surface-mount
Vibration Protection	SDIIH1A provides standard I/O pack vibration protection rating, and should be used for most applications SDIIH2A is enhanced to provide more vibration protection for use in some GE Drilling applications. The purchase price is higher for this version, which includes RTV and stabilizer bar.

6.3.2 Installation

Note E1 and E2 are chassis grounding screws for SCOM.

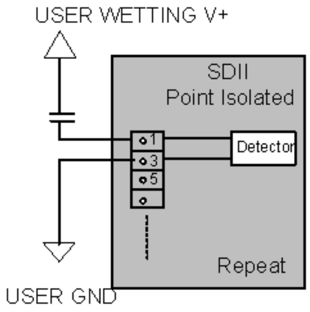
The SDII and plastic insulator are attached to a sheet metal carrier that mounts on to the cabinet using screws. An option board if used, plugs onto SDII and is held in place with the help of four stand-offs and the fastener hardware. The contact inputs are wired directly to the terminal block, typically using #18 AWG wires. Shields should be terminated on a separate bracket.

6.3.2.1 Terminal Board Wiring

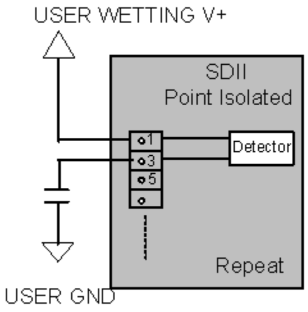
Connect the wires for the 16 isolated digital inputs directly to 48 pin pluggable Euro style box-type terminal blocks on the terminal board, with each terminal accepting up to #18 AWG wires. Each block has three screws per every one channel of contact input and each block can be unplugged from the board for maintenance. A shield terminal strip attached to chassis ground is located immediately to the left of each terminal block.

The connections are configured as follows:

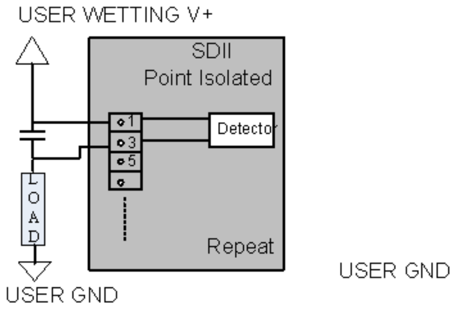
Series connection SDII-A



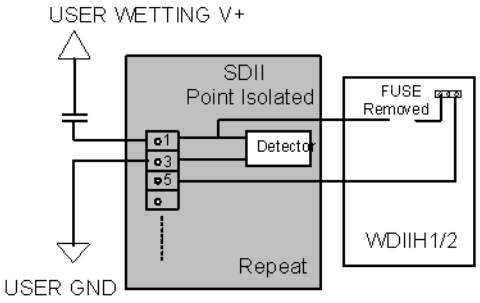
Series connection SDII- B



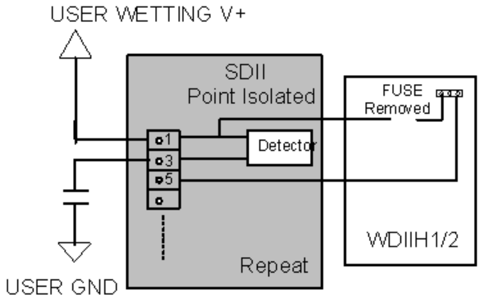
Parallel connection SDII- C



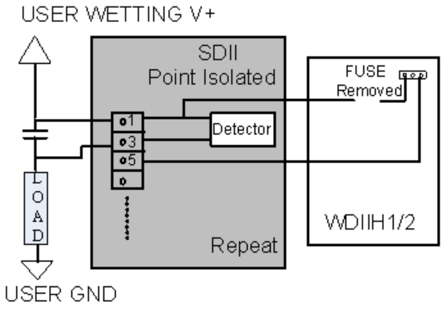
Series connection SDII-AA



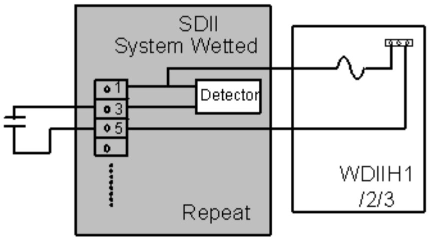
Series connection SDII- BB



Parallel connection SDII- CC



Series connection SDII- DD



Parallel connection - When the contact is off there will be leakage of 2 to 7 mA based on the amplitude of wetting voltage due to the parallel detector circuit. So for the loads which are sensitive to the current of 7 mA this configuration shall not be used. For example, if the load is a LED type indicator it will glow due to the leakage of detector circuit even if the contact is off. For such loads, this configuration should not be used.

6.3.2.2 Screw Definitions

SDII Field Terminal Definitions

SDII TB definitions		Point Isolated — Only SDII			Point Isolated — SDII+WDIIH1/2			System Wetted
		Series contact	Series contact	Parallel Contact	Series contact	Series contact	Parallel Contact	WDII-H1/2/3
Channel	**TB screws**	**SDII–A**	**SDII–B**	**SDII–C**	**SDII–AA**	**SDII–BB**	**SDII–CC**	**SDII–DD**
1	**1**	Contact connection 2	User V+ve	Contact connection 1	Contact connection 2	User V+ve	Contact connection 1	NC
	3	User GND	Contact connection 1	Contact connection 2	User GND	Contact connection 1	Contact connection 2	Contact connection 1
	5	NC	NC	NC	NC	NC	NC	Contact connection 2
2	**2**	Contact connection 2	User V+ve	Contact connection 1	Contact connection 2	User V+ve	Contact connection 1	NC
	4	User GND	Contact connection 1	Contact connection 2	User GND	Contact connection 1	Contact connection 2	Contact connection 1
	6	NC	NC	NC	NC	NC	NC	Contact connection 2
3	**7**	Contact connection 2	User V+ve	Contact connection 1	Contact connection 2	User V+ve	Contact connection 1	NC
	9	User GND	Contact connection 1	Contact connection 2	User GND	Contact connection 1	Contact connection 2	Contact connection 1
	11	NC	NC	NC	NC	NC	NC	Contact connection 2
4	**8**	Contact connection 2	User V+ve	Contact connection 1	Contact connection 2	User V+ve	Contact connection 1	NC
	10	User GND	Contact connection 1	Contact connection 2	User GND	Contact connection 1	Contact connection 2	Contact connection 1
	12	NC	NC	NC	NC	NC	NC	Contact connection 2
5	**13**	Contact connection 2	User V+ve	Contact connection 1	Contact connection 2	User V+ve	Contact connection 1	NC
	15	User GND	Contact connection 1	Contact connection 2	User GND	Contact connection 1	Contact connection 2	Contact connection 1
	17	NC	NC	NC	NC	NC	NC	Contact connection 2
6	**14**	Contact connection 2	User V+ve	Contact connection 1	Contact connection 2	User V+ve	Contact connection 1	NC
	16	User GND	Contact connection 1	Contact connection 2	User GND	Contact connection 1	Contact connection 2	Contact connection 1
	18	NC	NC	NC	NC	NC	NC	Contact connection 2

SDII Field Terminal Definitions (continued)

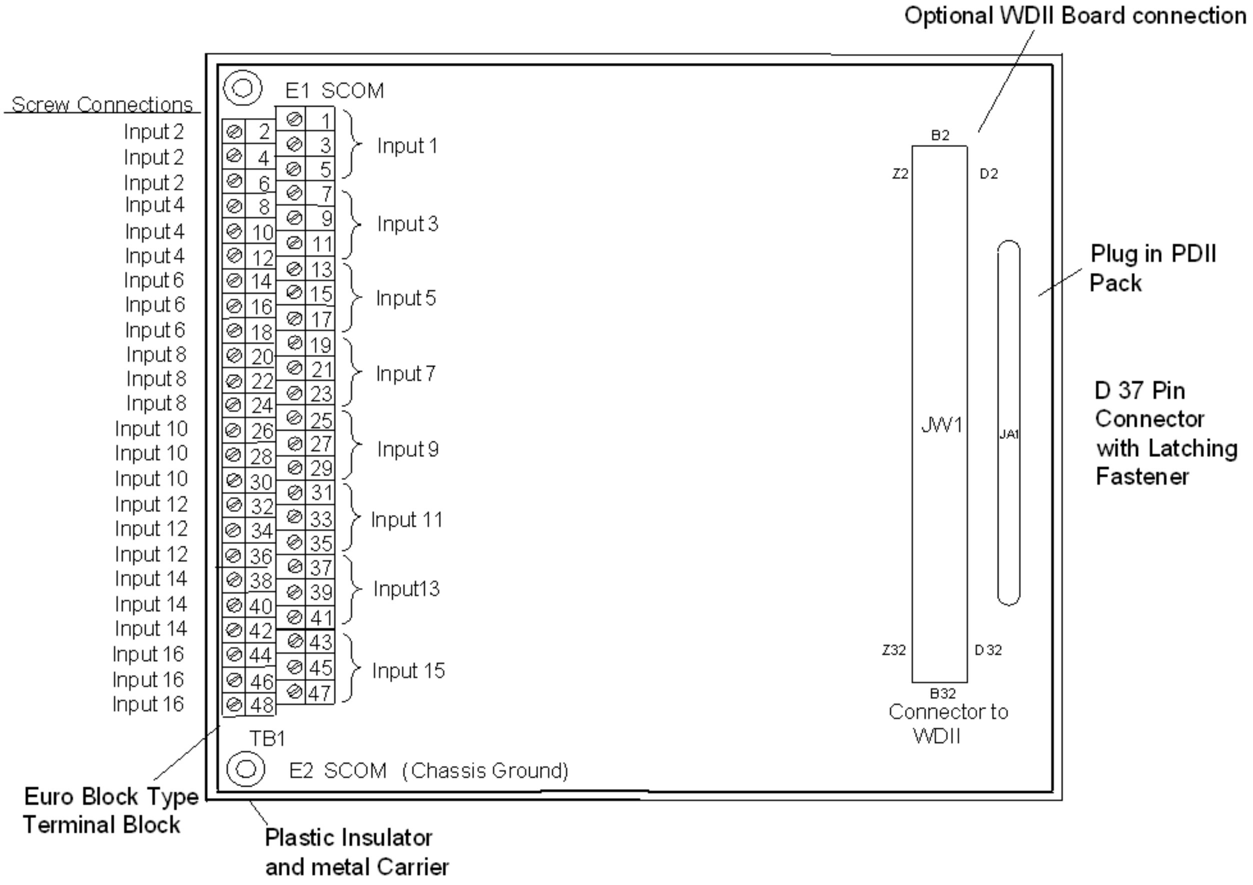
SDII TB definitions		Point Isolated — Only SDII			Point Isolated — SDII+WDIIH1/2			System Wetted
		Series contact	Series contact	Parallel Contact	Series contact	Series contact	Parallel Contact	WDII-H1/2/3
Channel	**TB screws**	**SDII–A**	**SDII–B**	**SDII–C**	**SDII–AA**	**SDII–BB**	**SDII–CC**	**SDII–DD**
7	**19**	Contact connection 2	User V+ve	Contact connection 1	Contact connection 2	User V+ve	Contact connection 1	NC
	21	User GND	Contact connection 1	Contact connection 2	User GND	Contact connection 1	Contact connection 2	Contact connection 1
	23	NC	NC	NC	NC	NC	NC	Contact connection 2
8	**20**	Contact connection 2	User V+ve	Contact connection 1	Contact connection 2	User V+ve	Contact connection 1	NC
	22	User GND	Contact connection 1	Contact connection 2	User GND	Contact connection 1	Contact connection 2	Contact connection 1
	24	NC	NC	NC	NC	NC	NC	Contact connection 2
9	**25**	Contact connection 2	User V+ve	Contact connection 1	Contact connection 2	User V+ve	Contact connection 1	NC
	27	User GND	Contact connection 1	Contact connection 2	User GND	Contact connection 1	Contact connection 2	Contact connection 1
	29	NC	NC	NC	NC	NC	NC	Contact connection 2
10	**26**	Contact connection 2	User V+ve	Contact connection 1	Contact connection 2	User V+ve	Contact connection 1	NC
	28	User GND	Contact connection 1	Contact connection 2	User GND	Contact connection 1	Contact connection 2	Contact connection 1
	30	NC	NC	NC	NC	NC	NC	Contact connection 2
11	**31**	Contact connection 2	User V+ve	Contact connection 1	Contact connection 2	User V+ve	Contact connection 1	NC
	33	User GND	Contact connection 1	Contact connection 2	User GND	Contact connection 1	Contact connection 2	Contact connection 1
	35	NC	NC	NC	NC	NC	NC	Contact connection 2
12	**32**	Contact connection 2	User V+ve	Contact connection 1	Contact connection 2	User V+ve	Contact connection 1	NC
	34	User GND	Contact connection 1	Contact connection 2	User GND	Contact connection 1	Contact connection 2	Contact connection 1
	36	NC	NC	NC	NC	NC	NC	Contact connection 2
13	**37**	Contact connection 2	User V+ve	Contact connection 1	Contact connection 2	User V+ve	Contact connection 1	NC
	39	User GND	Contact connection 1	Contact connection 2	User GND	Contact connection 1	Contact connection 2	Contact connection 1
	41	NC	NC	NC	NC	NC	NC	Contact connection 2

SDII Field Terminal Definitions (continued)

SDII TB definitions		Point Isolated — Only SDII			Point Isolated — SDII+WDIIH1/2			System Wetted
		Series contact	Series contact	Parallel Contact	Series contact	Series contact	Parallel Contact	WDII-H1/2/3
Channel	TB screws	SDII–A	SDII–B	SDII–C	SDII–AA	SDII–BB	SDII–CC	SDII–DD
14	**38**	Contact connection 2	User V+ve	Contact connection 1	Contact connection 2	User V+ve	Contact connection 1	NC
	40	User GND	Contact connection 1	Contact connection 2	User GND	Contact connection 1	Contact connection 2	Contact connection 1
	42	NC	NC	NC	NC	NC	NC	Contact connection 2
15	**43**	Contact connection 2	User V+ve	Contact connection 1	Contact connection 2	User V+ve	Contact connection 1	NC
	45	User GND	Contact connection 1	Contact connection 2	User GND	Contact connection 1	Contact connection 2	Contact connection 1
	47	NC	NC	NC	NC	NC	NC	Contact connection 2
16	**44**	Contact connection 2	User V+ve	Contact connection 1	Contact connection 2	User V+ve	Contact connection 1	NC
	46	User GND	Contact connection 1	Contact connection 2	User GND	Contact connection 1	Contact connection 2	Contact connection 1
	48	NC	NC	NC	NC	NC	NC	Contact connection 2

6.3.2.3 Cabling Connections

The PDII I/O pack is plugged into the SDII terminal board and attached to the side mounting brackets. One or two Ethernet cables plug into the pack. Firmware may need to be downloaded.



6.3.2.4 Euro Style Box-Type Terminal Blocks

The PDII module features 48 pluggable Euro style box-type terminal blocks. The terminal blocks on SDII accept conductors with the following characteristics:

Conductor Type	Minimum	Maximum
Conductor cross section solid	0.2 mm²	2.5 mm²
Conductor cross section stranded	0.2 mm²	2.5 mm²
Conductor cross section stranded, with ferrule without plastic sleeve	0.25 mm²	2.5 mm²
Conductor cross section stranded, with ferrule with plastic sleeve	0.25 mm²	2.5 mm²
Conductor cross section AWG/kcmil	24 AWG	12 AWG
Two conductors with same cross section, solid	0.2 mm²	1 mm²
Two conductors with same cross section, stranded	0.2 mm²	1.5 mm²
Two conductors with same cross section, stranded, without plastic sleeve	0.25 mm²	1 mm²
Two conductors with same cross section, stranded, TWIN ferrules with plastic sleeve	0.5 mm²	1.5 mm²

6.3.2.5 Fuses on WDII

Note Use the exact part as specified when replacement is needed

WDIIH1 and WDIIH2 have one removable fuse per channel in the supply line as per the following description:

Littelfuse® – 372 series, 200 mA, 250 V radial fuse (Part number 3720200051 or 37202000511)

GE part number for fuse –342A4908AFP1

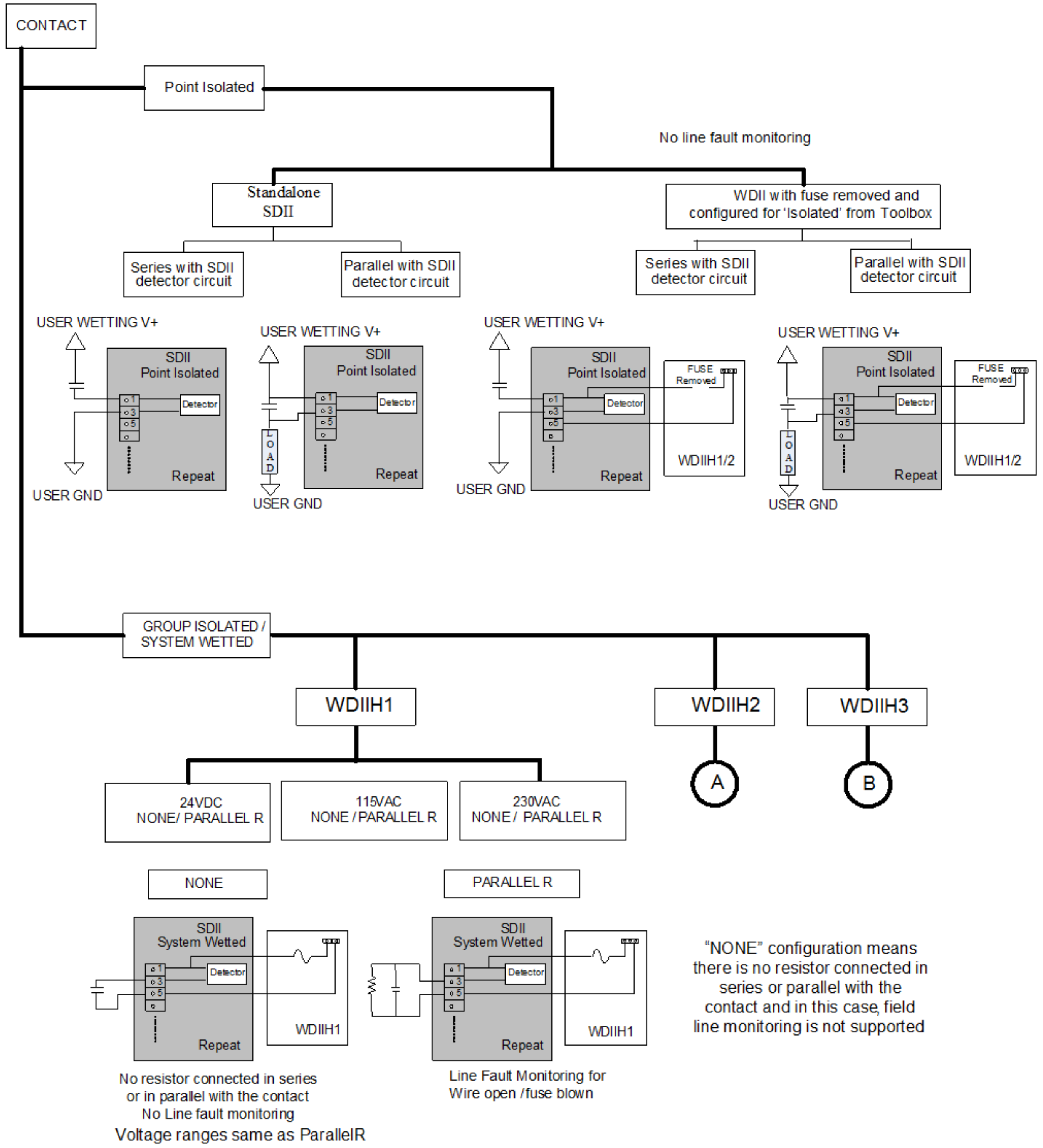
WDIIH3 has non-removable thermal fuse (PTC) in the supply line. The fuse numbers are in the following table:

Channel	SDII-TB Screws	WDIIH1 Fuses-Removable	WDIIH2 Fuses-Removable	WDIIH3 Thermal fuses (PTC)- Not-Removable
1	1 3 5	FU1	FU1	TR1
2	2 4 6	FU2	FU2	TR2
3	7 9 11	FU3	FU3	TR3
4	8 10 12	FU4	FU4	TR4
5	13 15 17	FU5	FU5	TR5
6	14 16 18	FU6	FU6	TR6
7	19 21 23	FU7	FU7	TR7
8	20 22 24	FU8	FU8	TR8
9	25 27 29	FU9	FU9	TR9
10	26 28 30	FU10	FU10	TR10
11	31 33 35	FU11	FU11	TR11
12	32 34 36	FU12	FU12	TR12
13	37 39 41	FU13	FU13	TR13

Channel	SDII-TB Screws	WDIIH1 Fuses-Removable	WDIIH2 Fuses-Removable	WDIIH3 Thermal fuses (PTC)- Not-Removable
14	38 40 42	FU14	FU14	TR14
15	43 45 47	FU15	FU15	TR15
16	44 46 48	FU16	FU16	TR16

6.3.2.6 Configuration Options

Note In the following drawings, the word *repeat* means the same blocks are repeated for all 16 channels with different screw numbers.

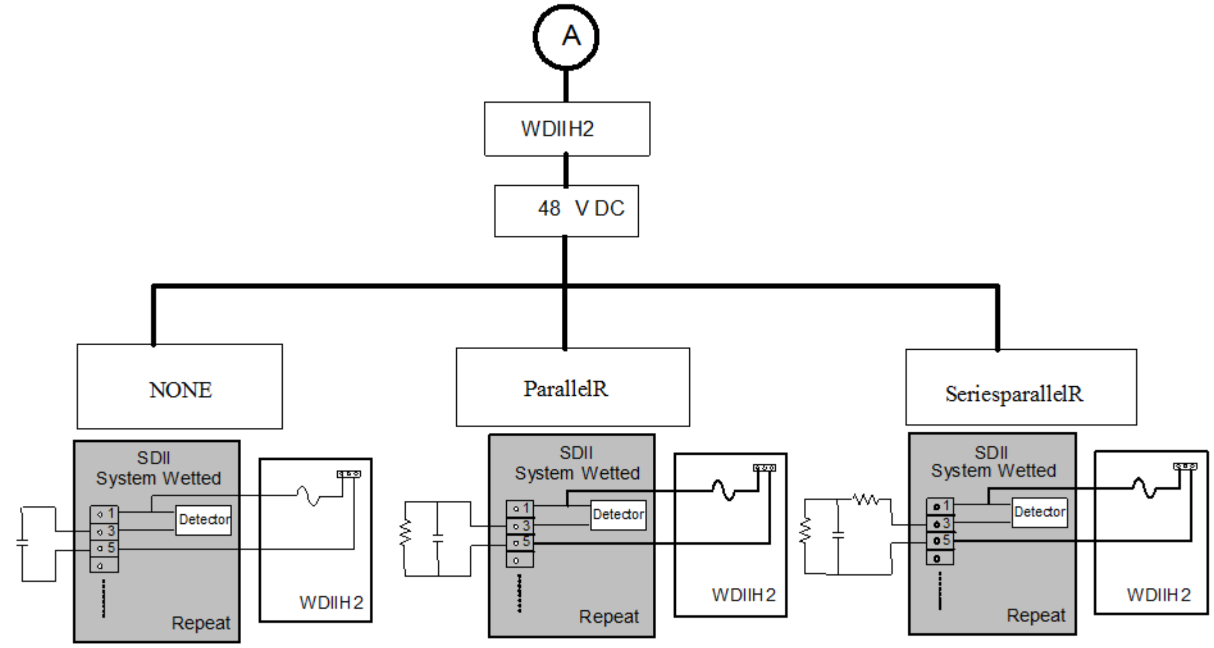


No resistor connected in series
or in parallel with the contact
No Line fault monitoring
Voltage ranges same as ParallelR

Line Fault Monitoring for
Wire open /fuse blown

"NONE" configuration means there is no resistor connected in series or parallel with the contact and in this case, field line monitoring is not supported

Configuration Options Using SDII/ SDII+WDII

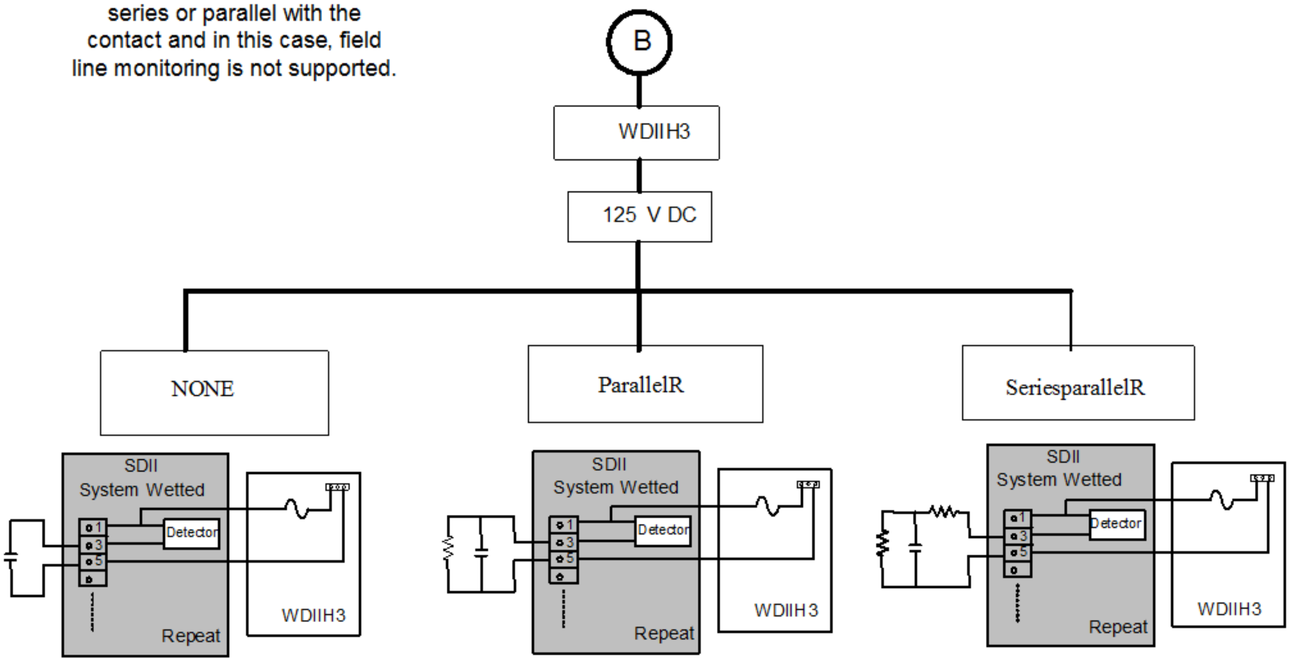


No resistor connected in series
or in parallel with the contact
No Line fault monitoring

Line Fault Monitoring for
Wire Open/Fuse blown

Line Fault Monitoring for
1.Wire open/ Fuse blown
2.Wire shorted

“NONE” configuration means there is no resistor connected in series or parallel with the contact and in this case, field line monitoring is not supported.



No resistor connected in series
or in parallel with the contact
No Line fault monitoring

Line Fault Monitoring for
Wire Open/Fuse blown

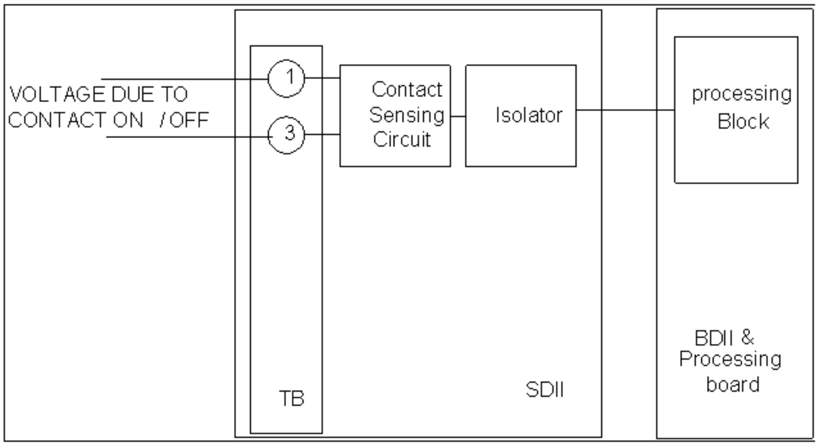
Line Fault Monitoring for
1.Wire open/ Fuse blown
2.Wire shorted

6.3.3 Operation

6.3.3.1 Point Isolated Input Signals

The SDII provides a sensing circuit, which converts the voltage present at the TB input to an isolated digital signal. Using the isolated signal, the firmware calculates the voltage present at the TB input. Based on the presence and absence of voltage at the TB input, it declares the status of contact as on or off.

Each input is isolated from each other. If SDII is used without an optional board, all the inputs are point isolated as well as system isolated.

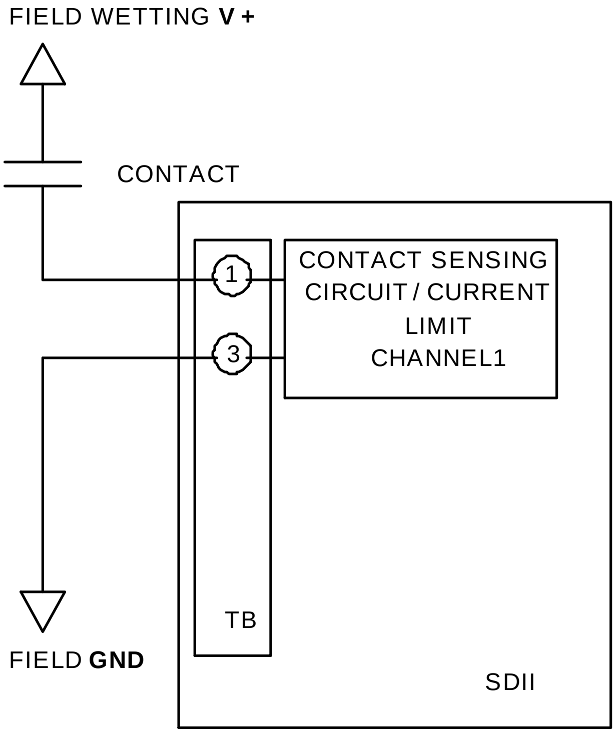


If SDII is used with optional board WDIIH1, channels can be system wetted with 24 V dc / 115 V 50/60 Hz ac rms / 230 V 50/60 Hz ac rms based on the TB points used for field wire terminations and the channel configuration setting through the ToolboxST application. The frequency range for AC 50 Hz and 60 Hz is ±3 Hz. System wetting requires that the respective channel fuse be present on WDII. Removal of the fuse allows use of the input as a point isolated signal path.

If SDII is used with optional board WDIIH2, all or some channels can be system wetted with 48 V dc based on the TB points used for field wire terminations and the channel configuration setting through toolbox.

If SDII is used with optional board WDIIH3, all channels are system wetted with 125 V dc.

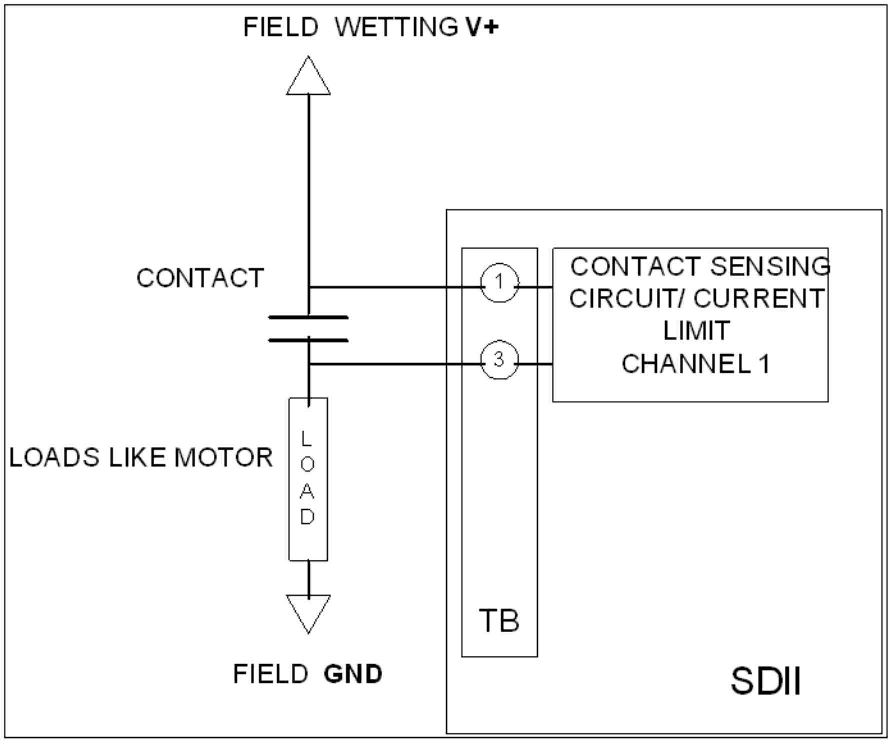
6.3.3.2 Point Isolated Contact Input Channels



Contact in series with detector circuit, current limiting circuit

In the figure above, the contact is connected in series with the detector circuit. An external current limit circuit is not necessary. The detector circuit offers current limit of 2 mA - 7 mA based on the input wetting voltage provided by the user.

When voltage is present at TB input, the contact input setting for the contact is on. When the contact is on, the system interprets it as true as there is voltage present at TB input when contact is on.



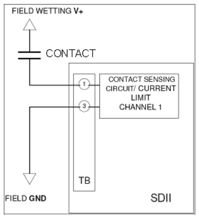
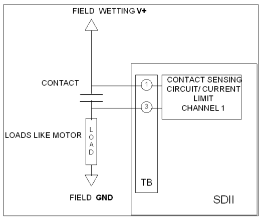
Contact in parallel with detector circuit

In the figure above, the contact is connected in parallel with the detector circuit. This can be used for sensing contacts in series with loads like an electric motor. An external current limit circuit is required as the SDII does not provide any current limit for the current flowing through contact. The user provides the wetting voltage. This configuration avoids the need of auxiliary sensing contacts for electric motor-like loads provided the motor voltage is within the SDII voltage sensing limit of 264 V dc or 265 V ac rms.

When the contact is off there will be leakage of 2 to 7 mA based on the amplitude of wetting voltage due to the parallel detector circuit. So for the loads which are sensitive to the current of 7 mA this configuration shall not be used. For example, if the load is a LED type indicator it will glow due to the leakage of detector circuit even if the contact is off. For such loads, this configuration should not be used.

When voltage is present at TB input, the contact input setting for the contact is on. When the contact is on, there is no voltage at TB input and the system interprets it as false. If the user configures the contact as an invert, when the contact is on the system interprets it as true.

In both the configurations, the contact must be connected in the first two pins provided for each contact. For channel 1 it is screw 1 and screw 3. A comparison of these configurations is given in the following table.

<table>
<tr><th></th><th>Connections</th><th>Diagram</th><th>Configuration For Signal Invert</th><th>System reporting when contact closed</th><th>System reporting when contact open</th></tr>
<tr><td>1</td><td>Contact in series with detector circuit</td><td rowspan="2">
</td><td>(Default) Normal</td><td>True</td><td>False</td></tr>
<tr><td></td><td>Contact in series with detector circuit</td><td>Invert</td><td>False</td><td>True</td></tr>
<tr><td>2</td><td>Contact in parallel with detector circuit</td><td rowspan="2">
</td><td>(Default) Normal</td><td>False</td><td>True</td></tr>
<tr><td></td><td>Contact in parallel with detector circuit</td><td>Invert</td><td>True</td><td>False</td></tr>
</table>

6.3.3.3 Voltage Ranges for Point Isolated Channels

Voltage ranges:

14 to 32 V dc, nominal 24 V dc

19 to 64 V dc, nominal 48 V dc

50 to 156 V dc, nominal 125 V dc

100 to 264 V dc, nominal 250 V dc

90 to 143 V ac rms, nominal 115 ac V rms, 47-63 Hz

90 to 264 V ac rms, nominal 230 ac V rms, 47-63 Hz

When the SDII is used in point isolated configuration, there can be a mix of ranges. That means every channel can have one of different input voltage within any of the ranges mentioned above.

For example, channel 1 can have a contact with a user wetting voltage of 24 V dc, channel 2 can have 115 V 60 Hz ac rms, and channel 3 contact can be wetted to 48 V dc by the user.

If the wetting voltage goes out of the specified ranges listed above (for each configured voltage), an invalid voltage alarm occurs and the status LED indicator turns RED. Contact status is not reported if there is invalid voltage. The wetting voltage is monitored only when it is present at the TB points and only for the following conditions:

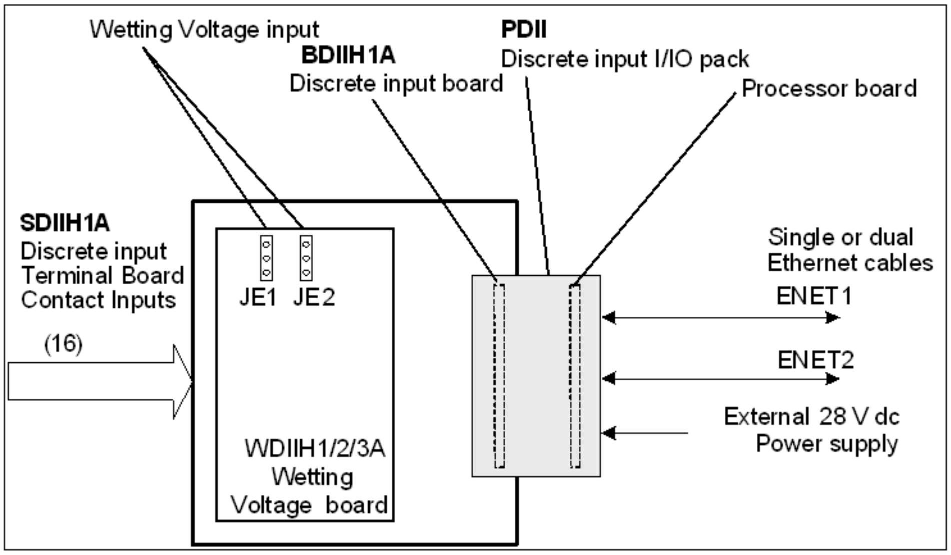
- The contact is on for a series contact
- The contact is off for a parallel contact

Note Accuracy for voltage monitoring for the invalid voltage alarm is ±6%

When the voltage is above or below these levels, an invalid wetting voltage alarm is raised. On lower side, the alarm will be generated below the range. If the wetting voltage goes below 10 V the alarm will be cleared and contact state reported will be False healthy in default configuration. For invert configuration, it will be True healthy.

6.3.3.4 System Wetted (Group Isolated) Input Signals

The contact input channels can be provided with wetting voltage through a WDII option board. Along with the system wetting, WDIIH boards offer field line fault monitoring with addition of one or two resistors connected in the field near the contact. WDII boards have an isolated voltage detector circuit similar to SDII to monitor the wetting voltage.

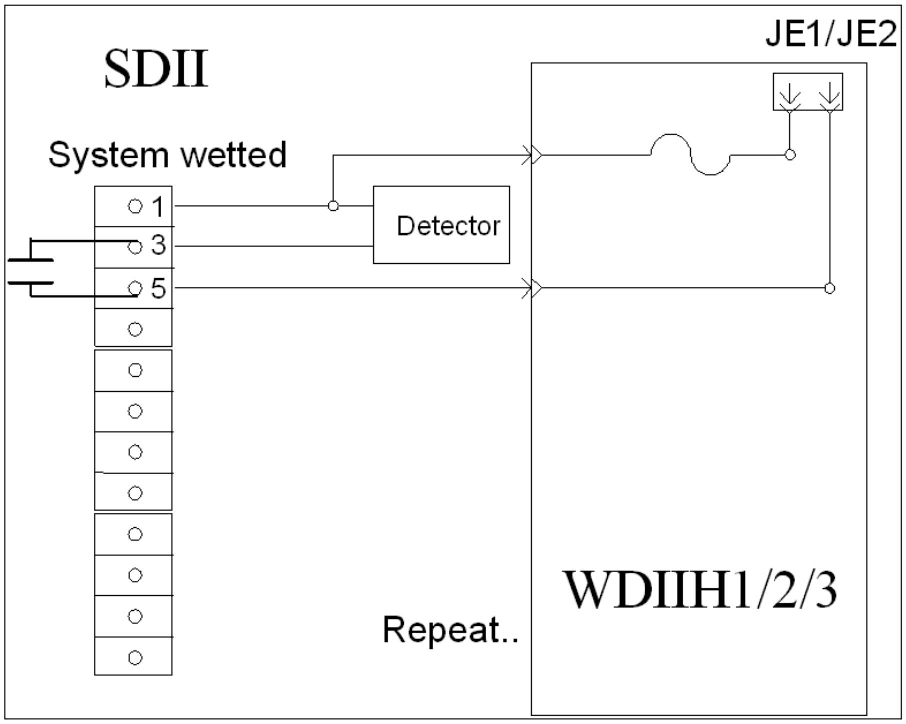


WDIIH1A is capable of providing 115 V/ 240 V ac rms, 50/60 Hz and 24 V dc wetting voltage with individual fuses in each supply line. The wetting voltage is connected through JE1 or JE2 parallel connectors. Pin 1 of JE1 should be connected to positive and pin 3 should be connected to negative. PDII can be configured to detect open field wiring or an open fuse on WDII with the addition of one resistor in parallel with the contact being sensed. Reversal of polarity at JE1/ JE2 is not desired.

WDIIH2A is capable of providing 48 V dc wetting voltage with fuse in supply line. The wetting voltage is connected through JE1 or JE2 parallel connectors. Pin 1 of JE1 should be connected to positive and pin 3 should be connected to negative. Reversal of polarity at JE1/ JE2 is not desired. PDII can be configured to detect open field wiring or an open fuse on WDII with the addition of one resistor in parallel with the contact being sensed. PDII can be configured to detect open fuse/field wiring and line-to-line short with the addition of one resistor in parallel and one resistor in series with the contact being sensed.

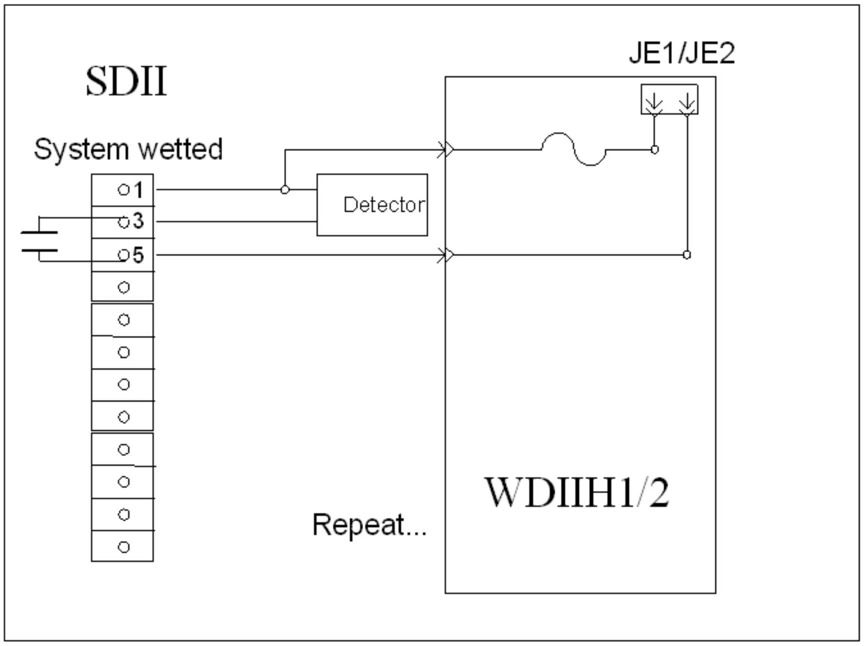
WDIIH3A is capable of providing 125 V dc contact wetting voltage with thermal fuse (PTC) in supply line. The wetting voltage is connected through JE1 or JE2 parallel connectors. Pin 1 of JE1 should be connected to positive and pin 3 should be connected to negative. Reversal of polarity at JE1/ JE2 is not desired. PDII can be configured to detect open field wiring or an open fuse on WDII with the addition of one resistor in parallel with the contact being sensed. PDII can be configured to detect open fuse/field wiring and line-to-line short with the addition of one resistor in parallel and one resistor in series with the contact being sensed.

For system wetted input signals, the contact must be connected in last two screws provided for each contact. For channel 1 it is screw 3 and screw 5. The SDII-WDII and the contact connection in case of system wetted contact inputs is displayed in the following figure.



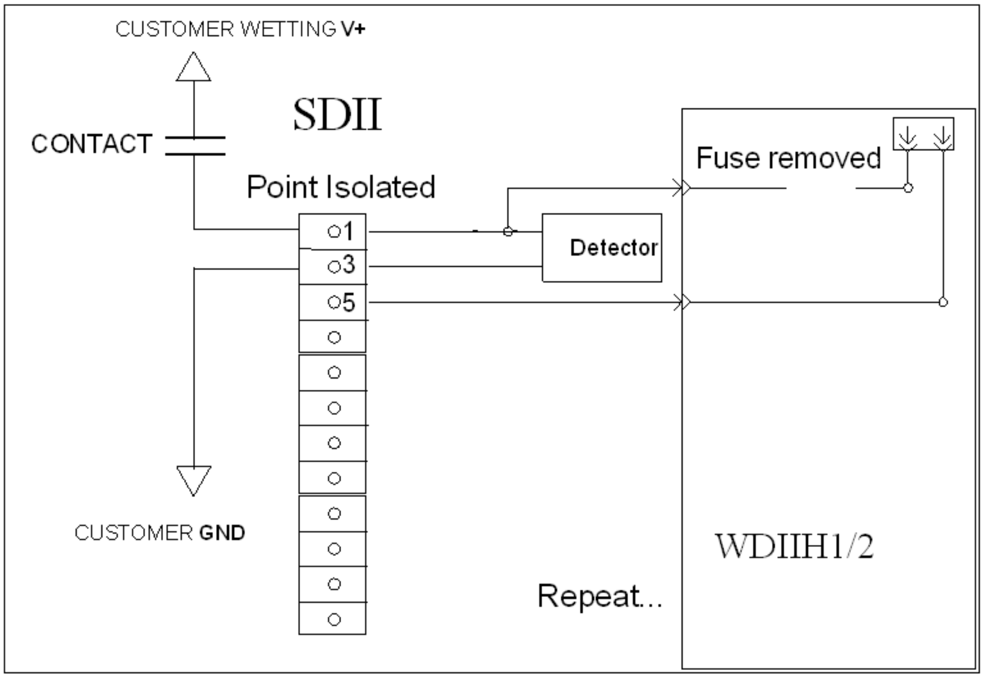
6.3.3.5 System Wetted and Point Isolated Mixed -Input Signals

When WDIIH1 or WDIIH2 featuring removable fuses are used, there can be a mix of system wetted contact inputs and point isolated contact inputs. Each contact is provided with three user terminals. For system-wetted channels, contact must be wired between last two user terminal points for that circuit. For channel 1 they are screw 3 and screw 5. In this case the detector circuit is in series with the contact and acts as the current limit. The contact can be connected as displayed in the following figure.

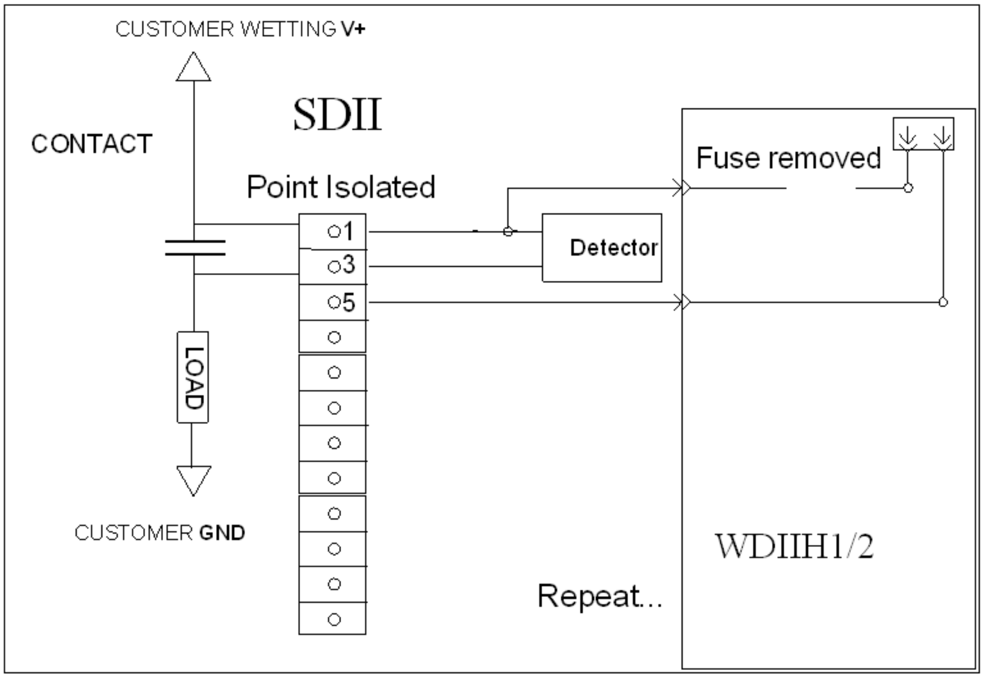


6.3.3.6 Point Isolated Channels when WDII is Used

To use any input as a point isolated input the fuse must be removed and the signal wired to the first two input terminals for that signal. For example, channel 1 uses screw 1 and screw 3. The pack must be configured to accept the input as a point isolated signal. Two ways to connect the contact are point isolated series and point isolated parallel.



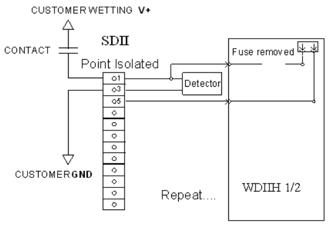
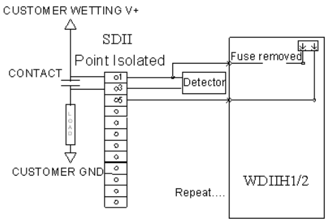
Point isolated series



Point Isolated Parallel

When the contact is off there will be leakage of 2 to 7 mA based on the amplitude of wetting voltage due to the parallel detector circuit. So for the loads which are sensitive to the current of 7 mA this configuration shall not be used. For example, if the load is a LED type indicator it will glow due to the leakage of detector circuit even if the contact is off. For such loads, this configuration should not be used.

While connecting and configuring point-isolated contacts using WDII the same care must be taken as the standalone SDII. A comparison for these configurations is given in the following table.

	Connections	Diagram	Configuration For Signal Invert	System Reporting when Contact Closed	System Reporting when Contact Open
1	**Contact in series with detector circuit**	 CUSTOMER WETTING V+ CONTACT SDII Point Isolated o1 o3 o5 Detector Fuse removed CUSTOMER GND Repeat.... WDIIH 1/2	**(Default) Normal**	**True**	**False**
	Contact in series with detector circuit		**Invert**	**False**	**True**
2	**Contact in parallel with detector circuit**	 CUSTOMER WETTING V+ SDII Point Isolated CONTACT o1 o3 o5 Detector Fuse removed LOAD CUSTOMER GND Repeat.... WDIIH1/2	**(Default) Normal**	**False**	**True**
	Contact in parallel with detector circuit		**Invert**	**True**	**False**

When WDIIH1 or H2 is used some channels can be configured as system wetted by keeping fuse intact and using last two TB points. The remaining channels can be point isolated by removing the fuse and using first two TB points.

WDIIH3 can be configured as system wetted (Board level) as it deploys thermal fuses (PTCs), which are not removable. WDIIH3 cannot support the point isolated and mixed configurations.

6.3.3.7 Field Line Fault Monitoring

Field line fault monitoring depends on knowledge of the contact wetting voltage provided by the sensing circuit on WDII. When SDIIH1 is used without a WDII, field line fault monitoring is not provided.

Note Connecting resistors other than the specified value may lead to incorrect detection of contact position or line fault.

When WDIIH1 is used with SDII there are two configurations possible.

None – No resistor is connected in series or in parallel with the contact; no field line monitoring. Only Contact on/off detection

Parallel Resistor – User has to add a resistor parallel to the contact in the field. When parallel resistor is used with Contact on/off and fuse blown/ the open field wire can be detected.

The specifications of parallel resistor for WDIIH1, 24 V dc — 3.01 kΩ, 1%, 0. 5 W. Orderable GE part number 336A4940HR-100

The specifications of parallel resistor for WDIIH1, 115 V ac — 22.1 kΩ, 1%, 3 W. Orderable GE part number 336A4940HW-100

The specifications of parallel resistor for WDIIH1, 230 V ac — 43.2 kΩ, 1%, 5 W. Orderable GE part number 336A4940HX-100

The allowable wetting voltage ranges are the same for None and Parallel resistor configuration. Refer to the *Voltage Ranges for Parallel Resistor Configuration* section for the actual voltage ranges for Parallel resistor configuration.

When WDIIH2 is used along with SDII, there are three configurations possible.

None – No resistor needs to be connected in series or parallel with the contact. No field line monitoring. Only Contact on/off detection

Parallel Resistor – User has to add a resistor in parallel with the contact in the field. This adds open fuse or field wire detection.

The specifications of parallel resistor for WDIIH2, 48 V dc — 6.04 kΩ, 1%, 1 W. Orderable GE part number 336A4940HT-100

Series Parallel Resistor – User has to add one resistor parallel to the contact and one resistor in series with the contact in the field. This adds open fuse or field wire detection and line-to-line field wire short detection.

The specifications of **parallel** resistor for WDIIH2, 48 V dc — 6.04 kΩ, 1%, 1 W. Orderable GE part number 336A4940HT-100

The specifications of **series** resistor for WDIIH2, 48 V dc — 3.32 kΩ, 1%, 0. 5 W. Orderable GE part number 336A4940HS-100

The permissible wetting voltage applied to WDIIH2 is equal to the most restrictive range for any wetted contact. If series-parallel resistors are used on any input then the voltage range listed for series-parallel inputs defines the range for all the channels of WDIIH2. If there are no signals using series-parallel resistors, then the less restrictive wetting voltage range applies.

Examples

When channels 1 to 16 in WDIIH2 are configured for None, then the voltage range applicable is the voltage range for None.

When channels 1 to 8 in WDIIH2 are configured for None and 9 to 16 are configured for Parallel Resistor then the voltage range applicable is the voltage range for None as the voltage ranges for None and Parallel Resistor are same.

When channels 1 to 16 in WDIIH2 are configured for Series Parallel Resistor, then the voltage range applicable is the voltage range for Series Parallel Resistor.

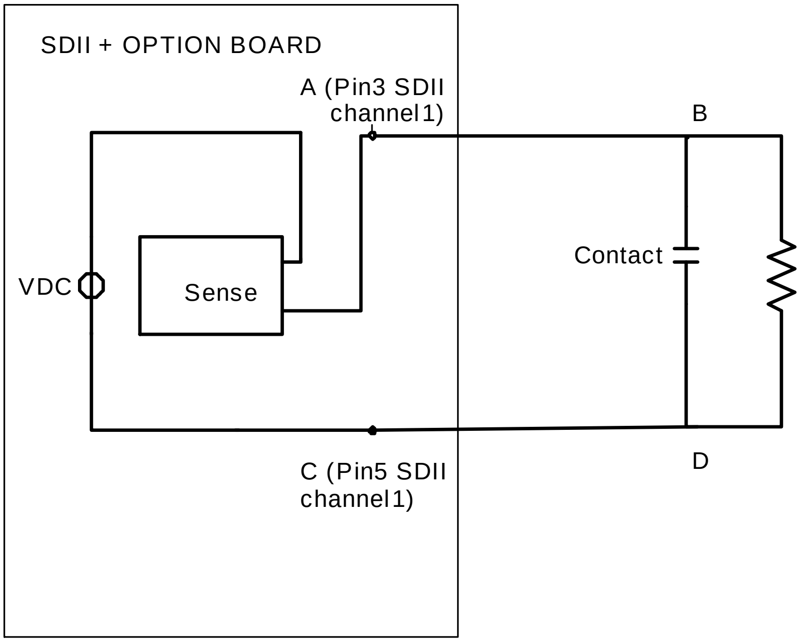
When channels 1 to 4 in WDIIH2 are configured for None, channels 5 to 14 are configured for Parallel Resistor, channel 15 is configured for Series Parallel Resistor, and channel 16 is configured as point isolated by removing the fuse then the voltage range applicable for all the first 15 channels is the voltage range for Series Parallel Resistor. The voltage range applicable for the 16th channel, which is configured as point isolated by removing the fuse, is the voltage range for point isolated inputs.

When WDIIH3 is used along with SDII, the same options as WDIIH2 are available except the point isolated input: None, Parallel Resistor, and Series Parallel Resistor.

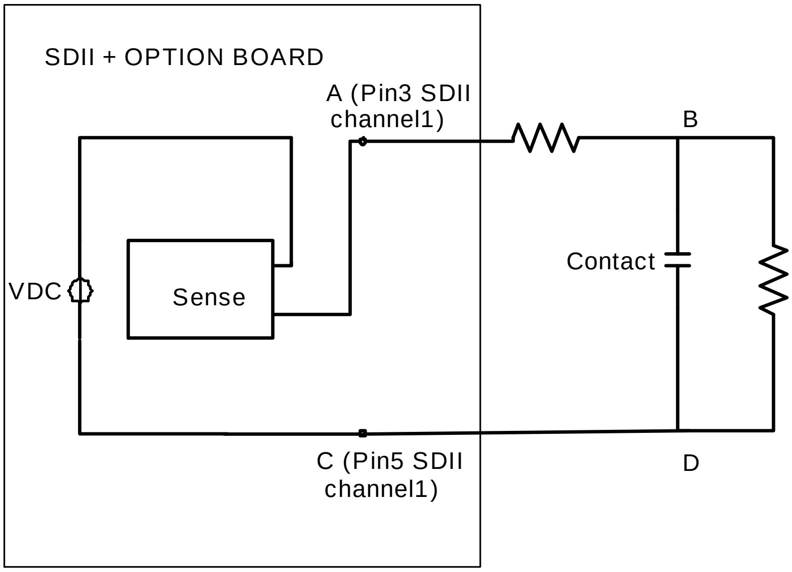
For parallel resistor connections, the specifications of parallel resistor for WDIIH3, 125 V dc —18.2 kΩ, 1%, 2 W. Orderable GE part number 336A4940HV-100

For Series-Parallel connections, the specifications of parallel resistor for WDIIH3, 125 V dc —18.2 kΩ, 1%, 2 W and the specification for series resistor for WDIIH3, 125 V dc—10 kΩ, 1%, 2 W. Orderable GE part number 336A4940HU-100

For WDIIH1, WDIIH2 and WDIIH3 Parallel Resistor configuration, the resistor is connected as follows.



For WDIIH2 and WDIIH3 Series Parallel Resistor configuration, the resistors are connected as follows.



6.3.3.8 Ground Fault (in Parallel Resistor Configuration)

If the user has hard ground so that common ground is tied up with the chassis or with earth, this is the same condition as contact true for the Parallel Resistor configuration. Irrespective of contact condition, it is treated as closed in normal configuration and is treated as false in Invert configuration. If the lower line to the contact is shorted to the chassis, there is no effect and it works normally and keeps detecting contact true/false and fuse blown/line open condition.

The JPDE diagnostic displays the line fault based on its configuration for fault detection if the JP1 jumper on JPDE is inserted. The following conditions are necessary for this to happen: there is no hard ground; the wetting voltage is taken from JPDE; any line to the contact is shorted to chassis in the field.

6.3.3.9 Ground Fault (in Series Parallel Resistor Configuration)

If the user has hard ground so that common ground is tied up with the chassis or with earth, this is the same condition as contact true for the Series Parallel Resistor configuration. Irrespective of contact condition, it is treated as closed in normal configuration and is treated as false in Invert configuration. If the lower line to the contact is shorted to chassis, there is no effect and it works normally and keeps detecting contact true/false and fuse blown/line open condition.

The JPDE diagnostic displays the line fault based on its configuration for fault detection if the JP1 jumper on JPDE is inserted. The following conditions are necessary for this to happen: there is no hard ground; the wetting voltage is taken from JPDE; any line to the contact is shorted to chassis in the field.

6.3.3.10 Voltage Ranges for Parallel Resistor Configuration

Voltage ranges:

- 18.5 to 32 V dc, nominal 24 V dc (WDIIH1) 32 to 64 V dc, nominal 48 V dc (WDIIH2)
- 70 to 145 V dc, nominal 125 V dc (WDIIH3)
- 90 to 143 V rms ac, nominal 115 V rms ac, 50/60 Hz ±3 Hz (WDIIH1)
- 180 to 264 V rms ac, nominal 230 V rms ac, 50/60 Hz ±3 Hz (WDIIH1)

Note 250 V dc range is not supported in this configuration as no WDII board can support 250 V dc range for system wetting.

If the wetting voltage goes out of the above ranges (Board level wetting voltage configuration is applicable only for WDIIH1; for WDIIH2 this value is fixed to 48 V dc and for WDIIH3 it is fixed to 125 V dc), an invalid voltage alarm occurs and the status LED indicator turns RED. Contact status is not reported if there is invalid voltage. Accuracy for voltage monitoring for Invalid voltage alarm: ±6%.

Note Some AC sensors acting as switches may have a low enough OFF impedance (due to internal RC snubbers) causing the voltage to drop below the wetting range when using a parallel resistor (refer to the section *Field Line Fault Monitoring*). This can be found by measuring the voltage at the terminal block and comparing it to the wetting range. For example, some sensors used with 115 V ac with the recommended 22K parallel resistor showed 47 V of signal when *off*, causing the signal to be declared U when FALSE. By increasing the parallel resistor to 39K, the off state voltage dropped to 35 V for a stable FALSE. Be sure to use appropriately rated resistors for 2 W or higher dissipation.

6.3.3.11 Voltage Ranges for Series Parallel Resistor Configuration

Voltage ranges:

- 42 to 56 V dc, nominal 48 V dc (WDIIH2)
- 90 to 145 V dc, nominal 125 V dc (WDIIH3)

Note 250 V dc range is not supported in this configuration as no WDII board can support 250 V dc range for system wetting.

If the wetting voltage goes out of the above ranges (Board level wetting voltage configuration is applicable only for WDIIH1; for WDIIH2 this value is fixed to 48 V dc and for WDIIH3 it is fixed to 125 V dc), an invalid voltage alarm occurs and the status LED indicator turns RED. Contact status is not reported if there is invalid voltage. Accuracy for voltage monitoring for Invalid voltage alarm: ±6%.

6.3.3.12 Sequence of Events (SOE)

The Sequence of Events (SOE) function records contact transitions using time stamping to display the sequence. It can be configured to be enabled or disabled.

Note SOE accuracy for contacts with DC voltage — ±1 ms. SOE accuracy for contacts with AC voltage — ±3 ms

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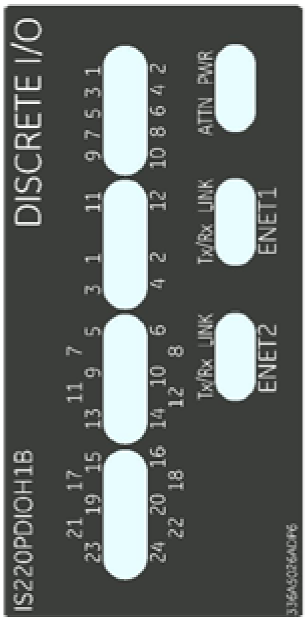
The SOEs are only for contact transitions and not for the faults related to field line monitoring. When the system is configured for field line monitoring (Parallel/ Series Parallel Resistor) in subsequent transitions the SOEs are logged as follows:

- If false, the contact in default configuration directly changes to the line-to-line short condition and one SOE is logged. The contact state in the ToolboxST application is TRUE UNHEALTHY (TRUE-U). The SOE needs to be ignored in this case, since the actual contact state does not change from False to True.
- If true, the contact in default configuration directly changes to the open wire condition and one SOE is logged. The contact state in the ToolboxST application is FALSE UNHEALTHY (FALSE-U). The SOE needs to be ignored in this case, since the actual contact state does not change from False to True.
- If true, the contact in invert configuration directly changes line-to-line short condition and one SOE is logged. The contact state in the ToolboxST application is FALSE UNHEALTHY (FALSE-U). The SOE needs to be ignored in this case, since the actual contact state does not change from False to True.
- If false, the contact in invert configuration directly changes to open wire condition and one SOE is logged. The contact state in the ToolboxST application is TRUE UNHEALTHY (TRUE-U). The SOE needs to be ignored in this case, since the actual contact state does not change from False to True.
- If false, the contact in default configuration directly changes to open wire condition and no SOE is logged. The contact state in the ToolboxST application is FALSE UNHEALTHY (FALSE-U).
- If true, the contact in default configuration directly changes to line-to-line short condition and no SOE is logged. The contact state in the ToolboxST application is TRUE UNHEALTHY (TRUE-U)
- If true, the contact in Invert configuration directly changes to open wire condition and no SOE is logged. The contact state in the ToolboxST application is TRUE UNHEALTHY (TRUE-U)
- If false, the contact in Invert configuration directly changes to line-to-line short condition and no SOE is logged. The contact state in the ToolboxST application is FALSE UNHEALTHY (FALSE-U)

If the line monitoring is configured (Parallel/ Series Parallel Resistor), and the wetting voltage changes suddenly (within 100 ms) by more than 7.5% the wrong detection can happen for contact open or closed condition and wrong the SOEs can be logged. When line fault occurs, it will be declared after 20 ms during which contact status reported is as the last contact condition.

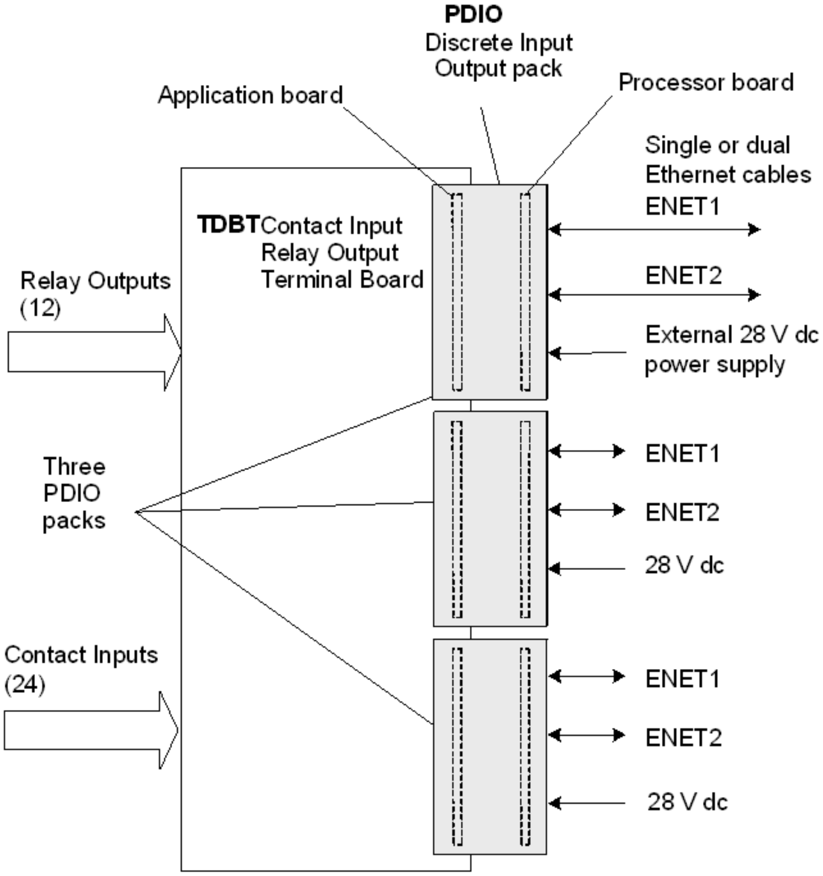
7 PDIO Discrete I/O Module

7.1 PDIO Discrete I/O Pack



The Discrete I/O pack (PDIO) provides the electrical interface between one or two I/O Ethernet networks and a discrete input/output terminal board. The PDIO contains a BPPx processor board and an acquisition board specific to the discrete input/output function. The I/O pack accepts up to 24 contact inputs, controls up to 12 relay outputs, and receives terminal board specific feedback signals. The associated terminal board determines voltage capability of the PDIO. System input to the I/O pack is through dual RJ-45 Ethernet connectors and a three-pin power input. Discrete signal input/output is through a DC-62 connector that connects directly with the associated terminal board connector. Visual diagnostics are provided through indicator LEDs.

The PDIO is the functional equivalent of a PDIA and a PDOA I/O pack combined into a single assembly. For simplex applications, it is mounted to a TDBS terminal board, which is the equivalent of a SRLY relay terminal board combined with a STCI contact input terminal board. For TMR applications, it is mounted to a TDBT terminal board, and can include a WROB option board for fused and sensed power distribution to the first six relay outputs and dedicated power to the last relay output. The following figure displays the signals for three PDIO I/O packs mounted on a TDBT terminal board.



7.1.1 Compatibility

The PDIO I/O pack includes one of the following compatible BPPx processor boards:

- The PDIOH1A contains a BPPB processor board.
- The PDIOH1B contains a functionally compatible BPPC processor board that is supported in ControlST* software suite V04.04 and later.

Redundancy refers to the number of I/O packs used in a signal path. The following are valid for PDIO.

- Simplex uses one I/O pack with one or two network connections.
- TMR uses three I/O packs with one network connection on each.

The PDIO I/O pack is compatible the following terminal and option boards.

Terminal Board	Contact Input Voltage	Redundancy	Option Boards
TDBSH2A	24 V dc	Simplex	WROB, WROF, WROG
TDBSH4A	48 V dc	Simplex	WROB, WROF, WROG
TDBSH6A	125 V dc	Simplex	WROB, WROF, WROG
TDBSH8A[1]	24 V dc	Simplex	
TDBTH2A	24 V dc	TMR	WROB
TDBTH4A	48 V dc	TMR	WROB
TDBTH6A	125 V dc	TMR	WROB
TDBTH8A[1]	24 V dc	TMR	

[1] These terminal boards are specifically designed for use in hazardous locations.

7.1.2 Installation

Warning

TDBSH8 or TDBTH8 terminal boards should not be used with intrinsic safety barriers.

Caution

When the solenoids are connected to the relay outputs, make sure that the solenoid coil rating does not exceed the voltage, current rating of the relay contacts given in the TDBS and TDBT specifications.

Caution

Discrete output option boards (such as WROB,WROF, and WROG) are not HazLoc certified, and shall not be used with TDBS or TDBT terminal boards in hazardous (classified) locations.

➢ **To install the PDIO I/O pack**

1. Securely mount the desired terminal board.
2. Directly plug the PDIO I/O pack into the terminal board connectors.
3. Mechanically secure the I/O pack(s) using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right-angle force applied to the DC-62 pin connector between the I/O pack and the terminal board. The adjustment should only be required once in the service life of the product.

Note The PDIO mounts directly onto the terminal board. Simplex terminal boards have a single DC-62 pin connector that receives the PDIO. TMR-capable terminal boards have three DC-62 pin connectors, one used for simplex operation, two for dual operation, and three for TMR operation. PDIO directly supports all of these connections.

4. Plug in one or two Ethernet cables depending on the system configuration. The pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
5. Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to remove power from the cable before plugging it in because the I/O pack has inherent soft-start capability that controls current inrush on power application.
6. Use the ToolboxST* application to configure the I/O pack as necessary. From the Component Editor, press F1 for help.

7.1.2.1 Connectors

The I/O pack contains the following connectors:

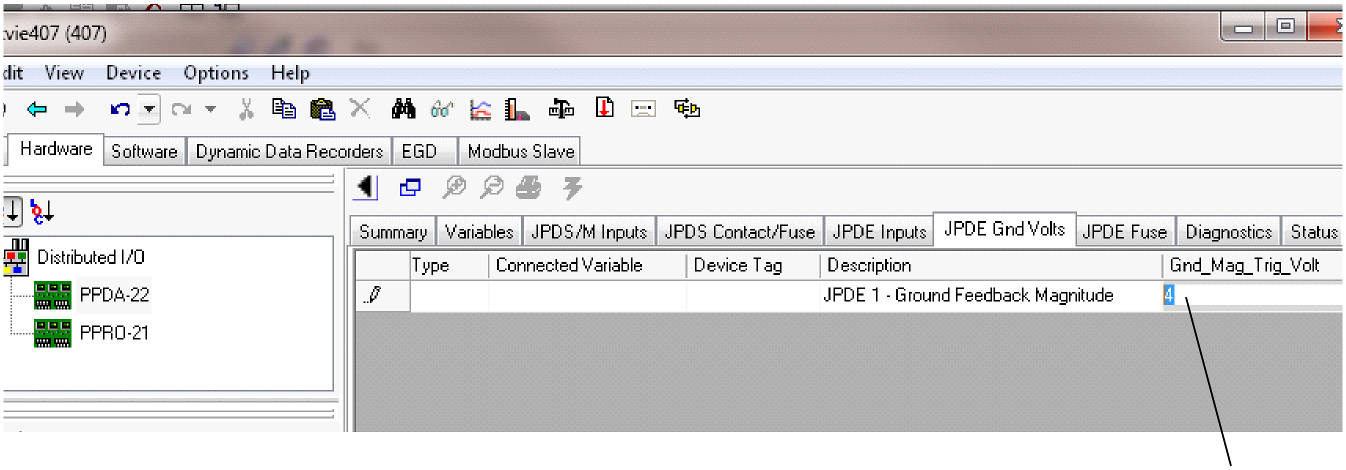
- A DC-62 pin connector on the underside of the PDIO I/O pack connects directly to the discrete input terminal board. The connector contains the 24 input signals, ID signal, relay coil power, and feedback multiplex command.
- An RJ-45 Ethernet connector named ENET1 on the side of the pack is the primary system interface.
- A second RJ-45 Ethernet connector named ENET2 on the side of the I/O pack is the redundant or secondary system interface.
- A 3-pin power connector on the side of the pack is for 28 V dc power for the I/O pack and terminal board.

7.1.2.2 Ground Fault Detection

If using TDBSH8A or TDBTH8A terminal boards, set the PPDA I/O pack, JPDE Gnd Volts, Ground Fault Threshold Feedback Magnitude (GND_Mag_Trig_Volt) limit at 4 V dc. Ground faults are annunciated when an excitation voltage output is grounded. The current limiting resistor in series with each excitation voltage output requires a lower threshold for ground fault detection.

➢ **To set the ground fault threshold**

1. From the ToolboxST application, Component Editor, Hardware Tab, Tree View, select the PPDA I/O pack that is attached to the JPDE power distribution board.
2. From the Summary View, select the **JPDE Gnd Volts** tab.



	Type	Connected Variable	Device Tag	Description	Gnd_Mag_Trig_Volt
				JPDE 1 - Ground Feedback Magnitude	4

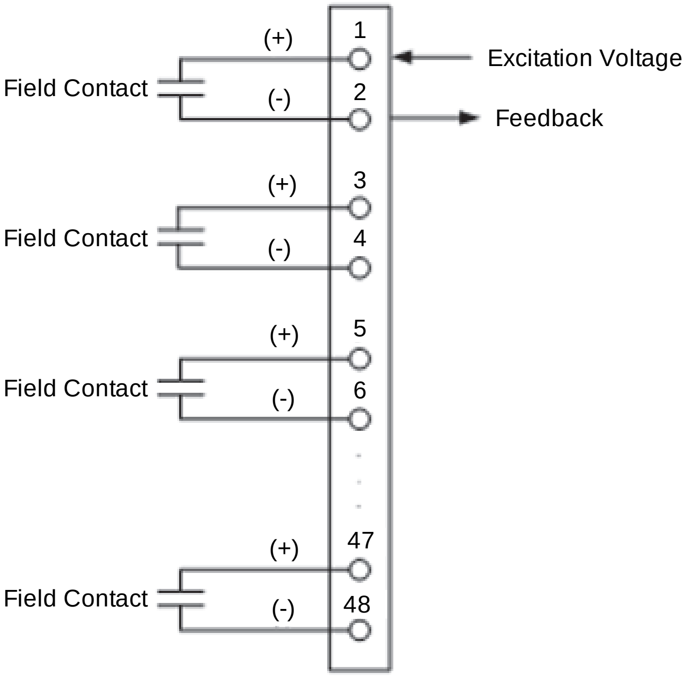
Change the value to 4.

7.1.2.3 Excitation Channels

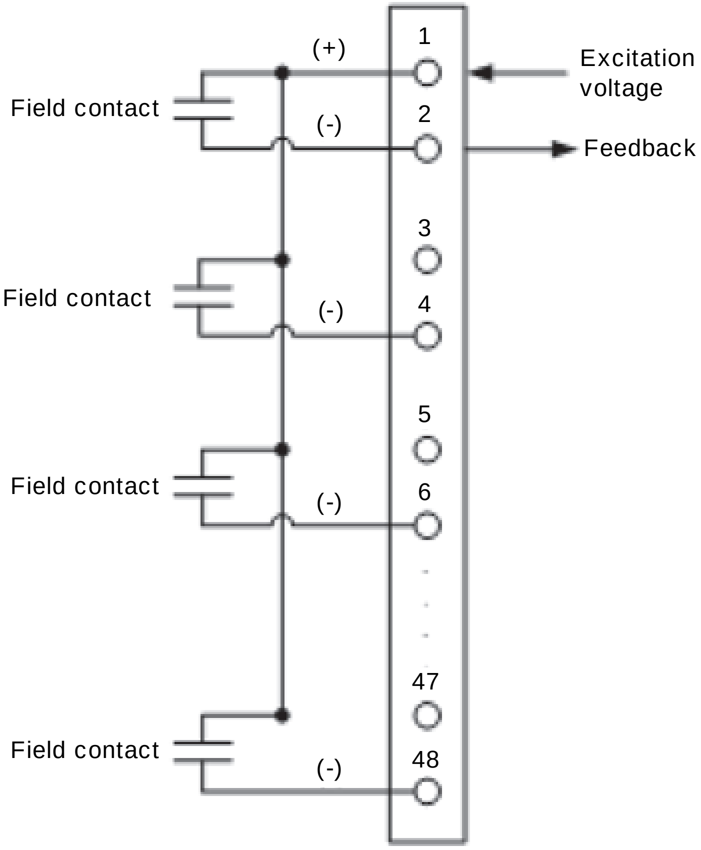
Warning

For TDBSH8A and TDBTH8A, each excitation voltage output can connect to only one field contact. In the application world, this is known as *home run* wiring. Branching one excitation voltage output to multiple contacts will cause misoperation and is not allowed. Grounding multiple excitation voltage outputs is not allowed as this will result in self-test failures or diagnostic alarms, as well as overheating of the terminal board.

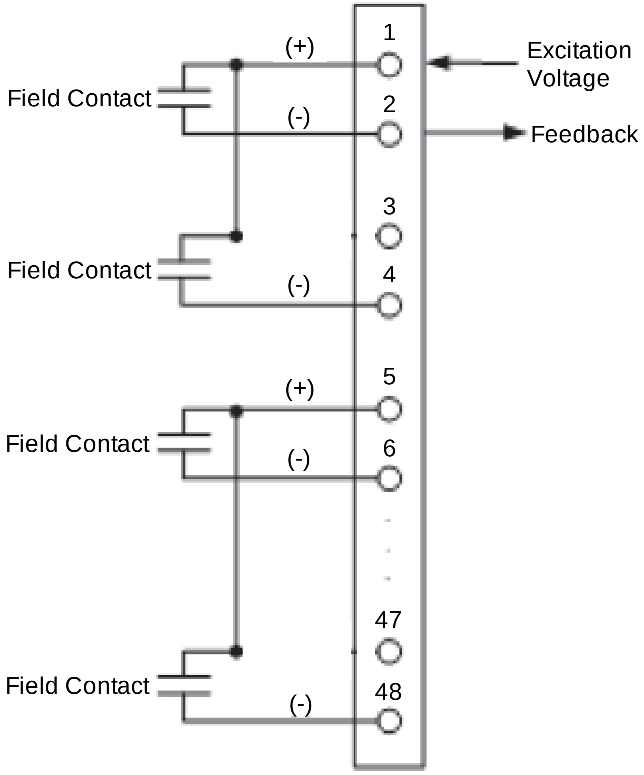
The following figures display correct configuration of excitation voltage channels based on compatible terminal board.



Correct Excitation Voltage Channels with TDBSH8A and TDBTH8A



One Excitation Voltage Channel for Multiple Field Contacts with TDBSH2A and TDBTH2A



Mixed Excitation Voltage of Different Channels with TDBSH2A and TDBTH2A

7.1.3 Operation

The following features are common to the distributed I/O modules:

- *BPPx Processor*
- *Processor LEDs*
- *Power Management*
- *ID Line*
- *I/O Module Common Diagnostic Alarms*

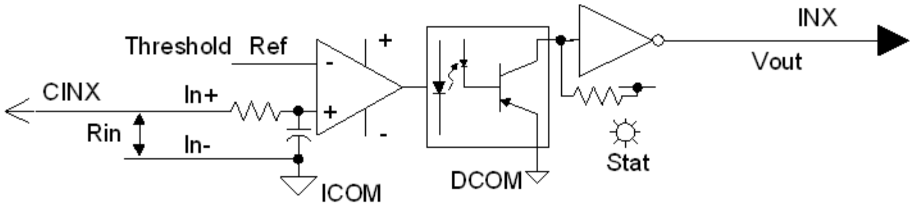
7.1.3.1 Connectors

The I/O pack contains the following connectors:

- A DC-62 pin connector on the underside of the PDIO I/O pack connects directly to the discrete input terminal board. The connector contains the 24 input signals, ID signal, relay coil power, and feedback multiplex command.
- An RJ-45 Ethernet connector named ENET1 on the side of the pack is the primary system interface.
- A second RJ-45 Ethernet connector named ENET2 on the side of the I/O pack is the redundant or secondary system interface.
- A 3-pin power connector on the side of the pack is for 28 V dc power for the I/O pack and terminal board.

7.1.3.2 Contact Input Signals

The discrete input/output acquisition board provides the second stage of signal conditioning and level shifting to interface the terminal board inputs to the control logic. Initial signal conditioning is provided on the terminal board. The discrete input acquisition input circuit is a comparator with a variable threshold. Each input is isolated from the control logic through an opto-coupler and an isolated power supply. The inputs are not isolated from each other. Each of the twenty-four inputs has filtering, hysteresis, and a yellow status LED, that indicates when an input is picked up. The LED will be OFF when the input is dropped-out. The LEDs are grouped at the bottom left of the PDIO I/O pack.

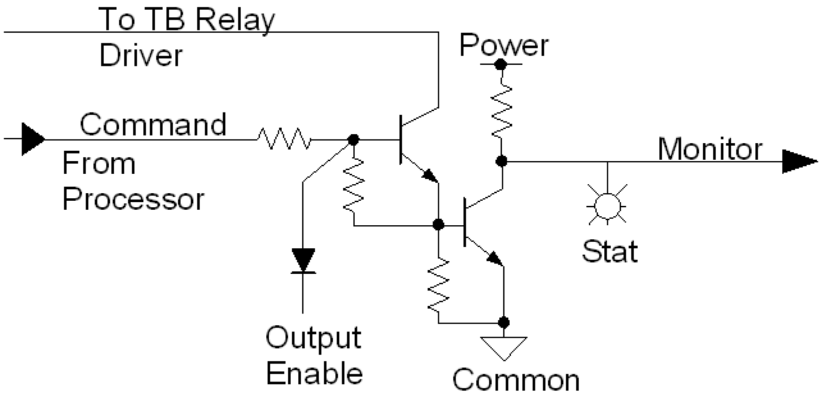


7.1.3.3 Variable Input Threshold

The input threshold is derived from the contact wetting voltage input terminal. In most applications this voltage is scaled to provide a 50% input threshold. This threshold is clamped to 13% to prevent an indeterminate state if the contact wetting voltage drops to zero. If the contact wetting voltage drops below 40% of the nominal voltage, the under-voltage detector annunciates this condition to the control. A special test mode is provided to force the inputs from the control pack. Every four seconds, the threshold is pulsed high and then low and the response of the opto-couplers is checked. Non-responding inputs are alarmed.

7.1.3.4 Relay Command Signals

The PDIO relay command signals are the first stage of signal conditioning and level shifting to interface the terminal board outputs to the control logic. Each output is an open collector transistor circuit with a current monitor to sense when the output is picked up and connected to a load. The status LEDs and monitor outputs indicate when an output is picked up and connected to the terminal board. If an output is commanded to be picked up and the correct load is not sensed, the status LED will be off and the monitor line will be false. The LEDs are grouped at the top left of the PDIO pack.



Relay Command Signals

7.1.3.5 Output Enable

All of the outputs are disabled during power application until a variety of internal self-tests are completed. An enable line reflects the status of all required conditions for operation. This function provides a path independent of the command to ensure relays stay dropped-out during power-up and initialization.

7.1.3.6 Monitor Inputs/Control

There are 15 inverting level shifting monitor input circuits. On a typical terminal board 12 of these circuits are used as relay contact feedbacks and the other three are used for fuse status. An inverting level shifting line is also provided from the control to the terminal board for status feedback multiplexing control allowing the pack to receive two sets of 15 signals from a terminal board.

7.1.3.7 Sequence Of Events (SOE)

All of the inputs and outputs may be individually configured to generate SOE records when the signal changes. It is not recommended to use output SOEs, but to instead use output feedback inputs (for example, relay feedback to log the relay SOEs). Input hardware is scanned at a 1000 Hz rate for SOE time stamping while output commands are captured when a change of command is received through Ethernet from the controller.

7.1.4 Specifications

Item	PDIO Specification
Number of Input Channels	24 DI and 12 form C contact DO
Input Isolation in Pack	Optical isolation to 1500 V on all inputs (group isolation)
Input Filter	Hardware filter, 4 ms
AC Voltage Rejection	60 V rms at 50/60 Hz at 125 V dc wetting voltage
Number of Relay Command Channels	12 relays
Relay and Coil Monitoring	12 relay/coil monitors, 3 fuse status feedbacks multiplexed to read status from 6 fuses. The selection of monitor feedbacks depends on the type of terminal board used, based on ID chip.
I/O Pack Response Time	From Ethernet command to output is typically 4 ms.
SOE Reporting	Each relay may be configured to report operation in the sequence of events (SOE) record.
Frame Rate	System dependent scan rate for control purposes 1,000 Hz scan rate for sequence of events monitoring
Fault Detection	Loss of contact input wetting voltage Non-responding contact input in test mode Incorrect terminal board Relay position feedback using contact pair separate from load contacts
Ambient Rating for Enclosure Design†	PDIOH1B is rated from -40 to 70°C (-40 to 158 °F) PDIOH1A is rated from -30 to 65°C (-22 to 149 °F)

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

7.1.5 Diagnostics

The I/O pack performs the following self-diagnostic tests:

- A powerup self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware.
- Continuous monitoring of the internal power supplies for correct operation.
- A powerup check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set.
- Monitoring for loss of contact input wetting voltage on the terminal board takes place at the selected system frame rate.
- Detecting a non-responding contact input during diagnostic test. In this test, the threshold is pulsed high and low and the response of the opto-couplers is checked. The test typically runs once every four seconds, and can be observed as a very brief period when all twenty-four contact input lights turn on.
- A frame rate comparison is made between the commanded state of each relay drive and the feedback from the command output circuit.
- Relay board specific feedback is read by the pack and processed every frame. The information varies depending on the relay board type. Refer to relay terminal board documentation for feedback specifics.

7.1.6 Configuration

Note The following information is extracted from the ToolboxST application and represents a sample of the configuration information for this board. Refer to the actual configuration file within the ToolboxST application for specific information.

Parameter	Description	Choices
Input Point Parameters	Terminal board connected to PDIO	Connected, not connected
Input	Selection will enable Contact Inputs or Relay feedback inputs	Used, Unused
SignalInvert	Inversion makes signal true if contact is open	Normal, Invert
SeqOfEvents	Record contact transitions in sequence of events	Enable, Disable
DiagVoteEnab	Enable voting disagreement diagnostic, only present on TDBT.	Enable, Disable
SignalFilter	Contact input digital filter in milliseconds (in addition to 4 ms hardware filter)	Zero, Ten, Twenty, Fifty, Hundred
Output Point Parameters		
RelayOutput	Selection will enable use of the relay	Used, Unused
SignalInvert	Inversion makes relay closed if signal is false	Normal, Invert
SeqOfEvents	Record relay command transitions in sequence of events	Enable, Disable
FuseDiag	Enable fuse diagnostic - Will appear as configuration item for use with Fuse daughterboard	Enable, Disable
Output_State	Select the state of the Relay condition based on I/O pack going offline with controller	PwrDownMode, HoldLastValue, Output_Value

7.2 PDIO Specific Alarms

The following alarms are specific to the PDIO I/O pack.

34-45

Description Relay circuit [ ] fuse(s) blown

Possible Cause The PDIO I/O pack fuse status feedback indicates a possible blown fuse.

Solution Perform the following items in the following order:

- Using the following table, check the fuse(s) in the appropriate terminal board for a possible blown fuse.

Terminal Board Fuses

Relay Output Circuit	TDBSH#A with WROB	TDBSH#A with WROF	TDBSH1A with WROG	TDBTH#A with WROB
1	FU1 FU7	FU1	FU1	FU1 FU7
2	FU2 FU8	FU2	FU2	FU2 FU8
3	FU3 FU9	FU3	FU3	FU3 FU9
4	FU4 FU10	FU4	FU4	FU4 FU10
5	FU5 FU11	FU5	FU5	FU5 FU11
6	FU6 FU12	FU6	FU6	FU6 FU12
7	Not fused	FU7	FU7	Not fused
8	Not fused	FU8	FU8	Not fused
9	Not fused	FU9	FU9	Not fused
10	Not fused	FU10	FU10	Not fused
11	Not fused	FU11	FU11	Not fused
12	Not fused	FU12	FU12	Not fused

- Verify the contact wetting/input power to the terminal board.
- Verify the terminal board configuration and jumper settings (on WROBH1A).
- Verify that the I/O pack output and fuse diagnostics are enabled properly in the ToolboxST configuration.
- Confirm that all connectors, power plugs, I/O packs, and daughter boards are fully seated.
- If the problem persists, perform the following:
  - Replace the I/O pack.
  - Replace the WROB, F, or G daughter board.
  - Replace the terminal board. (This requires a ToolboxST configuration Build and Download to update the terminal board serial number.)

46

Description All Fuses Blown or No Terminal Board Excitation

Possible Cause All fuse sensing indicates an open fuse. This may be due to loss of input power to the terminal board. Without power to the fuses, the sensing may indicate a false open-fuse condition.

Solution

- Confirm the correct input power to terminal board.
- Check the I/O pack connector alignment and seating.
- Check the I/O pack configuration.
- Check all fuses.
- Replace the I/O pack.
- Replace the terminal board.

47-58

Description Relay Coil [ ] Failure

Possible Cause Relay feedback does not match commanded state

Solution

- Clear the voter disagreements (for TMR).
- Check the I/O pack connector alignment and seating.
- Check the I/O pack configuration.
- Replace the terminal board.

59-70

Description Relay Output Driver [ ] Failure

Possible Cause Relay command signal as seen at the I/O pack output connector to the terminal board does not match the commanded state.

Solution The command signal feedback requires a properly connected terminal board.

- Check the pack-terminal board connector alignment and seating.
- Replace the I/O pack.
- Replace the terminal board.

72-95

Description Contact Input [ ] not responding to self-test mode

Possible Cause The input hardware internal to I/O pack has experienced a failure.

Solution Replace the I/O pack.

96-119

Note This alarm is obsolete.

Description Contact Input [ ] not responding to low self-test mode

Possible Cause The input hardware internal to I/O pack has experienced a failure.

Solution Replace the I/O pack.

120

Description Excitation Voltage not valid, Contact Inputs not valid

Possible Cause

- The contact excitation may not be connected to the terminal board.
- The contact wetting voltage applied to the terminal board is not within the acceptable range for the board.

Solution

- Check the contact excitation voltage connections to the terminal board.
- Check the power distribution and wiring to ensure that correct wetting power is applied to the terminal board.

1050-1210

Description Logic Signal [ ] Voting Mismatch

Possible Cause In a TMR application, the values for the specified signal do not agree between the R, S, and T I/O packs.

Solution

- Verify that the R, S, and T I/O packs are equal with the ToolboxST configuration.
- Check the I/O pack power and networking.
- Check the I/O pack mounting on the terminal board.
- Replace the I/O pack.

7.3 TDBS Terminal Board for Simplex Discrete Input/Output

7.3.1 Functional Description

The Simplex Discrete Input/Output (TDBS) terminal board is designed for DIN-rail or flat mounting and works with the PDIO I/O pack. The I/O pack plugs into the D-type connector and communicates with the controller over Ethernet. A single connection point for the PDIO is provided with one or two network connections possible from the PDIO to the controller(s).

The TDBS terminal board accepts 24 group isolated contact inputs that are supplied with a nominal 24, 48, or 125 V dc wetting voltage from an external source. The contact inputs have noise suppression to protect against surge and high-frequency noise. TDBS provides 12 form-C relay outputs and accepts different W-type option boards to expand relay functions. All terminal board versions have pluggable terminal blocks.

7.3.1.1 TDBS Compatibility

Valid PDIO and TDBS Combinations

Terminal Board	Wetting Voltage
TDBSH2A	Nominal 24 V dc, floating, ranging from 16 to 32 V dc
TDBSH4A	Nominal 48 V dc, floating, ranging from 32 to 60 V dc
TDBSH6A	Nominal 125 V dc, floating, ranging from 100 to 145 V dc
TDBSH8A[1]	Nominal 24 V dc, floating or grounded, ranging from 16 to 31 V dc
[1] This terminal board is specifically designed for use in hazardous locations.	

The following three option boards are available for use with the TDBSH2A, H4A, or H6A:

- ***IS200WROBH1A*** turns the relay portion of TDBS into the functional equivalent of IS200TRLYH1B. This option provides fused and sensed power distribution to the first six relay outputs and dedicated power to the last relay output.
- ***IS200WROFH1A*** puts a single fuse in series with each relay common connection, and can be used for feedback from 9 to 240 V ac or from 12 to 125 V dc.
- ***IS200WROGH1A*** distributes power from an input connector to each relay through a single fuse, and can be used for feedback from 9 to 240 V ac or from 12 to 125 V dc.

Note When using WROB, WROF, or WROG, the incoming voltage can be either ac or dc.

7.3.2 Installation

Caution

Do not replace TDBSH2A with TDBSH8A without first installing ControlST software suite 4.05 or later.

Warning

TDBSH8A or TDBTH8A terminal boards shall not be used with intrinsic safety barriers.

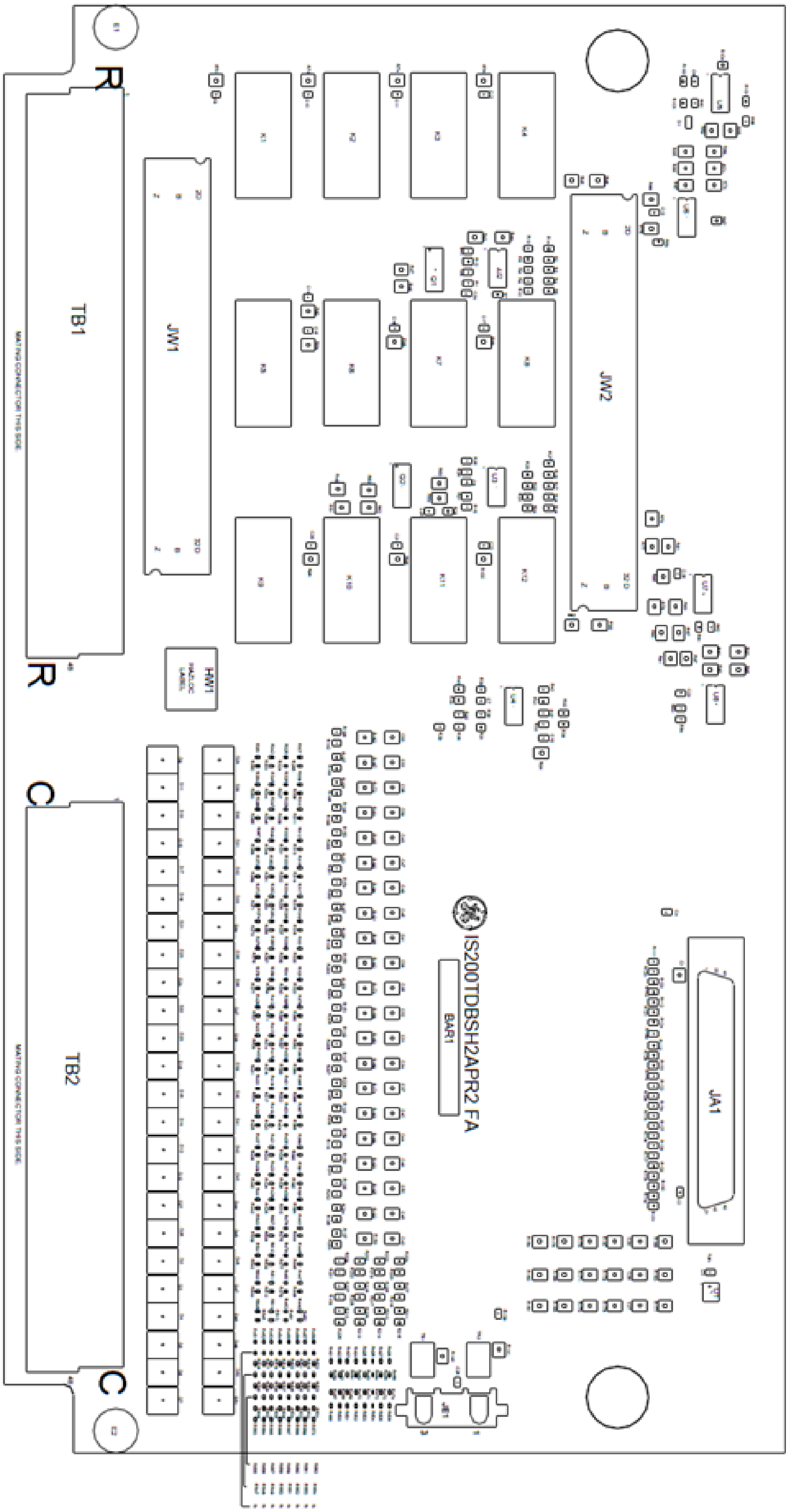
Caution

Discrete output option boards (such as WROBH1A, WROFH1A, and WROGH1A) are not HazLoc certified, and so shall not be used with TDBS or TDBT terminal boards in hazardous (classified) locations.

The TDBS plus a plastic insulator mounts on a sheet metal carrier that then mounts on a DIN rail. Optionally the TDBS plus insulator mounts on a sheet metal assembly that then bolts in a cabinet. The connections are wired directly to two sets of 48 point terminal blocks, typically using #24 - #12 AWG wires. The upper set of terminals, TB1, connects to the relay portion of the board and the lower set of terminals, TB2, connect to the contact input circuits. Shields should be terminated on a separate bracket.

For TDBSH2A, TDBSH4A, and TDBSH6A, the wetting voltage output terminals are all connected in parallel and fed from the positive voltage applied to JE1 pin 1. It is permissible to run a single wetting voltage lead from the board terminal to a group of remote contacts and then bring the individual contact wires back to the inputs. Negative or return wetting voltage is supplied by JE1 pin 3.

For TDBSH8A, each wetting voltage output terminal is protected by a separate internal current limit resistor. A separate wetting voltage lead must be run for each individual output.


R
TB1
JW1
K1
K2
K3
K4
K5
K6
K7
K8
K9
K10
K11
K12
JW2
HW1
R
C
TB2
IS200TDBSH2APR2 FA
BAR1
JA1
C

TDBS Layout

7.3.2.1 Relay Output Signals

If a relay option board is used, it plugs into TDBSH2A, 4A, 6A connectors JW1 and JW2 and is held in place by the force of the connectors. The following table identifies the function of each relay terminal point grouped as TB1 as it relates to the presence of an option board. If external power is to be supplied it is wired to a connector provided on the option board.

- NC – normally closed contact of a form C relay
- COM – common point of a form C relay contact
- NO – normally open contact of a form C relay
- SOL – return circuit path for a solenoid that is powered by the relay board
- VSENSE – the input to a voltage sensor that looks between VSENSE and COM
- RETURN – return power path for devices powered by the WROGH1A option board

Output Terminal	Relay	TDBSH2A, 4A, 6A	TDBSH2A, 4A, 6A + WROBH1A	TDBSH2A, 4A, 6A + WROFH1A with Fuses	TDBSH2A, 4A, 6A + WROFH1A no Fuses	TDBSH2A, 4A, 6A + WROGH1A
1	1	NC	NC	NC	NC	NC
2		COM	COM	COM (unfused)	COM	POWER
3		NO	NO	NO	NO	NO
4			SOL	COM (fused)	VSENSE	RETURN
5	2	NC	NC	NC	NC	NC
6		COM	COM	COM (unfused)	COM	POWER
7		NO	NO	NO	NO	NO
8			SOL	COM (fused)	VSENSE	RETURN
9	3	NC	NC	NC	NC	NC
10		COM	COM	COM (unfused)	COM	POWER
11		NO	NO	NO	NO	NO
12			SOL	COM (fused)	VSENSE	RETURN
13	4	NC	NC	NC	NC	NC
14		COM	COM	COM (unfused)	COM	POWER
15		NO	NO	NO	NO	NO
16			SOL	COM (fused)	VSENSE	RETURN
17	5	NC	NC	NC	NC	NC
18		COM	COM	COM (unfused)	COM	POWER
19		NO	NO	NO	NO	NO
20			SOL	COM (fused)	VSENSE	RETURN
21	6	NC	NC	NC	NC	NC
22		COM	COM	COM (unfused)	COM	POWER
23		NO	NO	NO	NO	NO
24			SOL	COM (fused)	VSENSE	RETURN
25	7	NC	NC	NC	NC	NC
26		COM	COM	COM (unfused)	COM	POWER
27		NO	NO	NO	NO	NO
28				COM (fused)	VSENSE	RETURN
29	8	NC	NC	NC	NC	NC
30		COM	COM	COM (unfused)	COM	POWER
31		NO	NO	NO	NO	NO
32				COM (fused)	VSENSE	RETURN
33	9	NC	NC	NC	NC	NC
34		COM	COM	COM (unfused)	COM	POWER
35		NO	NO	NO	NO	NO
36				COM (fused)	VSENSE	RETURN
37	10	NC	NC	NC	NC	NC
38		COM	COM	COM (unfused)	COM	POWER

Output Terminal	Relay	TDBSH2A, 4A, 6A	TDBSH2A, 4A, 6A + WROBH1A	TDBSH2A, 4A, 6A + WROFH1A with Fuses	TDBSH2A, 4A, 6A + WROFH1A no Fuses	TDBSH2A, 4A, 6A + WROGH1A
39		NO	NO	NO	NO	NO
40				COM (fused)	VSENSE	RETURN
41	11	NC	NC	NC	NC	NC
42		COM	COM	COM (unfused)	COM	POWER
43		NO	NO	NO	NO	NO
44				COM (fused)	VSENSE	RETURN
45	12	NC	NC	NC	NC	NC
46		COM	COM	COM (unfused)	COM	POWER
47		NO	NO	NO	NO	NO
48			SOL	COM (fused)	VSENSE	RETURN

7.3.2.2 Contact Input Signals

Contact input connections are made to the 48 terminals on the lower portion of the terminal board, grouped as TB2. Contact wetting voltage is provided to the board through the JE1 3-pin Mate-N-Lok® connector on the lower portion of the board.

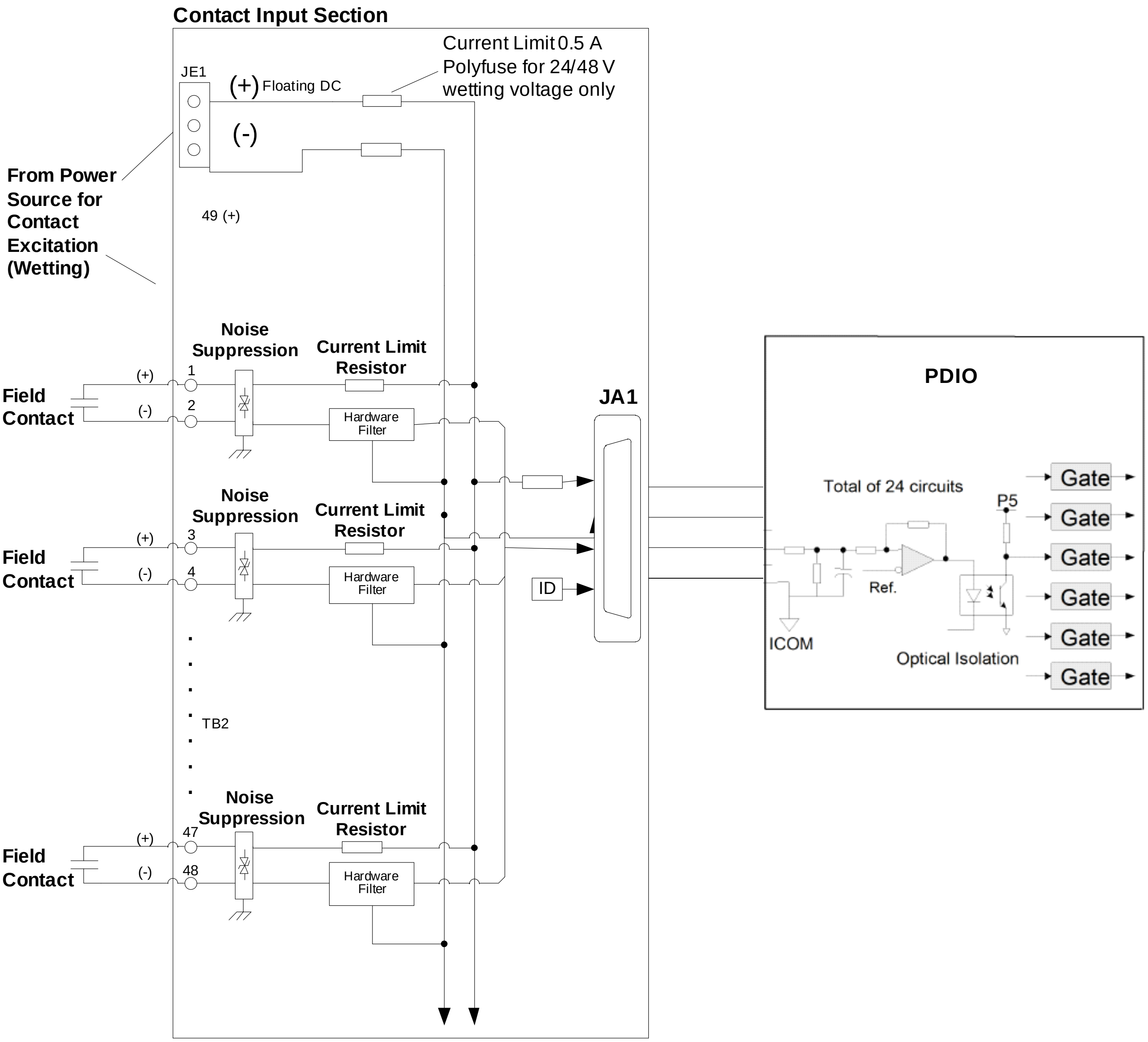
Terminal	Signal		Terminal	Signal
1	Wet 1		25	Wet 13
2	In 1		26	In 13
3	Wet 2		27	Wet 14
4	In 2		28	In 14
5	Wet 3		29	Wet 15
6	In 3		30	In 15
7	Wet 4		31	Wet 16
8	In 4		32	In 16
9	Wet 5		33	Wet 17
10	In 5		34	In 17
11	Wet 6		35	Wet 18
12	In 6		36	In 18
13	Wet 7		37	Wet 19
14	In 7		38	In 19
15	Wet 8		39	Wet 20
16	In 8		40	In 20
17	Wet 9		41	Wet 21
18	In 9		42	In 21
19	Wet 10		43	Wet 22
20	In 10		44	In 22
21	Wet 11		45	Wet 23
22	In 11		46	In 23
23	Wet 12		47	Wet 24
24	In 12		48	In 24

7.3.3 Operation

7.3.3.1 Contact Inputs

The contact input function and on-board signal conditioning are scaled for 24, 48, and 125 V dc wetting voltage. The input wetting voltage ranges are listed in the section, *TDBS Specifications*. The threshold voltage is 50% of the wetting voltage. Contact input currents are resistance limited to 2.5 mA on the first 21 circuits, and 10 mA on circuits 22 through 24. The 24 V dc supply on TDBSH2 is current limited to 0.5 A using polymer positive temperature coefficient fuses that can be reset. Filters reduce high-frequency noise and suppress surge on each input near the point of signal entry.

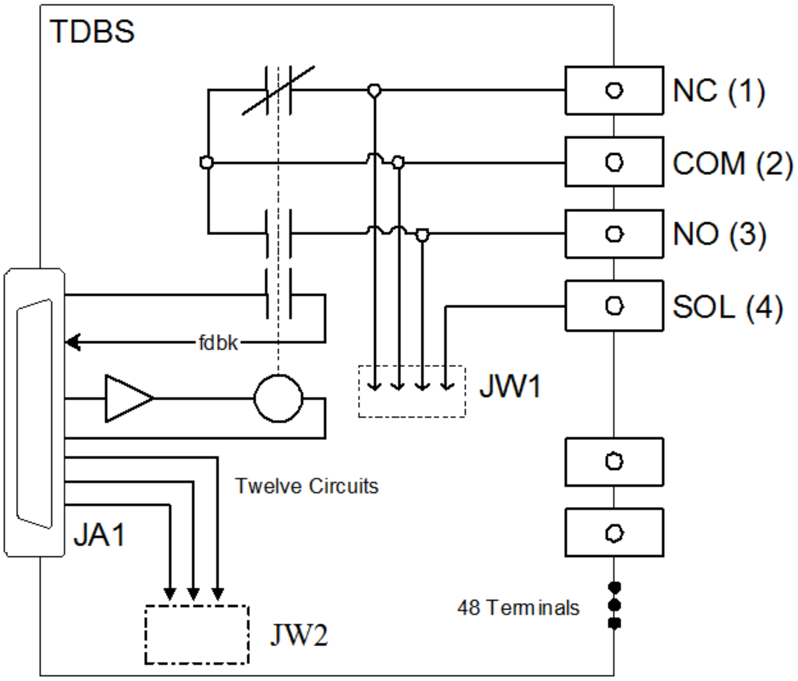
The discrete input voltage signals go to the I/O processor which passes them through optical isolators, converts them to digital signals, and transfers them to the controller. With TDBSH2A, TDBSH4A, and TDBSH6A, the contact input section has wetting voltage output terminals that are all connected in parallel and fed from the positive voltage applied to JE1 pin 1. Current limit resistors are omitted. In the following figure, TDBSH8A contact input section has a current limit resistor on each wetting voltage output.



TDBSH8A Contact Inputs

7.3.3.2 TDBS Relay Outputs

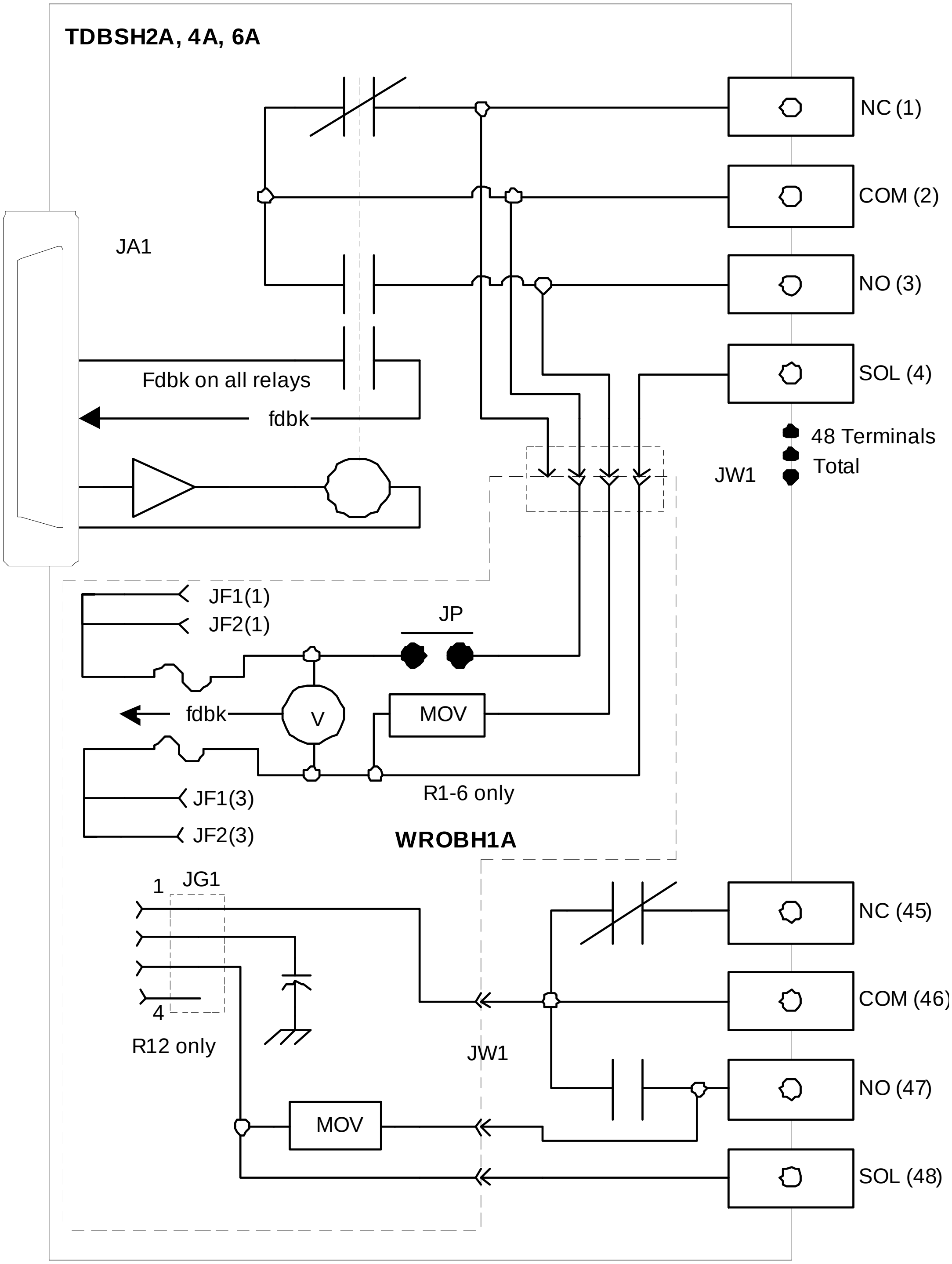
TDBS uses pluggable type terminals and has connectors JW1 and JW2 supporting option board connection. The relay portion of TDBS does not change between groups H2, H4, and H6, only the contact input circuits change. TDBS relays may be used at any specified ac or dc voltage without regard to board group. Electrically TDBS has the following circuit for each of the 12 relays:



Note Without an option board, the SOL terminal associated with each relay has no connection.

7.3.3.3 TDBSH2A, 4A, 6A + WROBH1A

Option board IS200WROBH1A adds capability to TDBS to yield a combination that has the same relay circuit functionality as an IS200TRLYH1B terminal board when used simplex. Included are fused sensed power distribution to the first six relays and dedicated power to the last relay. Electrically, TDBS plus WROBH1A has the following circuit. WROBH1A has default fuse values of 3.15 A. Connector JW2 and its connections to JA1 are omitted for clarity.



Both sides of the power distribution on relays 1-6 are fused allowing the board for use in systems where dc power is floating with respect to earth. Fuse voltage feedback is compatible with 24 V, 48 V, and 125 V dc applications, as well as 120 V and 240 V ac applications.

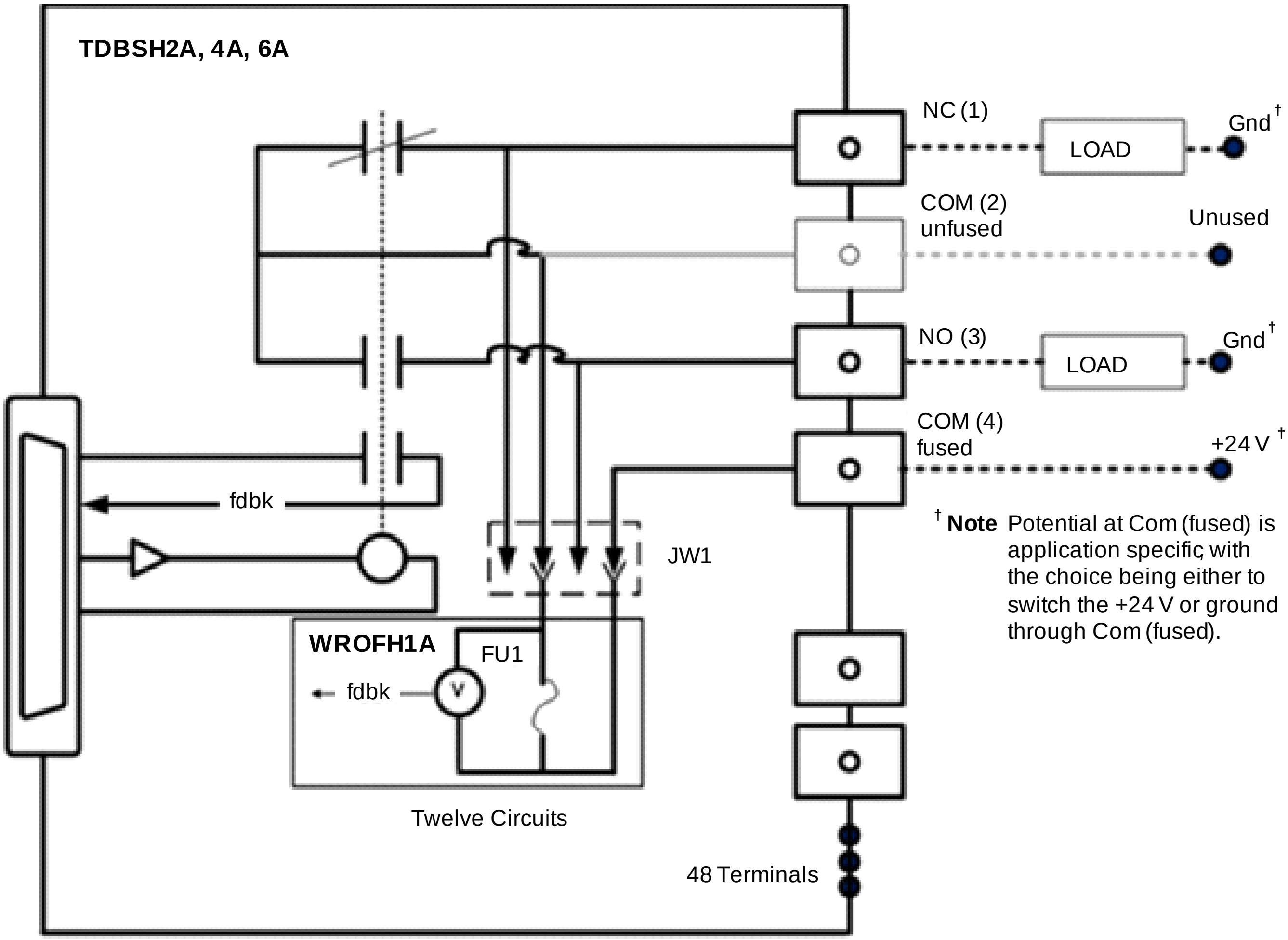
Relationship Between Fuses, Jumpers, Relays, and Terminals

Relay	+Fuse	-Fuse	Jumper	Terminals
1	FU7	FU1	JP1	1-4
2	FU8	FU2	JP2	5-8
3	FU9	FU3	JP3	9-12
4	FU10	FU4	JP4	13-16
5	FU11	FU5	JP5	17-20
6	FU12	FU6	JP6	21-24

7.3.3.4 TDBSH2A, 4A, 6A + WROFH1A Fused in Series

Option board IS200WROFH1A adds an optional fuse in series with the COM connection for each relay output by using the SOL terminal in place of COM. Isolated voltage sensing that is not polarity sensitive is provided for each fuse. Refer to the *TDBS Compatibility* section for compatible applications. The WROFH1A has a default fuse value of 3.15 A.

With the original application for this board, each relay output has a fuse in series with power applied from an external source. In the following figure, connector JW2 and its connections to JA1 are omitted for clarity. Fuses FU1 through FU12 are associated with relay circuits 1 through 12 respectively.

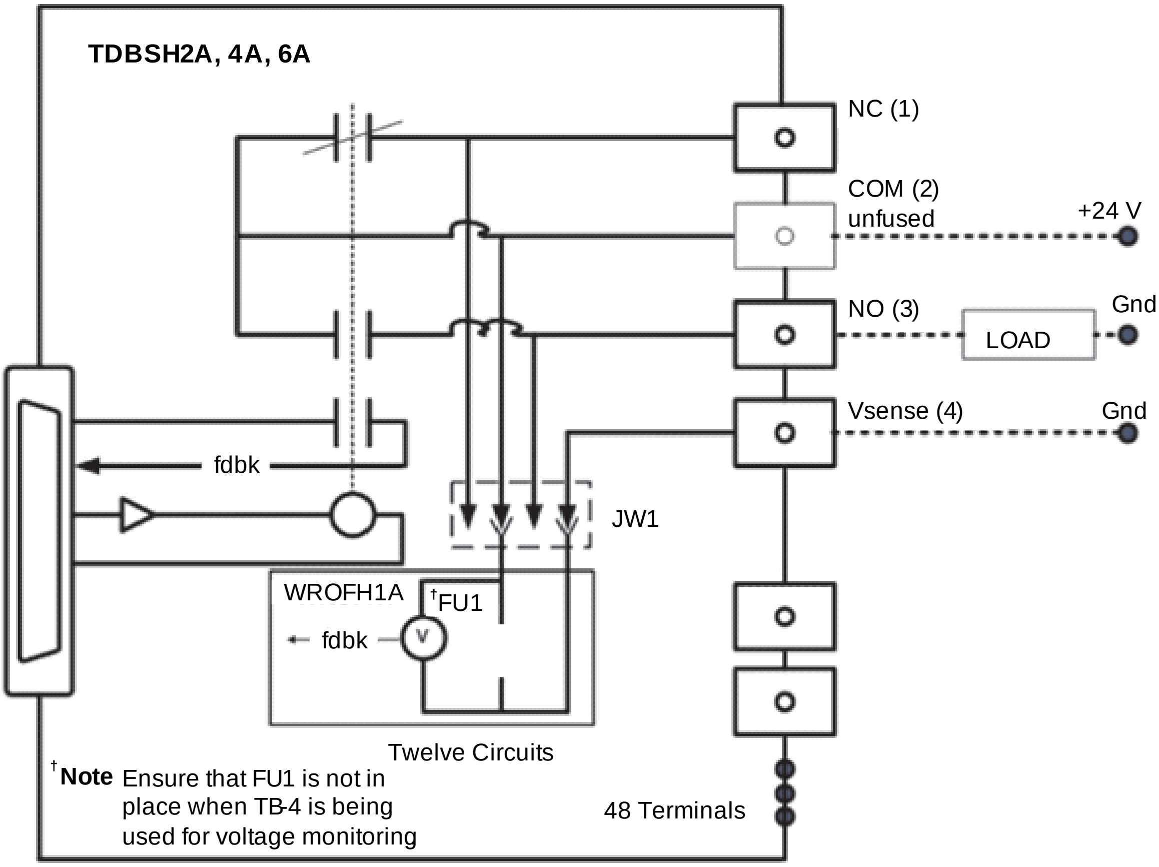


† **Note** Potential at Com (fused) is application specific, with the choice being either to switch the +24 V or ground through Com (fused).

7.3.3.5 TDBSH2A, 4A, 6A + WROFH1A Isolated Contact Voltage Feedback

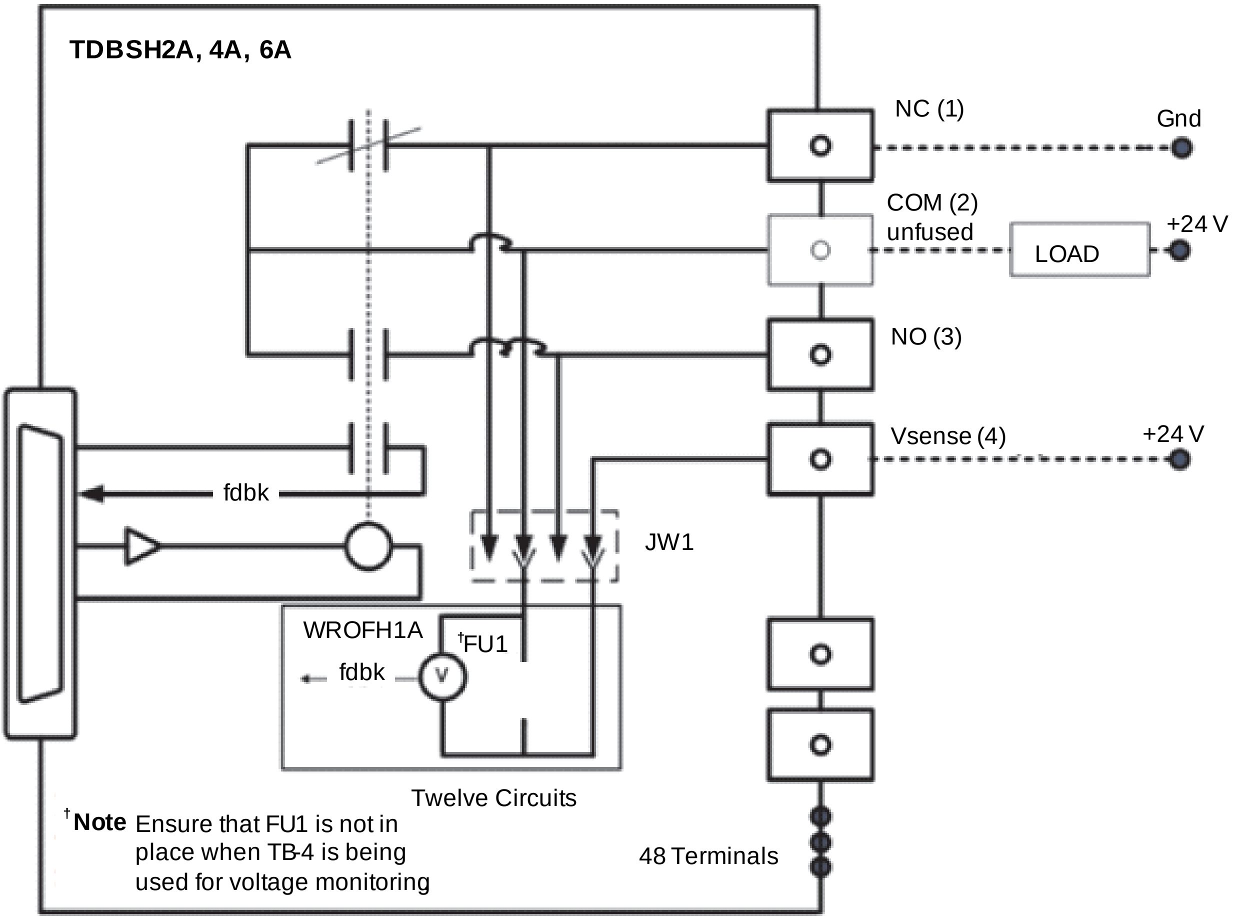
With the alternate application of this board, if the fuse is removed from a circuit, the isolated voltage detector remains. The fourth terminal may now be wired to either the NC or NO terminal to provide isolated contact voltage feedback. I/O pack firmware has a configuration option to turn off fuse blown alarm generation for a given relay if it is being used in this fashion.

Note Refer to the TDBS *Installation* section. The fourth screw is Vsense.



†**Note** Ensure that FU1 is not in place when TB-4 is being used for voltage monitoring

Normally Open

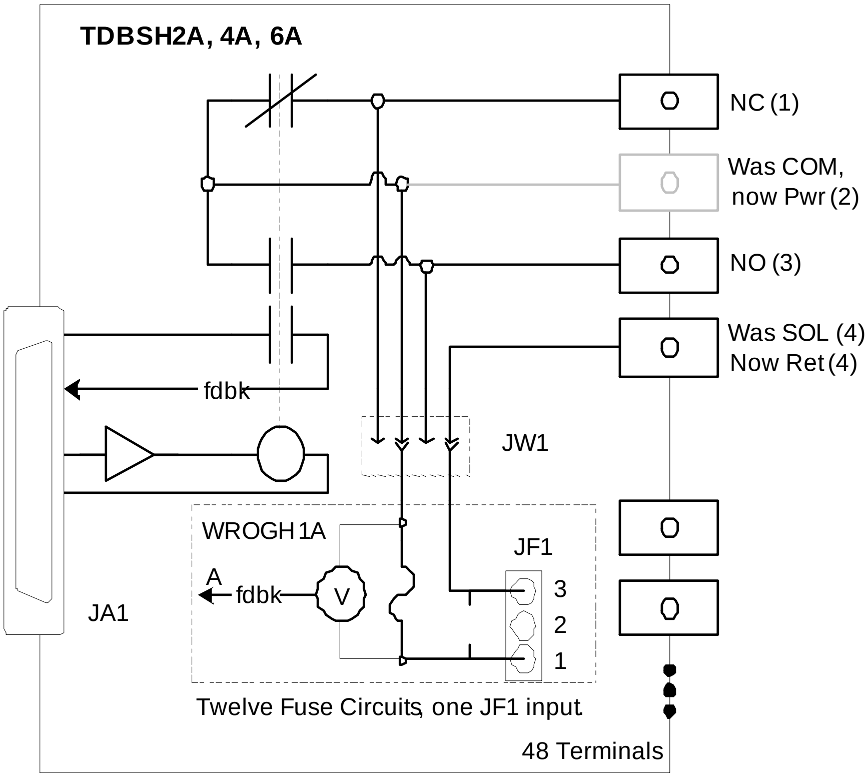


†**Note** Ensure that FU1 is not in place when TB-4 is being used for voltage monitoring

Normally Closed

7.3.3.6 TDBSH2A, 4A, 6A + WROGH1A

Option board IS200WROGH1A adds fused power distribution for all twelve relay outputs. Isolated voltage sensing that is not polarity sensitive is provided for each fuse. Refer to the *TDBS Compatibility* section for compatible applications. The WROGH1A has a default fuse value of 3.15 A. Electrically, TDBSH2A, 4A, 6A plus WROGH1A has the following circuit. Connector JW2 and its connections to JA1 are omitted for clarity. Fuses FU1 through FU12 are associated with relay circuits 1 through 12 respectively.



7.3.4 Specifications

Item	TDBS Specification
Terminal Blocks	Euro Style Box-type Pluggable
Number of Input Channels	24 dry contact voltage input channels
Wetting Voltage	H2A: Nominal 24 V dc, floating, ranging from 16 to 32 V dc H4A: Nominal 48 V dc, floating, ranging from 32 to 60 V dc H6A: Nominal 125 V dc, floating, ranging from 100 to 145 V dc H8A: Nominal 24 V dc, floating or grounded, ranging from 16 to 31 V dc
Input Current	H2A, H8A: Nominal 24 V dc applications: First 21 circuits draw 2.5 mA, Last three circuits draw 10 mA
	H4A: Nominal 48 V dc applications: First 21 circuits draw 2.5 mA, Last three circuits draw 10.4 mA
	H6A: Nominal 125 V dc applications: First 21 circuits draw 2.55 mA, Last three circuits draw 10 mA
Input Filter	Hardware filter, 4 ms
Fault Detection in I/O Board	Loss of contact input wetting voltage Non-responding contact input in test mode
AC Voltage Rejection	H2A, H8A: 12 V rms at 24 V dc wetting voltage H4A: 24 V rms at 48 V dc wetting voltage H6A: 60 V rms at 125 V dc wetting voltage
Number of Relay Channels	12 relays
Rated Voltage on Relay Contacts	a: Nominal 24 V dc, 48 V dc, or 125 V dc b: Nominal 120 V ac or 240 V ac
Max Load Current	a: 0.6 A for 125 V dc operation b: 1.2 A for 48 V dc operation c: 3.15 A for 24 V dc operation d: 3.15 A for 120/240 V ac, 50/60 Hz operation
Max Response Time On	25 ms typical
Max Response Time Off	25 ms typical
Contact Material	Silver-Nickel Alloy
Contact Life	Electrical operations: 100,000 Mechanical operations: 5,000,000
Fault Detection	Relay position feedback using contact pair separate from load contacts.
Size - TDBS	17.8 cm wide x 33.02 cm high (7.0 in x 13.0 in)
Technology	Surface-mount

Option Boards

WROBH1A Option Board	
Powered Output Circuits	6 fused, associated with relays 1-6, fed from parallel connectors JF1 and JF2 (GE part number 259A9266P16). Both sides of the power source are fused for each output. MOV suppression on NO contact. 1 unfused, associated with relay 12, fed from connector JG1. MOV suppression on NO contact.
WROFH1A Option Board	
Fused Output Circuits	12 fused circuits, one per relay (GE part number 259A9266P16)
WROGH1A Option Board	
Powered Output Circuits	12 fused circuits, one associated with each relay (GE part number 259A9266P16). Single side fusing of the power is associated with the power input on JF1 pin 1. Return power path through JF1pin 3 is not fused.

7.3.5 Diagnostics

The PDIO monitors the following functions on TDBS:

- The contact input wetting voltage is monitored. If the wetting voltage drops to below 40% of the nominal voltage, a diagnostic alarm (fault) is set and latched.
- The TDBS provides diagnostic feedback to PDIO indicating the state of each relay by monitoring an isolated set of contacts on each relay.
- When WROB is used with TDBS isolated voltage feedback is used to detect fuse status for the six fuse pairs on the board.
- When WROF is used with TDBS isolated voltage feedback is used to monitor each fuse. If voltage is present and the fuse is open a diagnostic is generated. The diagnostic may be disabled in PDIO configuration should it be desired to use the feedback circuit with the fuse removed.
- When WROG is used with PDIO isolated voltage feedback is used to monitor each fuse. If voltage is present and the fuse is open a diagnostic is generated.
- The terminal board connector has an ID device that is interrogated by the PDIO. The connector ID is coded into a read-only chip containing the board serial number, board type, and revision number. Any relay option card also contains an ID. If a mismatch is encountered, a hardware incompatibility fault is created.

7.3.6 Configuration

Option board WROBH1 includes six jumpers that are used to apply or remove power from a relay. Boards are produced with all six jumpers in place. The jumper is removed from the board when a relay is to be used as dry contacts and power distribution is not desired.

There are no jumpers associated with the WROFH1 board. For each relay the inclusion or exclusion of a series fuse is determined by the terminal point used as the relay common. For each relay the associated WROF fuse may be removed to allow direct use of the fuse voltage sensing circuit as a voltage detector.

There are no jumpers associated with the WROGH1 board.

There are no jumpers or hardware settings on TDBS.

7.4 TDBT Discrete Input/Output

7.4.1 Functional Description

The Discrete Input/Output (TDBT) terminal board is used for TMR redundancy with either DIN-rail or flat mounting. Three PDIO I/O packs plug into D-type connectors and communicate with the controllers over Ethernet. The TDBT board accepts 24 group-isolated contact inputs that are supplied with a nominal 24, 48, or 125 V dc wetting voltage from an external source. The contact inputs have noise suppression to protect against surge and high-frequency noise. TDBT provides 12 form-C relay outputs and accepts the WROB option board to expand relay functions. All terminal board versions have pluggable terminal blocks.

Three connection points for the PDIO I/O pack are provided. With dual controllers the PDIO on TDBT connector JR1 would be networked to the R controller, JS1 PDIO to the S controller, and JT1 PDIO to both R and S controllers. With TMR controllers one network connection is provided to each PDIO leading to the respective controller. TDBT is not designed to operate correctly with a single PDIO I/O pack.

7.4.1.1 Compatibility

Valid PDIO and TDBT Combinations

Terminal Board	Wetting Voltage
TDBTH2A	Nominal 24 V dc, floating, ranging from 16 to 32 V dc
TDBTH4A	Nominal 48 V dc, floating, ranging from 32 to 60 V dc
TDBTH6A	Nominal 125 V dc, floating, ranging from 100 to 145 V dc
TDBTH8A[1]	Nominal 24 V dc, floating or grounded, ranging from 16 to 31 V dc
[1] This terminal board is specifically designed for use in hazardous locations.	

The WROBH1A is an option board that plugs into TDBTH2A, H4A, or H6A to provide fused and sensed power distribution to the first six relay outputs and dedicated power to the last relay output. The WROFH1A and WROGH1A option boards are not compatible with the TDBT terminal board.

Note When using a WROB with TDBT, the incoming wetting voltage can be either ac or dc.

7.4.2 Installation

Caution

Do not replace a TDBTH2A with TDBSH8A unless having ControlST software suite 4.05 or later.

Warning

TDBSH8A or TDBTH8A terminal boards should not be used with intrinsic safety barriers.

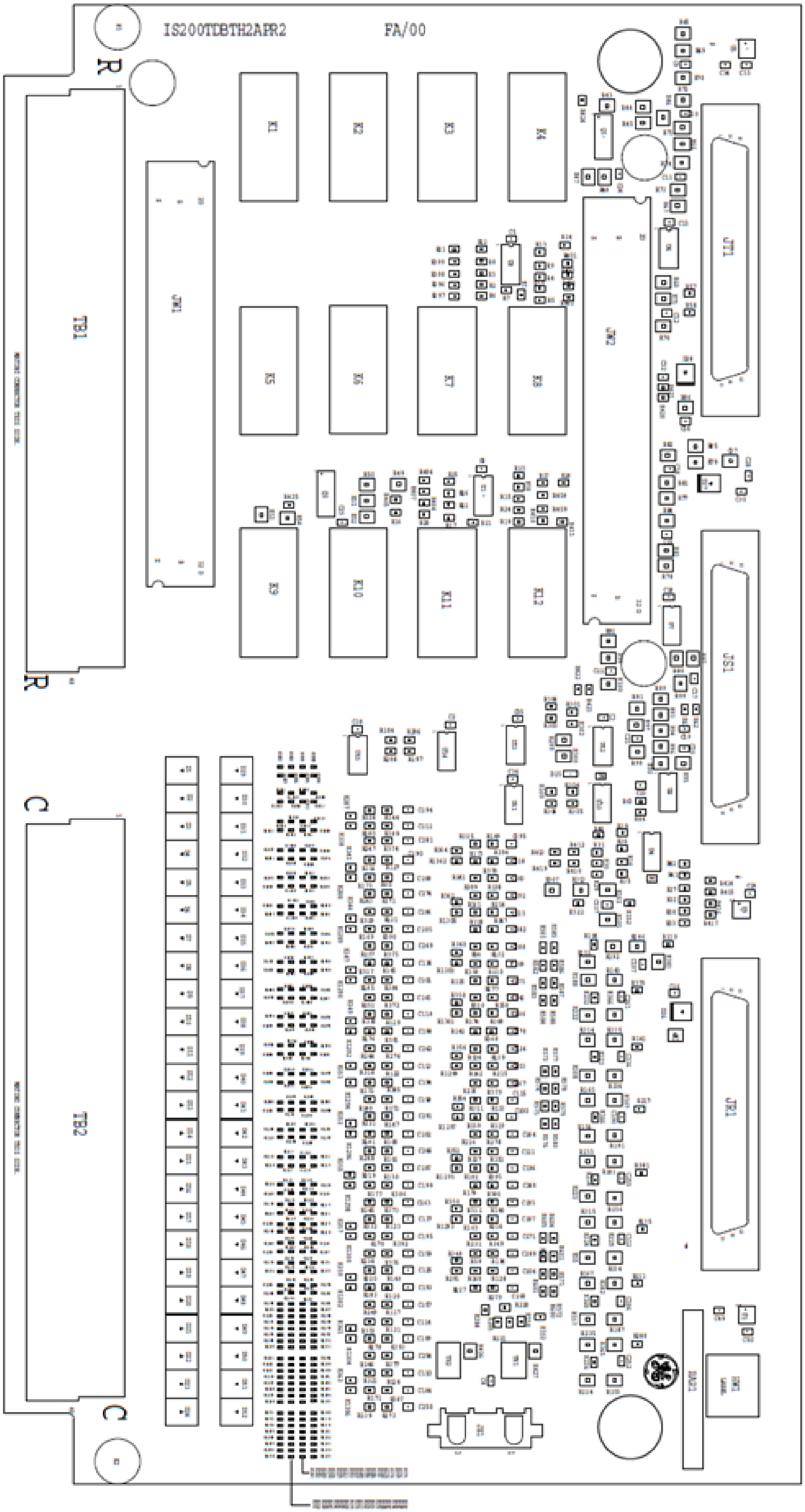
Caution

Discrete output option boards (such as WROBH1A, WROFH1A, or WROGH1A) are not HazLoc certified, and so shall not be used with TDBS or TDBT terminal boards in hazardous (classified) locations.

The TDBT plus a plastic insulator mounts on a sheet metal carrier that then mounts on a DIN rail. Optionally the TDBT plus insulator mounts on a sheet metal assembly that then bolts in a cabinet. The connections are wired directly to two sets of 48 terminal blocks, typically using #24 - #12 AWG wires. The upper set of terminals, TB1, connects to the relay portion of the board and the lower set of terminals, TB2, connect to the contact input circuits. Screw assignments for the two sets of terminals are identical to those found on the SRLY relay board and the STCI contact input terminal board. Shields should be terminated on a separate bracket.

For TDBTH2A, TDBTH4A, and TDBTH6A, the wetting voltage output terminals are all in parallel and fed from the positive voltage applied to JE1 pin 1. It is permissible to run a single wetting voltage lead from the board terminal to a group of remote contacts and then bring the individual contact wires back to the inputs. Negative or return wetting voltage is supplied by JE1 pin 3.

For TDBTH8A, each wetting voltage output terminal is protected by a separate internal current limit resistor. A separate wetting voltage lead must be run for each individual output.


IS200TDBTH2APR2
FA/00
R
R
C
C
TB1
TB2
JW1
JW2
K1
K2
K3
K4
K5
K6
K7
K8
K9
K10
K11
K12
JT1
JS1
JR1

TDBT Layout

7.4.2.1 Relay Outputs

If a relay option board is used, it plugs onto TDBT connectors JW1 and JW2 and is held in place by the force of the connectors. The following table identifies the function of each relay terminal point grouped as TB1 as it relates to the presence of an option board. If external power is to be supplied it is wired to a connector provided on the option board.

TB1 Terminal	Relay	TDBTH2A, 4A, 6A + WROBH1A	TDBT + WROB	TB1 Terminal	Relay	TDBT	TDBTH2A, 4A, 6A + WROBH1A
1	1	NC	NC	25	7	NC	NC
2		COM	COM	26		COM	COM
3		NO	NO	27		NO	NO
4			SOL	28			
5	2	NC	NC	29	8	NC	NC
6		COM	COM	30		COM	COM
7		NO	NO	31		NO	NO
8			SOL	32			
9	3	NC	NC	33	9	NC	NC
10		COM	COM	34		COM	COM
11		NO	NO	35		NO	NO
12			SOL	36			
13	4	NC	NC	37	10	NC	NC
14		COM	COM	38		COM	COM
15		NO	NO	39		NO	NO
16			SOL	40			
17	5	NC	NC	41	11	NC	NC
18		COM	COM	42		COM	COM
19		NO	NO	43		NO	NO
20			SOL	44			
21	6	NC	NC	45	12	NC	NC
22		COM	COM	46		COM	COM
23		NO	NO	47		NO	NO
24			SOL	48			SOL

7.4.2.2 Contact Inputs

Contact input connections are made to the 48 terminals on the lower portion of the terminal board, grouped as TB2. Contact wetting voltage is provided to the board through the JE1 3-pin Mate-N-lok connector on the lower portion of the board.

TB2 Terminal	Signal
1	Wet 1
2	In 1
3	Wet 2
4	In 2
5	Wet 3
6	In 3
7	Wet 4
8	In 4
9	Wet 5
10	In 5
11	Wet 6
12	In 6
13	Wet 7
14	In 7
15	Wet 8
16	In 8
17	Wet 9
18	In 9
19	Wet 10
20	In 10
21	Wet 11
22	In 11
23	Wet 12
24	In 12
25	Wet 13
26	In 13
27	Wet 14
28	In 14
29	Wet 15
30	In 15
31	Wet 16
32	In 16
33	Wet 17
34	In 17
35	Wet 18
36	In 18
37	Wet 19
38	In 19
39	Wet 20
40	In 20
41	Wet 21
42	In 21
43	Wet 22
44	In 22
45	Wet 23
46	In 23
47	Wet 24
48	In 24

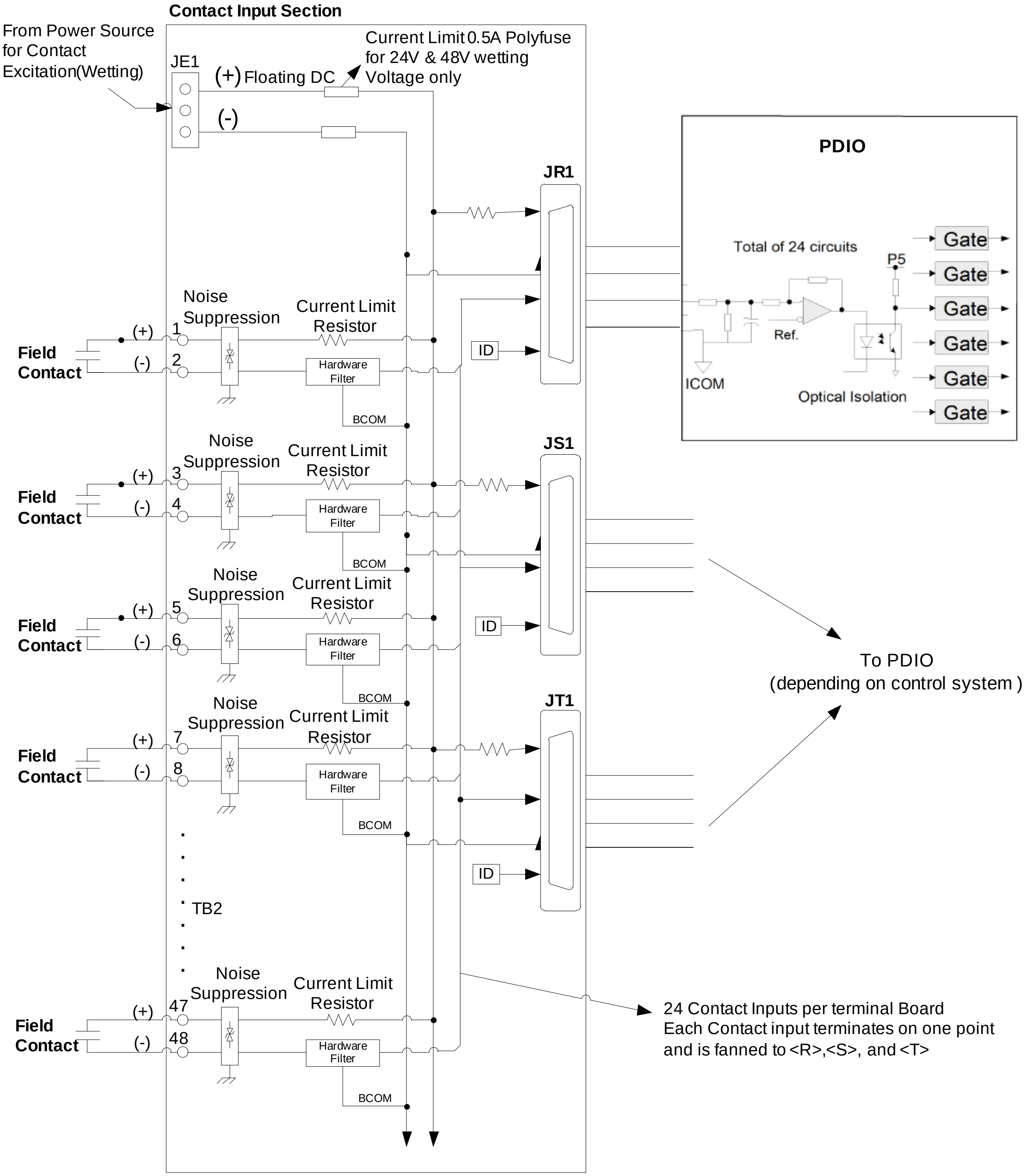
7.4.3 Operation

7.4.3.1 Contact Inputs

The contact input function and on-board signal conditioning are the same as those on STCI, they are scaled for 24, 48, and 125 V dc wetting voltage. The input wetting voltage ranges are listed in the section *Specifications*. The threshold voltage is 50% of the wetting voltage. Contact input currents are resistance limited to 2.5 mA on the first 21 circuits, and 10 mA on circuits 22 through 24. The 24 V dc supply on TDBTH2A is current limited to 0.5 A using polymer positive temperature coefficient fuses that can be reset.

Filters reduce high-frequency noise and suppress surge on each input near the point of signal entry. The discrete input voltage signals go to the I/O processor which passes them through optical isolators, converts them to digital signals, and transfers them to the controller. With TDBTH2A, TDBTH4A, and TDBTH6A terminal boards, wetting voltage output terminals are all connected in parallel and fed from the positive voltage applied to JE1 pin 1. Current limit resistors are omitted.

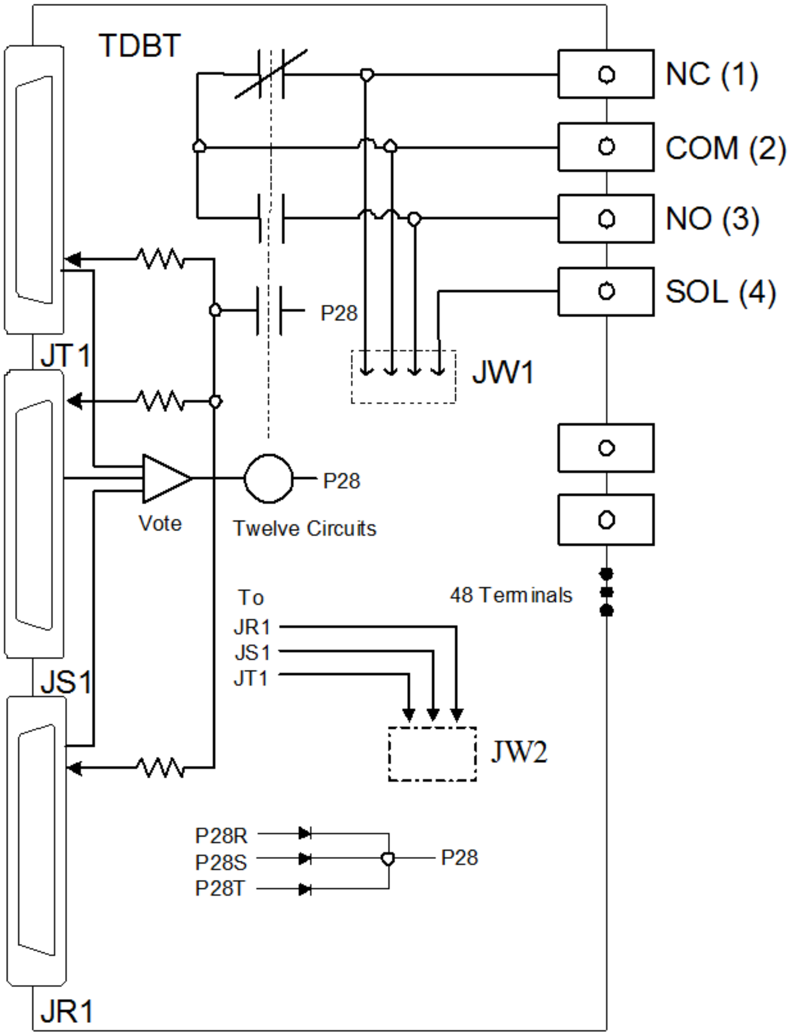
In the following figure, the TDBTH8A contact input section has current limit resistors on each wetting voltage output.


Contact Input Section
From Power Source for Contact Excitation(Wetting)
JE1
(+) Floating DC
(-)
Current Limit 0.5A Polyfuse for 24V & 48V wetting Voltage only
JR1
JS1
JT1
PDIO
Total of 24 circuits
P5
Gate
Gate
Gate
Gate
Gate
Gate
Ref.
ICOM
Optical Isolation
Field Contact
(+)
(-)
1
2
3
4
5
6
7
8
47
48
Noise Suppression
Current Limit Resistor
Hardware Filter
BCOM
ID
TB2
To PDIO (depending on control system)
24 Contact Inputs per terminal Board
Each Contact input terminates on one point and is fanned to <R>,<S>, and <T>

TDBTH8A Contact Inputs

7.4.3.2 Relay Outputs

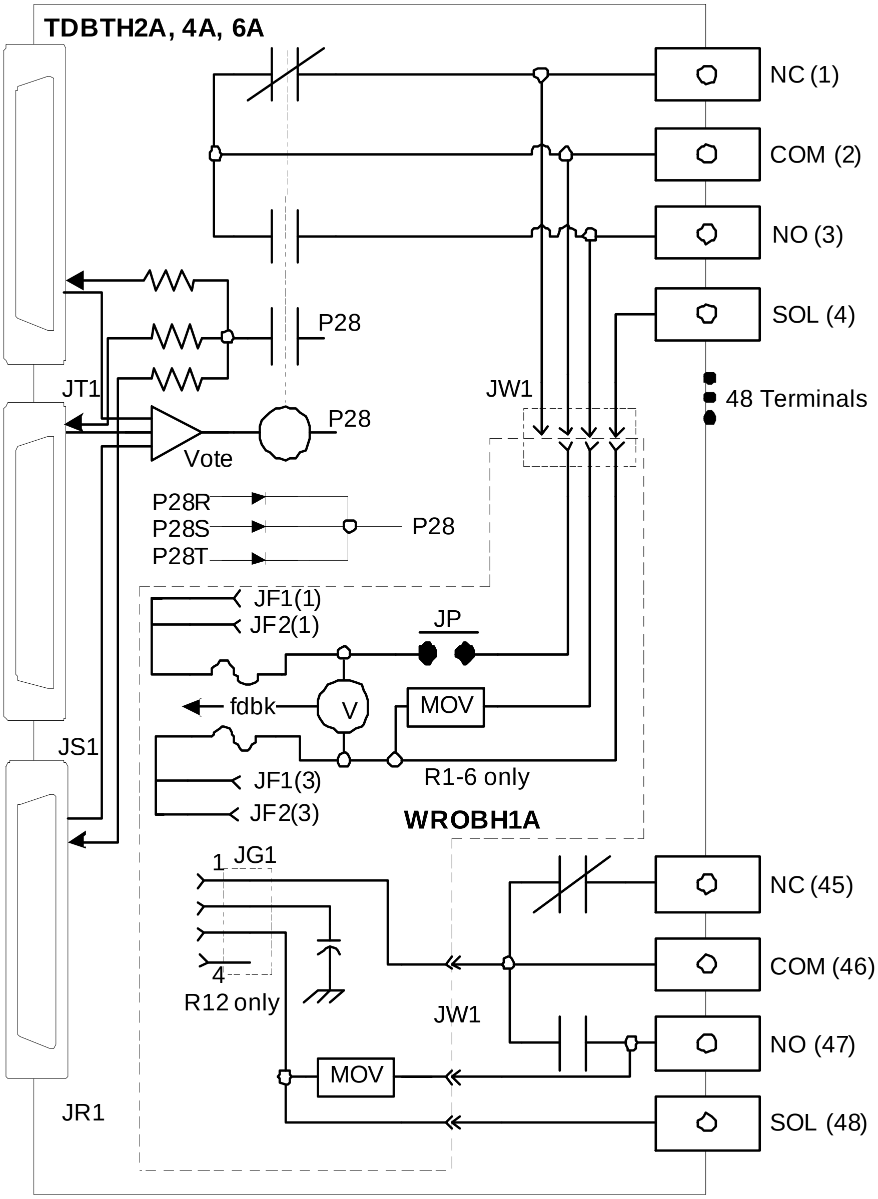
TDBT uses pluggable type terminals and has connectors JW1 and JW2 supporting option board connection. The relay portion of TDBT does not change between groups H2A, H4A, and H6A, only the contact input circuits change. Electrically, TDBT has the following circuit for each of the 12 relays. TDBT relays may be used at any specified ac or dc voltage without regard to board group.



Without an option board, the SOL terminal associated with each relay has no connection. TDBT is designed to support a current rating of 5 A and voltage clearance greater than is needed for 250 V ac on all customer screw and JW1 circuits. The relay contact rating is the limiting item for each application.

7.4.3.3 TDBTH2A, 4A, 6A + WROBH1A

Option board WROBH1A adds capability to TDBTH2A, 4A, 6A to yield a combination that has the same relay circuit functionality as an IS200TRLYH1B terminal board when used in a TMR system. Included are fused sensed power distribution to the first six relay contacts and dedicated power to the last relay contact. Electrically TDBTH2A, 4A, 6A plus WROBH1A has the following circuit. The WROBH1A has a default fuse values of 3.15 A. Connector JW2 and its connections are omitted for clarity.



Both sides of the power distribution on relays 1-6 are fused allowing the board to be used in systems where dc power is floating with respect to earth. Fuse voltage feedback is compatible with 24 V, 48 V, and 125 V dc applications as well as 120 V and 240 V ac applications. The following table lists the relationship between fuses, jumpers, relays, and terminals.

+Fuse	-Fuse	Jumper	Terminals
FU7	FU1	JP1	1-4
FU8	FU2	JP2	5-8
FU9	FU3	JP3	9-12
FU10	FU4	JP4	13-16
FU11	FU5	JP5	17-20
FU12	FU6	JP6	21-24

7.4.4 Specifications

Item	TDBT Specification
Terminal Blocks	Euro Style Box-type Pluggable
Number of Channels	24 dry contact voltage input channels
Wetting Voltage	H2A: Nominal 24 V dc, floating, ranging from 16 to 32 V dc H4A: Nominal 48 V dc, floating, ranging from 32 to 60 V dc H6A: Nominal 125 V dc, floating, ranging from 100 to 145 V dc H8A: Nominal 24 V dc, floating or grounded, ranging from 16 to 31 V dc
Input Current	H2A, H8A: Nominal 24 V dc applications, first 21 circuits draw 2.5 mA, Last three circuits draw 10 mA
	H4A: Nominal 48 V dc applications, first 21 circuits draw 2.5 mA, Last three circuits draw 10.4 mA
	H6A: Nominal 125 V dc applications, first 21 circuits draw 2.55 mA, Last three circuits draw 10 mA
Input Filter	Hardware filter, 4 ms
Fault Detection in I/O Board	Loss of contact input wetting voltage Non-responding contact input in test mode
AC Voltage Rejection	H2A, H8A: 12 V rms at 24 V dc wetting voltage H4A: 24 V rms at 48 V dc wetting voltage H6A: 60 V rms at 125 V dc wetting voltage
Number of Relay Channels on One TDBT	12 relays
Rated Voltage on Relay Contacts	Nominal 24 V dc, 48 V dc, or 125 V dc Nominal 120 V ac or 240 V ac
Max Load Current	0.6 A for 125 V dc operation 1.2 A for 48 V dc operation 3.15 A for 24 V dc operation 3.15 A for 120/240 V ac, 50/60 Hz operation
Max Response Time On	25 ms typical
Max Response Time Off	25 ms typical
Contact Material	Silver-Nickel Alloy
Contact Life	Electrical operations: 100,000 Mechanical operations: 5,000,000
Fault Detection	Relay position feedback using contact pair separate from load contacts.
Size - TDBT	17.8 cm wide x 33.02 cm high (7.0 in x 13.0 in)
Technology	Surface-mount

WROBH1A Option Board

Powered Output Circuits	6 fused, associated with relays 1-6, fed from parallel connectors JF1 and JF2 (GE part number 259A9266P16). Both sides of the power source are fused for each output. MOV suppression across NO relay contact. 1 unfused, associated with relay 12, fed from connector JG1. MOV suppression across NO relay contact.
Compatible Terminal Boards	TDBTH2A, H4A, H6A

7.4.5 Diagnostics

The PDIO monitors the following functions on TDBT:

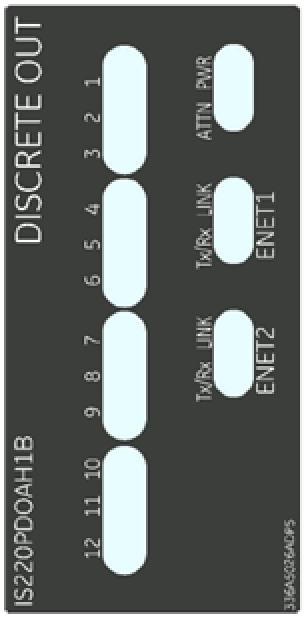
- The contact wetting voltage is monitored. If the wetting voltage drops to below 40% of the nominal voltage, a diagnostic alarm (fault) is set and latched.
- The TDBT provides diagnostic feedback to PDIO indicating the state of each relay by monitoring an isolated set of contacts on each relay. Position feedback is fanned out to all three PDIOs.
- When WROBH1A is used with TDBT isolated voltage feedback is used to detect fuse status for the six fuse pairs on the board. TDBT provides this feedback to all three PDIO packs.
- Each terminal board I/O pack connector has an ID device that is interrogated by the PDIO. The connector ID is coded into a read-only chip containing the board serial number, board type, and revision number. WROB contains three ID devices, one for each PDIO. If a mismatch between I/O pack, terminal board, or option card is encountered, a hardware incompatibility fault is created.

7.4.6 Configuration

Option board WROBH1A includes six jumpers that are used to apply or remove power from a relay. Boards are produced with all six jumpers in place. The jumper is removed from the board when a relay is to be used as dry contacts and power distribution is not desired. There are no jumpers or hardware settings on the TDBT terminal board.

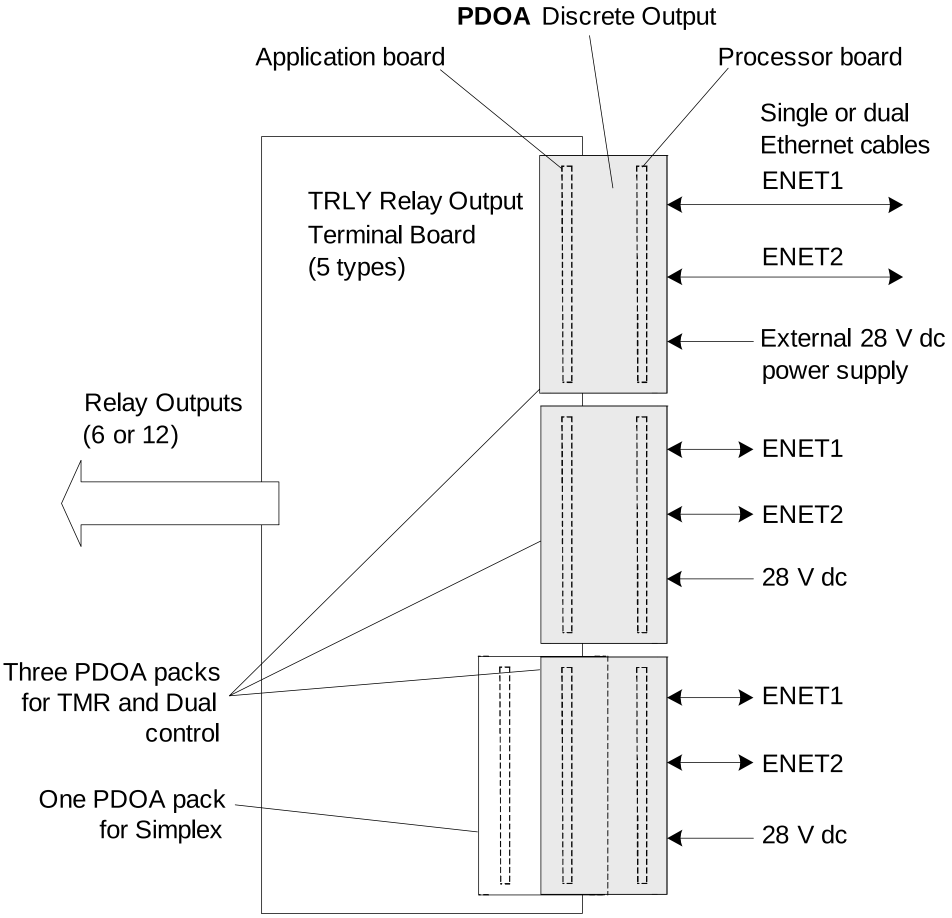
8 PDOA, YDOA Discrete Output Modules

8.1 Mark VIe PDOA Discrete Output Pack



The Discrete Output (PDOA) I/O pack provides the electrical interface between one or two I/O Ethernet networks and a discrete output terminal board. The I/O pack contains a *BPPx* processor board and an acquisition board specific to the discrete output function. The PDOA is capable of controlling up to 12 relays and accepts terminal board specific feedback. Electromagnetic relays (with types TRLYH1B, C, D, and F terminal boards) and solid-state relays (with type TRLYH#E boards) are available.

A 3-pin input is used for external 28 V dc power. Dual RJ-45 Ethernet connectors are provided for an interface to the IONet. The DC-37 pin connector provides an interface to the associated terminal board. Visual diagnostics are provided through indicator LEDs.


PDOA Discrete Output
Application board
Processor board
Single or dual Ethernet cables
ENET1
ENET2
External 28 V dc power supply
TRLY Relay Output Terminal Board (5 types)
Relay Outputs (6 or 12)
ENET1
ENET2
28 V dc
Three PDOA packs for TMR and Dual control
One PDOA pack for Simplex
ENET1
ENET2
28 V dc

8.1.1 Compatibility

The PDOA includes one of the following compatible BPPx processor boards.

- The PDOAH1A contains a BPPB processor board.
- The PDOAH1B contains a functionally compatible BPPC that is supported in the ControlST* software suite V04.04 and later.

The PDOA is compatible with the following discrete (relay) output terminal boards, including the TRLY boards and SRLY boards, but not the DIN-rail mounted DRLY boards.

Terminal Board	Simplex [1]	TMR [2]
TRLYH1B, S1B	Yes	Yes
TRLYH1C		
TRLYH2C		
TRLYH1D, S1D		
TRLYH1E TRLYH2E TRLYH3E		
TRLYH1F, S1F TRLYH2F, S2F	No	Yes
SRLYH1A, S1A SRLYH2A, S2A	Yes	No
[1] Simplex uses one I/O pack with one or two network connections. [2] TMR uses three I/O packs with one network connection on each pack.		

8.1.2 Installation

➢ **To install the PDOA I/O pack**

1. Securely mount the desired terminal board.
2. Directly plug the PDOA I/O pack into the terminal board connectors.
3. Mechanically secure the I/O pack(s) using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right-angle force applied to the DC–37 connector between the pack and the terminal board. The adjustment should only be required once in the service life of the product.

Note The PDOA mounts directly onto a terminal board. Simplex terminal boards have a single DC-37 connector that receives the PDOA. TMR-capable terminal boards have four DC-37 connectors, one used for simplex operation and three used for TMR operation. PDOA directly supports all of these connections.

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4. Plug in one or two Ethernet cables depending on the system configuration. The I/O pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
5. Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to remove power from the cable before plugging it in because the I/O pack has inherent soft-start capability that controls current inrush on power application.
6. Use the ToolboxST* application to configure the I/O pack as necessary. From the Component Editor, press F1 for help.

Note From the ToolboxST application, PDOA module add/modify dialog box, the drop down labeled *I/O Module Trip From* should be left blank unless the PDOA is used with a PGEN I/O pack to perform the power load unbalance (PLU) function.

8.1.2.1 Connectors

- The DC-37 pin connector on the underside of the I/O pack connects directly to a discrete output terminal board.
- The RJ-45 Ethernet connector (ENET1) on the I/O pack side is the primary system interface.
- The second RJ-45 Ethernet connector (ENET2) on the I/O pack side is the redundant or secondary system interface.

Note The terminal board provides fused power output from a power source that is applied directly to the terminal board, not through the I/O pack connector.

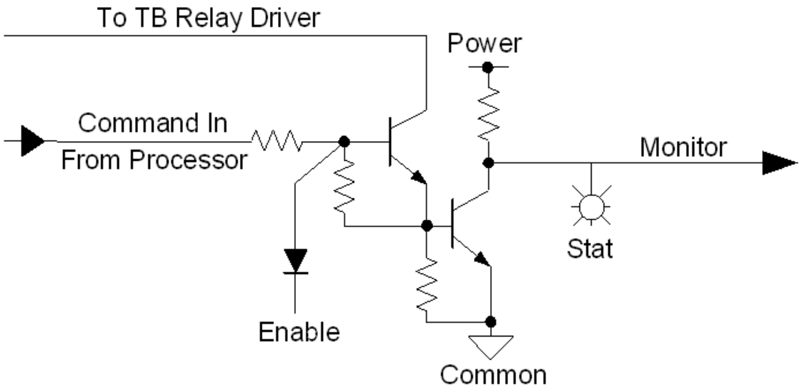
8.1.3 Operation

The following features are common to the distributed I/O modules:

- *BPPx Processor*
- *Processor LEDs*
- *Power Management*
- *ID Line*
- *I/O Module Common Diagnostic Alarms*

8.1.3.1 Relay Command Signals

The PDOA relay command signals are the first stage of signal conditioning and level shifting to interface the terminal board outputs to the control logic. Each output is an open collector transistor circuit with a current monitor to sense when the output is picked up and connected to a load. The status LEDs and monitor outputs indicate when an output is picked up and connected to the terminal board. If an output is picked up and the correct load is not sensed, the status LED will be off and the monitor line will be false.



8.1.3.2 Output Enable

All of the outputs are disabled during power application until a variety of internal self-tests are completed. An enable line reflects the status of all required conditions for operation. This function provides a path independent of the command to ensure relays stay dropped-out during power-up and initialization.

8.1.3.3 Monitor Inputs/Control

There are 15 inverting level shifting monitor input circuits. On a typical TRLY terminal board 12 of these circuits are used as relay contact feedbacks and the other three are used for fuse status. An inverting level shifting line is also provided from the control to the terminal board for status feedback multiplexing control allowing the pack to receive two sets of 15 signals from a terminal board.

8.1.3.4 Sequence of Events (SOE)

Outputs may be individually configured to generate SOE records when the signal changes. It is not recommended to use output SOEs, but to instead use output feedback inputs (for example, relay feedback to log the relay SOEs). Output commands are captured when a change of command is received through Ethernet from the controller.

8.1.3.5 Power Load Unbalance (PLU)

This function is used by GE. Refer to GEH-6721_Vol_III for GE Industrial Applications.

8.1.4 Specifications

Item	PDOA Specification
Number of Relay Channels in One PDOA I/O Pack	12 relays (different types depending on the terminal board)
Relay and Coil Monitoring	12 relay/coil monitors, 3 fuse status feedbacks muxed to read status from 6 fuses
I/O Pack Response Time	From Ethernet command to output is approximately in 6 ms
SOE Reporting	Each relay may be configured to report operation in the Sequence of Events (SOE) record
Size	8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in x 1.65 in x 4.78 in)
Technology	Surface-mount
Ambient Rating for Enclosure Design†	PDOAH1B is rated from -40 to 70°C (-40 to 158 °F) PDOAH1A is rated from -30 to 65°C (-22 to 149 °F)

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

8.1.5 Diagnostics

The I/O pack performs the following self-diagnostic tests:

- A power on self-test that includes checks of RAM, flash memory, Ethernet ports, and processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set
- A comparison is made between the commanded state of each relay drive and the feedback from the command output circuit.
- Relay board specific feedback is read by the pack and processed. The information varies depending on the relay board type.
- If the PDOA has been configured for the power load unbalance (PLU) function (used by GE Industrial applications).

Details of the individual diagnostics are available in the ToolboxST application. The diagnostic signals can be individually latched, and then reset with the RSTDIAG signal if they go healthy.

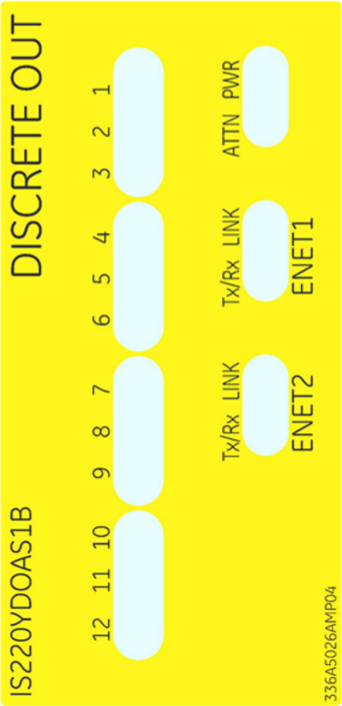
8.1.5.1 PDOA Status LEDs

Output LEDs

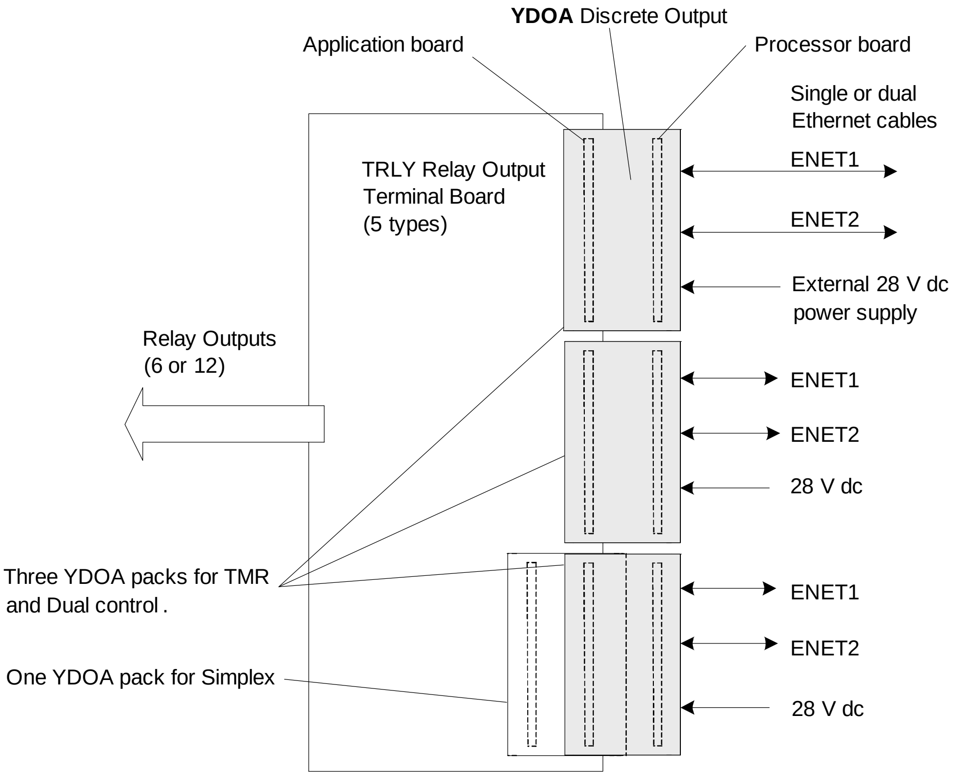
Color	I/O Pack Label	Description
Yellow	1 – 12	Provided for each output to indicate the presence of a command to energize the relay

Note Refer to the Common Module, Processor LEDs section.

8.2 Mark VIeS YDOA Discrete Output Pack



The Discrete Output (YDOA) pack provides the electrical interface between one or two I/O Ethernet networks and a discrete output terminal board. The pack contains a common processor board and an acquisition board specific to the discrete output function. The YDOA is capable of controlling up to 12 relays and accepts terminal board specific feedback. Electromagnetic relays (with types TRLYS1B, D, and F terminal boards) are available. Input to the pack is through dual RJ-45 Ethernet connectors and a three-pin power input. Output is through a DC-37 pin connector that connects directly with the associated terminal board connector. Visual diagnostics are provided through indicator LEDs.



8.2.1 YDOA Compatibility

The YDIA I/O pack contains an internal processor board. The following table lists the available versions of the YDOA.

YDOA Version Compatibility

I/O Pack	Processor Board	Compatible (Supported) Firmware	ControlST Software Suite Versions
YDOAS1A	BPPB	V04.11	Supported in V05.04 and all later versions
YDOAS1B	BPPC	V05.00 and later	Supported in V06.01 and later versions

Attention

YDOAS1A and YDOAS1B I/O pack versions cannot be mixed on the same T-type terminal board.

All three YDOA I/O packs in a TMR set must be the same hardware form.

To upgrade or replace the YDOA, refer to the following replacement procedures for specific instructions:

- *Replace Mark VIeS Safety I/O Pack with Same Hardware Form*
- *Replace Mark VIeS Safety I/O Pack with Upgraded Hardware Form*

YDOA is compatible with several types of discrete (relay) output terminal boards.

YDOA Terminal Board Compatibility

Terminal Board	Description	I/O Pack Redundancy		
		Simplex	Dual	TMR
TRLYS1B	Relay output with coil sensing	Yes	No	Yes
TRLYS1D	Relay output with solenoid integrity sensing	Yes	No	Yes
TRLYS1F, S2F	Relay output with TMR contact voting	No	No	Yes
SRLYS1A, S2A	Form C contact relays	Yes	No	No
SRSAS1A, S3A	Compact size with normally open relays For hardware availability, contact the nearest GE Sales or Service Office, or an authorized GE Sales Representative. Compatible with YDOAS1B firmware V05.00 or later Compatible with the YDOAS1A firmware V04.11	Yes	No	Yes

I/O pack redundancy refers to the number of I/O packs used in a signal path, as follows:

- Simplex uses one I/O pack.
- TMR uses three I/O packs.

8.2.2 YDOA Installation

➢ **To install the YDOA pack**

1. Securely mount the desired terminal board.
2. Directly plug one YDOA for simplex or three YDOAs for TMR into the terminal board connectors.
3. Mechanically secure the packs using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right-angle force applied to the DC-37 connector between the pack and the terminal board. The adjustment should only be required once in the life of the product.
4. Plug in one or two Ethernet cables depending on the system configuration. The I/O pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
5. Apply power to the pack by plugging in the connector on the side of the I/O pack. It is not necessary to insert this connector with the power removed from the cable as the YDOA has inherent soft-start capability that controls current inrush on power application.
6. Use the ToolboxST application to configure the YDOA as necessary.

8.2.2.1 Connectors

- A DC-37 pin connector on the underside of the YDOA connects directly to a discrete output terminal board.
- An RJ-45 Ethernet connector named ENET1 on the pack side is the primary system interface.
- A second RJ-45 Ethernet connector named ENET2 on the pack side is the redundant or secondary system interface.
- A 3-pin power connector on the pack side is the input point for 28 V dc power for the pack and terminal board.

Note The terminal board provides fused power output from a power source that is applied directly to the terminal board, not through this pack connector.

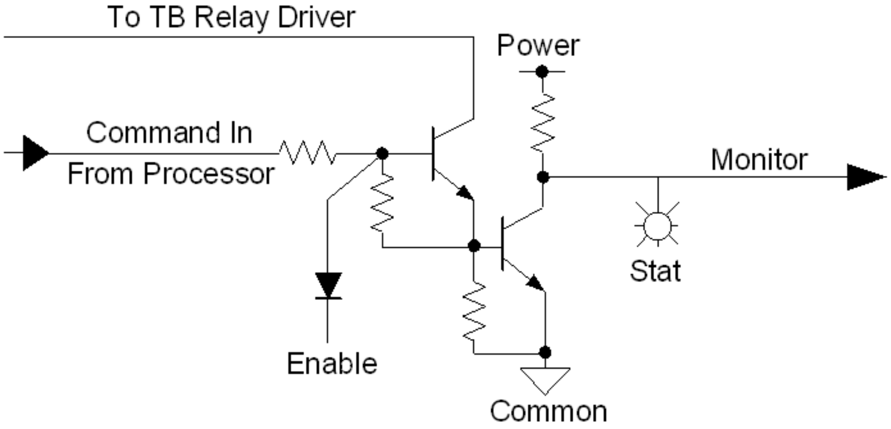
8.2.3 YDOA Operation

The following features are common to the safety I/O modules:

- *BPPx Processor Board*
- *Processor LEDs*
- *I/O Module Common Diagnostic Alarms*

8.2.3.1 Relay Command Signals

The YDOA relay command signals are the first stage of signal conditioning and level shifting to interface the terminal board outputs to the control logic. Each output is an open collector transistor circuit with a current monitor to sense when the output is picked up and connected to a load. The status LEDs and monitor outputs indicate when an output is picked up and connected to the terminal board. If an output is picked up and the correct load is not sensed, the status LED will be off and the monitor line will be false.



8.2.3.2 Output Enable

All of the outputs are disabled during power application until a variety of internal self-tests is completed. An enable line reflects the status of all required conditions for operation. This function provides a path independent of the command to ensure relays stay dropped-out during power-up and initialization.

8.2.3.3 Monitor Inputs/Control

There are 15 inverting level shifting monitor input circuits. On a typical TRLY terminal board, 12 of these circuits are used as relay contact feedbacks and the other three are used for fuse status. An inverting level shifting line is also provided from the control to the terminal board for status feedback multiplexing control allowing the pack to receive two sets of 15 signals from a terminal board.

8.2.4 Specifications

Item	YDOA Specification
Number of Relay Channels	12 relays (different types depending on the terminal board)
Relay and Coil Monitoring	12 relay/coil monitors, 3–fuse status feedbacks are multiplexed to read status from six fuses
I/O Pack Response Time	From Ethernet command to output is approximately 6 ms
SOE Reporting	Each relay can be configured to report operation in the Sequence of Events (SOE) record
Size	8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in x 1.65 in x 4.78 in)
Technology	Surface-mount
Ambient Rating for Enclosure Design†	-30 to 65°C (-22 to 149 °F)

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

8.2.5 YDOA Diagnostics

The I/O pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and processor board hardware
- Continuous monitoring of the internal power supplies for correct operation

- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set.
- A comparison is made between the commanded state of each relay drive and the feedback from the command output circuit.
- Relay board specific feedback is read by the pack and processed. The information varies depending on the relay board type. Refer to relay terminal board documentation for feedback specifics.

Details of the individual diagnostics are available in the ToolboxST application. The diagnostic signals can be individually latched, and then reset with the RSTDIAG signal if they go healthy.

8.2.5.1 YDOA Status LEDs

Output LEDs

Color	I/O Pack Label	Description
Yellow	1 – 12	Provided for each output to indicate the presence of a command to energize the relay

---

Note Refer to the Common Module, *Processor LEDs* section.

8.3 PDOA or YDOA Configuration

8.3.1 Inputs

Parameter	Description	Select Option or Enter Value
ContactInput	Enables Relay#Fdbk	Unused, Used
SignalInvert	Inverts Relay#Fdbk signal and Relay#ContactFdbk signal (if available) **Do not rely on the SignalInvert property of digital inputs to invert the value. Implement this operation in the application code with the input connected to a NOT block.**	Normal, Invert
SeqOfEvents	Record RelayFdbk transitions in sequence of events Not available with TRLY#D.	Disable, Enable
DiagVoteEnab	Enable voting disagreement diagnostic	Disable, Enable
SignalFilter	Relay feedback digital filter in milliseconds, is only available with TRLYH#C (not available for safety use)	Zero, Ten, Twenty, Fifty, Hundred

8.3.2 Outputs

Parameter	Description	Select Option or Enter Value
RelayOutput	Enable relay output	Used, Unused
SignalInvert	Inversion makes relay closed if signal is false **Do not rely on the SignalInvert property of digital inputs to invert the value. Implement this operation in the application code with the input connected to a NOT block.**	Normal, Invert
SeqOfEvents	Record relay command transitions in sequence of events	Disable, Enable
FuseDiag	Enable fuse diagnostic (if available)	Enable, Disable
Output_State	Select the state of the relay condition based on I/O pack going offline with controller	PwrDownMode, HoldLastValue, Output_Value
Output_Value	Pre-determined value for the outputs (only displayed if Output_State is set to Output_Value)	Off, On

8.3.3 Variables

Name	Description	Direction	Type
L3DIAG_PDOA_x L3DIAG_YDOA_x	I/O diagnostic indication, where x = R, S, or T	Input	BOOL
LINK_OK_PDOA_x LINK_OK_YDOA_x	I/O link okay indication, where x = R, S, or T	Input	BIT
ATTN_PDOA_x ATTN_YDOA_x	I/O Attention Indication, where x = R, S, or T	Input	BIT
IOPackTmpr_x	I/O pack temperature, where x = R, S, or T	Input	REAL
†Cap1_Ready_x	I/O pack capture buffer 1 ready for upload (currently not used), where x = R, S, or T	Input	BIT
†Cap2_Ready_x	I/O pack capture buffer 2 ready for upload (currently not used), where x = R, S, or T	Input	BIT
†CV_Permissive	CV (control valve) permissive for PGEN PLU function	Input	BIT
†IV_Permissive	IV (intercept valve) permissive for PGEN PLU function	Input	BIT
† Not applicable to YDOA			

Name	Description	Direction	Type
Relay#	Relay# output command	Output	BIT
Relay#Fdbk	Relay# Driver Status (set of 12 relays)	Input	BIT
Relay#ContactFdbk	Relay# Contact Status (set of 12 relays), available for TRLY#C, TRLY#E, SRSA, and SRLY only	Input	BIT
Fuse#Fdbk	Fuse voltage (if available)	Input	BIT
Solenoid#Status	Solenoid# Resistance Sense (set of 6 relays), True means resistance within the range, False means resistance out of the range, available for TRLY#D only	Input	BIT

8.4 PDOA or YDOA Specific Alarms

The following alarms are specific to the PDOA or YDOA I/O pack.

33-129

Description Logic Signal [ ] Voting Mismatch

Possible Cause In a TMR application, the values for the specified signal do not agree between R, S, and T I/O packs.

Solution

- Verify that R, S, and T I/O pack configurations are equal to ToolboxST configuration.
- Check the I/O pack power and networking.
- Check the I/O pack mounting on terminal board.
- Replace the I/O pack.

130-141

Description Relay circuit [ ] fuse(s) blown

Possible Cause The PDOA I/O pack fuse status feedback indicates a possible blown fuse.

Solution Perform the following items in the following order:

- Using the following fuse table, *Terminal Board Fuses*, check the fuse(s) in the appropriate terminal board for a possible blown fuse.
- Verify the contact wetting/input power to the terminal board.
- Verify the terminal board configuration and jumper settings (on TRLYH1B, S1B, or WROBH1A).
- Verify that the I/O pack output and fuse diagnostics are enabled properly in the ToolboxST configuration.
- Confirm that all connectors, power plugs, I/O packs, and daughterboards are fully seated.
- If the problem persists, perform the following:
  - Replace the I/O pack.
  - Replace the WROB, F, or G daughterboard or the WPDF daughterboard.
  - Replace the terminal board. (This requires a ToolboxST configuration Build and Download to update the terminal board serial number.)

Terminal Board Fuses

Relay Output Circuit #	TRLYH1-B/S1B	TRLYH#C	TRLYH1D/-S1D	TRLYH#F/-S#F with WPDF	SRLY_2A with WROB	SRLY_2A with WROF	SRLY_2A with WROG
1	FU1 FU7	FU1 FU7	FU1 FU7	FU1 FU13	FU1 FU7	FU1	FU1
2	FU2 FU8	FU2 FU8	FU2 FU8	FU2 FU14	FU2 FU8	FU2	FU2
3	FU3 FU9	FU3 FU9	FU3 FU9	FU3 FU15	FU3 FU9	FU3	FU3
4	FU4 FU10	FU4 FU10	FU4 FU10	FU4 FU16	FU4 FU10	FU4	FU4
5	FU5 FU11	FU5 FU11	FU5 FU11	FU5 FU17	FU5 FU11	FU5	FU5
6	FU6 FU12	FU6 FU12	FU6 FU12	FU6 FU18	FU6 FU12	FU6	FU6
7	Not fused	Not fused	N/A	FU7 FU19	Not fused	FU7	FU7
8	Not fused	Not fused	N/A	FU8 FU20	Not fused	FU8	FU8
9	Not fused	Not fused	N/A	FU9 FU21	Not fused	FU9	FU9
10	Not fused	Not fused	N/A	FU10 FU22	Not fused	FU10	FU10
11	Not fused	Not fused	N/A	FU11 FU23	Not fused	FU11	FU11
12	Not fused	Not fused	N/A	FU12 FU24	Not fused	FU12	FU12

142

Description All fuses blown or no terminal board excitation

Possible Cause If fuse sensing indicates an open fuse, this may be due to loss of input power to the terminal board. Without power to the fuses, the sensing may indicate a false open-fuse condition.

Solution

- Confirm the correct input power to the terminal board.
- Check the I/O pack connector alignment and seating.
- Check the I/O pack configuration.
- Check all fuses.
- Replace the I/O pack.
- Replace the terminal board.

143-154

Description Relay Output Coil [ ] does not match commanded state

Possible Cause

- The relay feedback does not match the commanded state for TRLY__B, TRLY__F, or SRLY, or SRSA specific terminal boards.
- SRSA: The mechanical relay (1 or 7) is not picked up when the relay (2-6 or 8-12) is closed.
- SRSA: Wetting power A (relays 2-6) or B (relays 8-12) is not applied.
- SRSA: Relay is picked up but no current (minimum 100 mA) is flowing through the relay circuit.

Solution

- Clear the voter disagreements.
- Check the I/O pack connector alignment and seating.
- Check the I/O pack configuration.
- SRSA: Pick up the mechanical relay before closing the solid state relays.
- SRSA: Verify that the wetting power bank A and B have voltage applied.
- SRSA: Verify that a proper output circuit is connected to the relay.
- Replace the terminal board.

155-166

Description NO [Normally Open] contact [ ] voltage disagreement with command

Possible Cause Voltage is not detected across an open TRLY__C or TRLY__E output contact.

Solution

- Clear the voter disagreements.
- Check the application to ensure that voltage should be present when relay is open.
- Check that the voltage is within the published detection range. Refer to the terminal board help documentation.
- Check the I/O pack configuration.
- Replace the terminal board.

167-178

Description Relay Driver [ ] does not match commanded state

Possible Cause The relay command signal, displayed at the I/O pack output connector to the terminal board, does not match the commanded state.

Solution The command signal feedback requires a properly connected terminal board.

- Check the I/O pack to terminal board connector alignment and seating.
- Replace the I/O pack.
- Replace the terminal board.

179-184

Description Relay [ ] connected field device impedance outside of acceptable range

Possible Cause A connected load does not fall within published impedance limits for TRLY__D-specific terminal boards.

Solution

- Clear the voter disagreements.
- Check for field wiring open or short circuits.
- Check the attached load to ensure that impedance is within the published limits for TRLY__D. Refer to the terminal board help documentation.
- Check TRLY input power.
- Replace TRLY__D.

191

Description Config Mismatch: TRLY__F terminal board is configured for SIMPLEX redundancy

Possible Cause The TRLY__F board is connected to an I/O pack that is configured as simplex. Due to the redundant nature of the TRLY__F terminal board, a TMR I/O pack module configuration is required.

Solution From the ToolboxST application, configure the I/O pack redundancy as TMR. Build and download a new configuration.

192

Description Peer to Peer Communication Failure Code [ ]

Possible Cause PGEN peer-to-peer communication for the PLU function has been lost. Refer to the PGEN documentation for a description of peer-to-peer communication.

Solution

- From the ToolboxST application, select *None* for **I/O Module Trip From** as the source for a trip if the PLU function is not used. Build and download the parameters.
- If a PGEN is used as a source for **I/O Module Trip From** then check the online status of the PGEN, and correct this if it is not online.
- If other communication diagnostic alarms are active, check for issues with network cables, switches, and such.

194

Description Peer to Peer Communication Compatibility mismatch: PDOA [ ], Received Message [ ]

Possible Cause The firmware revision of PGEN used for the source of the PLU trip is not compatible with the PDOA firmware revision.

Solution Upgrade the PGEN and PDOA to the latest firmware revision with the ControlST software suite, and download the firmware and parameters to both I/O packs.

195

Description Peer to Peer Communication Initialization failure

Possible Cause The peer-to-peer link with PGEN for the PLU function could not be initialized.

Solution From the ToolboxST application, build and download parameters to the PDOA and PGEN that are used for the PLU function.

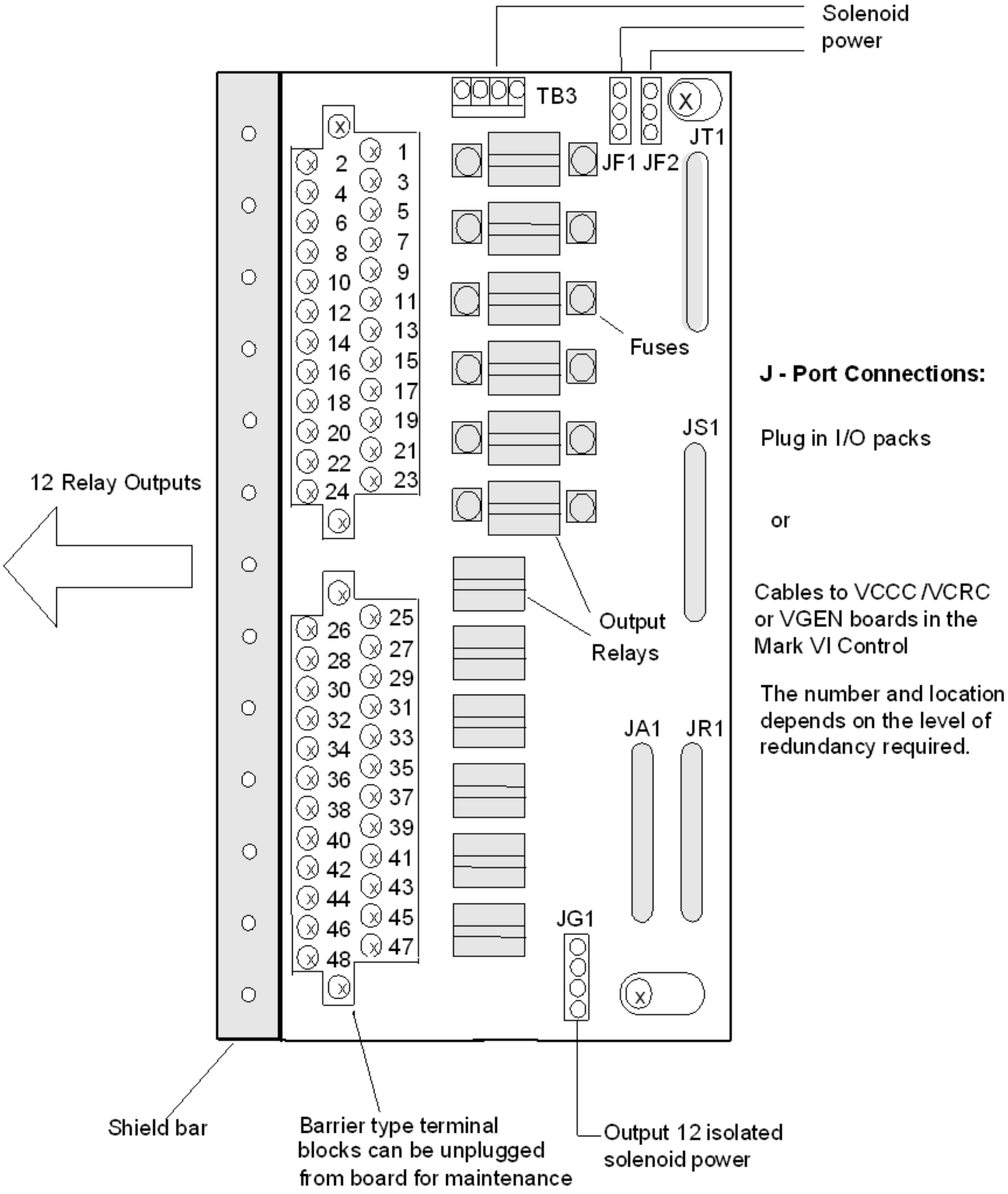
8.5 TRLY Discrete Output Terminal Boards

The following TRLY discrete output terminal boards work with the PDOA or YDOA I/O pack.

- *TRLY_1B Relay Output with Coil Sensing*
- *TRLYH#C Relay Output with Contact Sensing*
- *TRLYH_1D Relay Output with Solenoid Integrity Sensing*
- *TRLYH#E Solid-sate Relay Output*
- *TRLY_1F, 2F Relay Output with TMR Contact Voting*

8.6 TRLYH1B, S1B Relay Output with Coil Sensing

The Relay Output with coil sensing (TRLY_1B) terminal board holds 12 plug-in magnetic relays. The first six relay circuits configured by jumpers for either dry, Form-C contact outputs, or to drive external solenoids. A standard 125 V dc or 115/230 V ac source, or an optional 24 V dc source with individual jumper selectable fuses and on-board suppression, can be provided for field solenoid power. The next five relays (7-11) are unpowered isolated Form-C contacts. Output 12 is an isolated Form-C contact, used for special applications such as ignition transformers.



TRLY_1B Relay Output Terminal Board

8.6.1 TRLY_1B Compatibility

The terminal board supports simplex and TMR applications. The I/O pack plugs into the DC-37 pin connectors on the terminal board. Connector JA1 is used on simplex, and connectors JR1, JS1, and JT1 are used for TMR.

Board Revision	Mark VIe Control IS220PDOA	Mark VIeS Safety Control IS220YDOA	Comments
TRLYH1B	Yes, all versions	No	
TRLYS1B	Yes, all versions	Yes, all versions	IEC 61508 safety certified with Mark VIeS YDOA.

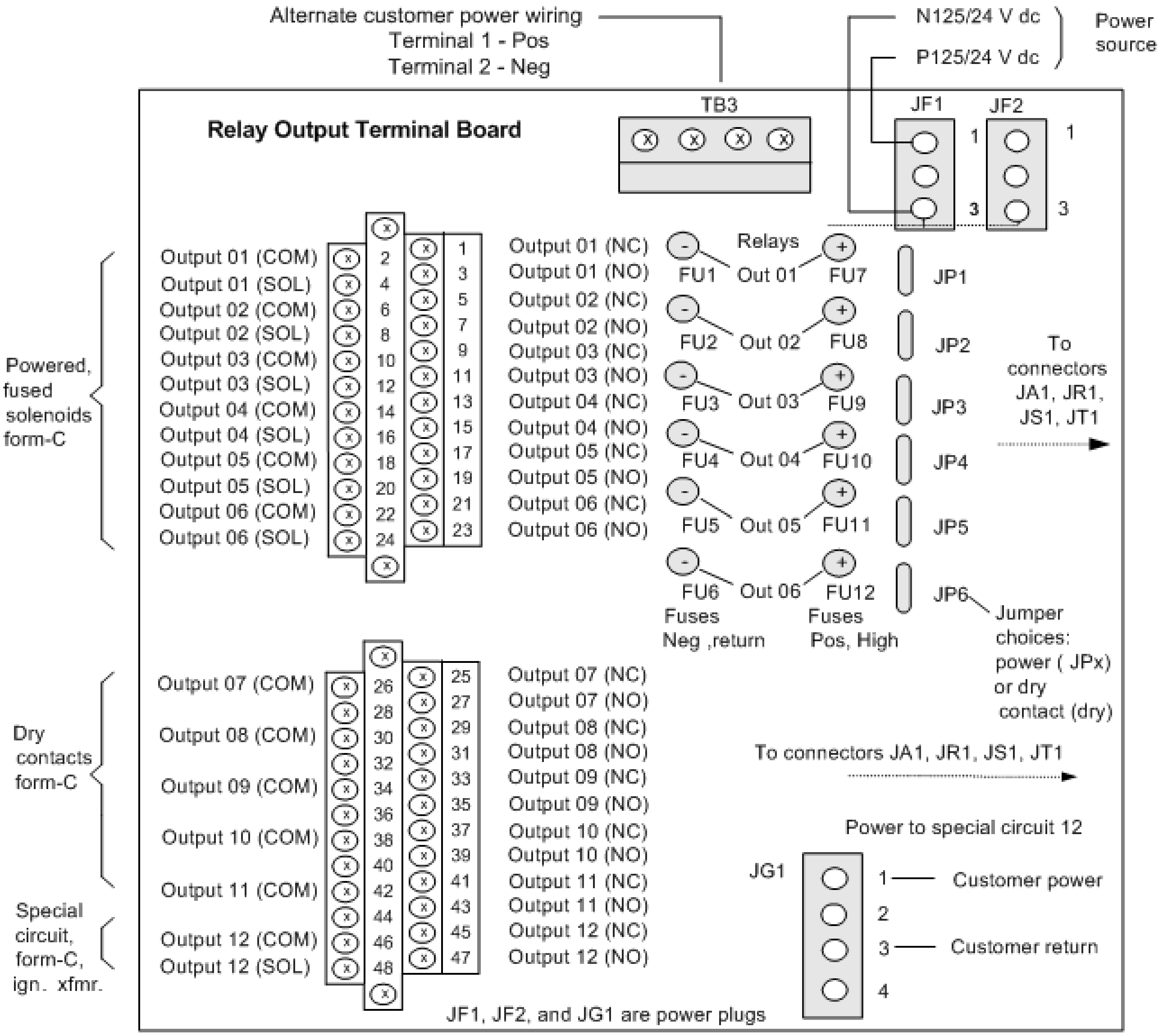
8.6.2 TRLY_1B Installation

Connect the wires for the 12 relay outputs directly to two I/O terminal blocks on the terminal board. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield terminal strip attached to chassis ground is located on to the left side of each terminal block.

Connect the solenoid power for outputs 1-6 to JF1. JF2 can be used to daisy chain power to other TRLYs. Alternatively, power can be wired directly to TB3 when JF1/JF2 are not used. Connect power for the special solenoid, Output 12, to connector JG1.

Note These jumpers are also for isolation of the monitor circuit when used on isolated contact applications.

Jumpers JP1-JP6 are supplied with the board. The appropriate jumper should be installed if power to a field solenoid is required. Conduct individual loop energization checks as per standard practices and install the jumpers as required. For isolated contact applications, remove the fuses to ensure that suppression leakage is removed from the power bus. If both the jumpers and the fuses are not removed, external power will be connected to the suppression circuits in some operating conditions.



TRLY_1B Terminal Board Wiring

8.6.3 TRLY_1B Operation with Multiple Power Sources

8.6.3.1 Dry Contacts

When these terminal boards are used as dry contacts to switch ac voltage using circuits 01 through 06, and are simultaneously supplied with 125 V dc power through JF1, JF2, or TB3, unless all the fuses and JPx jumpers for the relay contact being used as a dry contact with a separate supply are removed, the separate supply will be present on the Normally Open (NO) relay terminal. If the JPx jumpers and fuses for the ac powered dry contact are not correctly removed, it will tie the ac voltage to N 125 V dc when the contact closes. A similar situation exists for the P-125. Since most ac supplies operate with a grounded neutral, the sum of the ac peak voltage and the 125 V dc is applied to MOVs connected between the dc and ground. In 120 V ac applications, the MOV rating is sufficient to withstand that voltage.

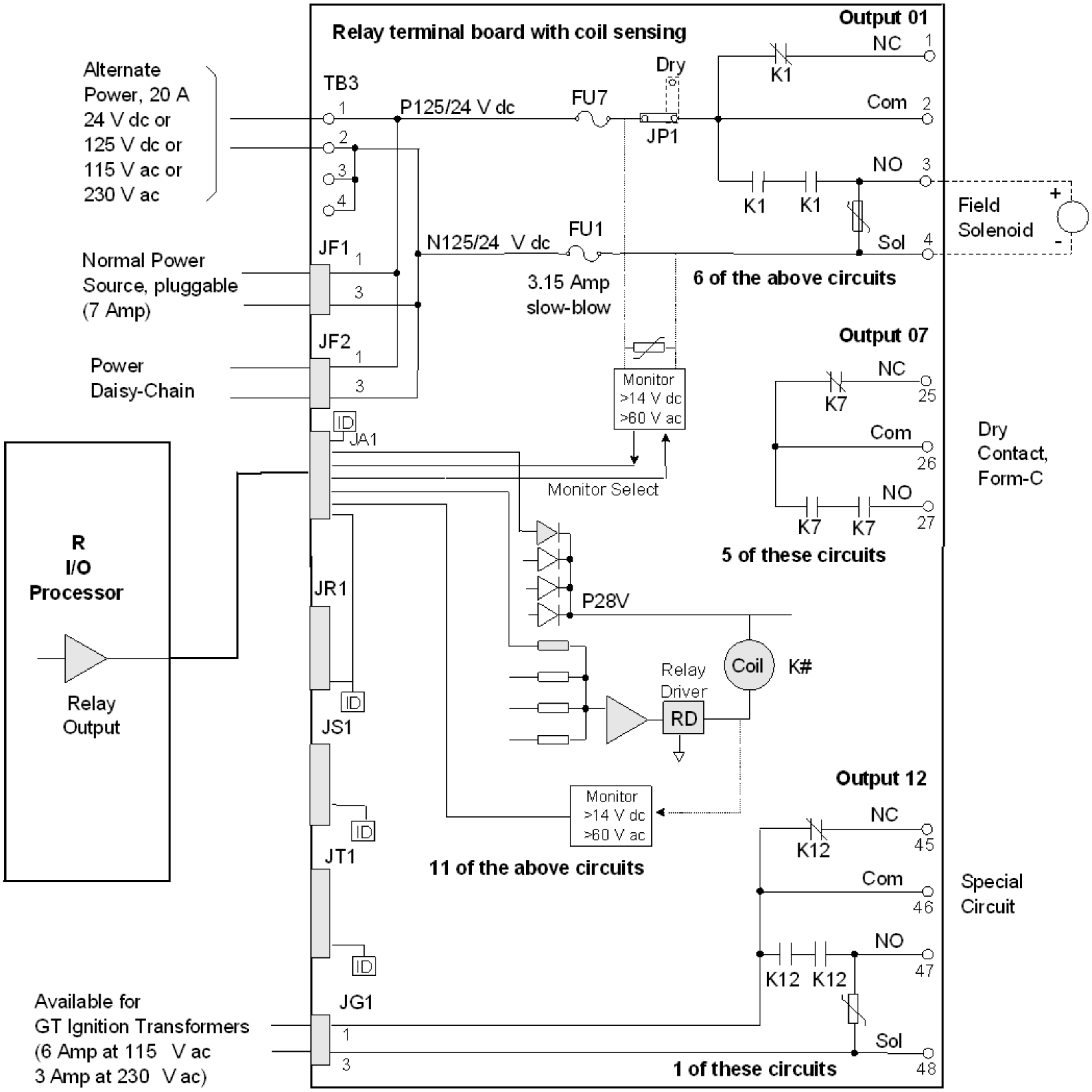
When the board is also supplied with 125 V dc, the preferred solution is not to connect the circuits 01 through 06 to ac-powered control circuits. If there is insufficient spare availability, remove both the fuses and the jumper for the contact in use for ac switching, isolating the ac voltage on the contact circuit from the dc distribution voltage. Store the jumpers and fuseholder caps separately to reduce the possibility of inadvertent re-installation, (for example after some maintenance activity).

The risk of damage to the MOVs due to cross-connections between the ac and dc power systems is not limited to the TRLY, but is present anywhere the 125 V dc is exposed to cross-connection to 125 V ac. This is including but not limited to contact sensing in motor control centers and breaker close circuits.

8.6.3.2 Simplex

Relay drivers, fuses, and jumpers are mounted on the TRLY_1B. For simplex operation, D-type connectors carry control signals and monitor feedback voltages between the I/O pack and TRLY_1B through JA1.

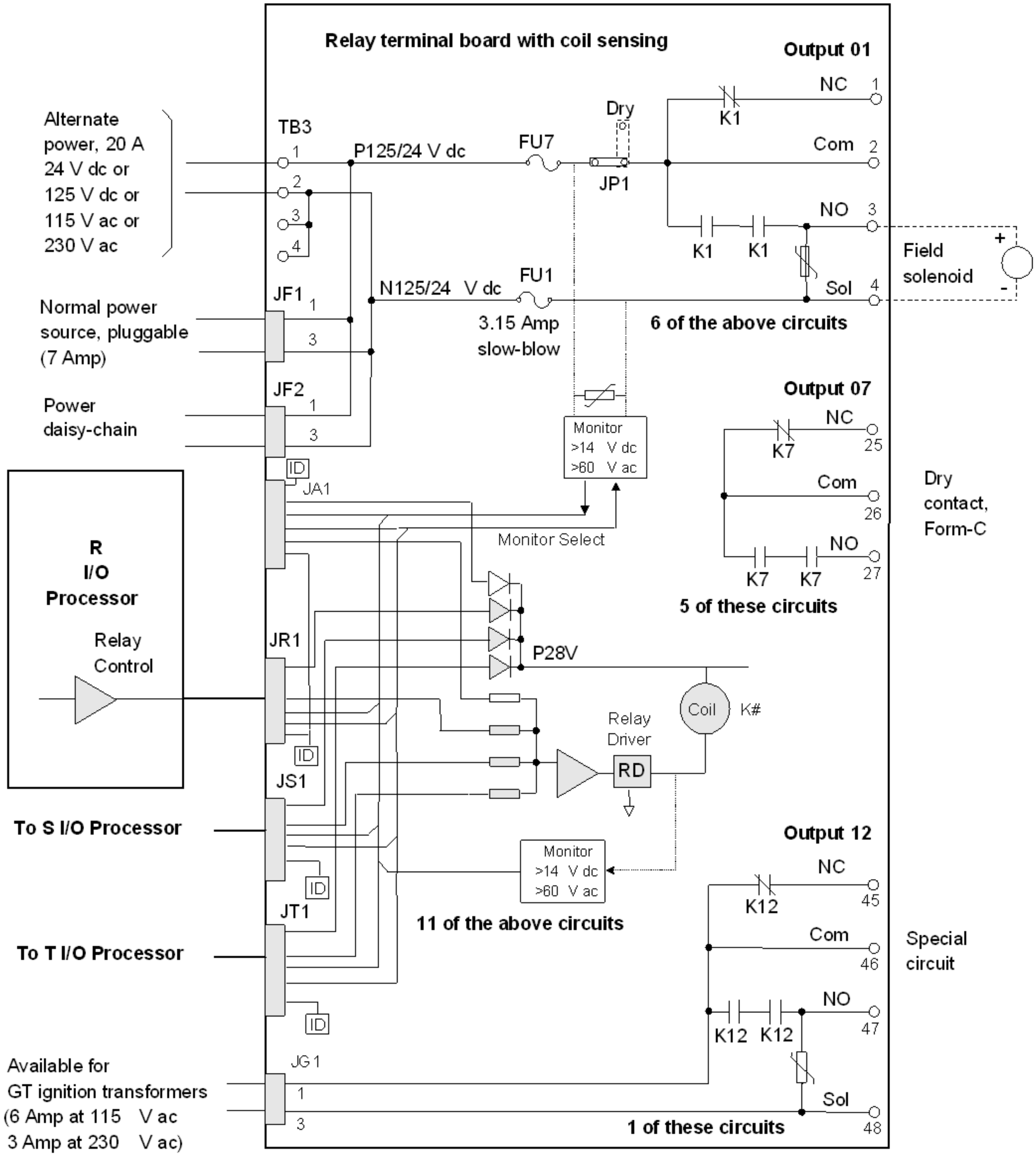
Relays are driven at the frame rate and have a 3.0 A ac rating. The typical time to operate is 10 ms. Relays 1-6 have a 250 V metal oxide varistor (MOV) for transient suppression between Normally Open (NO) and the power return terminals. The relay outputs have a fail-safe feature that vote to de-energize the corresponding relay when a cable is unplugged or communication with the associated I/O pack is lost.



TRLY_1B Circuits, Simplex System

8.6.3.3 TMR

For TMR applications, relay control signals are fanned into TRLY_1B from the three I/O processors R, S, and T through plugs JR1, JS1, and JT1. These signals are voted and the result controls the corresponding relay driver. Power for the relay coils comes from all three I/O packs and is diode-shared.



TRLY_1B Circuits, TMR

8.6.4 TRLY_1B Specifications

Item	TRLY_1B Specification
Number of Relay Channels on One TRLY_1B Board	12: 6 relays with optional solenoid driver voltages 5 relays with dry contacts only 1 relay with 7 A rating
Rated Voltage on Relays	Nominal 125 V dc or 24 V dc Nominal 115/230 V ac
Max Load Current	0.6 A for 125 V dc operation 3.0 A for 24 V dc operation 3.0 A for 115 / 230 V ac, 50/60 Hz operation 6 A at 115 V ac for relay 12 only
Relay Contact Current Rating	24 V dc voltage current rating 10 A, resistive current rating 2 A, L/R = 7 ms, without suppression
	125 V dc voltage current rating 0.5 A, resistive current rating 0.2 A, L/R = 7 ms, without suppression
	125 V dc voltage current rating 0.5 A, resistive current rating 0.65 A, L/R = 150 ms, with suppression (MOV) across the load
	115 / 230 ac voltage current rating 3.0 A
Max Response Time On	25 ms typical
Max Response Time Off	25 ms typical
Maximum Inrush Current	10 A
Contact Material	Silver cad-oxide
Contact Life	Electrical operations: 100,000 Mechanical operations: 10,000,000
Fault Detection	Loss of relay solenoid excitation current Coil current disagreement with command Unplugged cable or loss of communication with I/O board: relays de-energize if communication with associated I/O board is lost
Size	17.8 cm wide x 33.02 cm high (7.0 in x 13.0 in)

8.6.5 TRLY_1B Diagnostics

Diagnostic tests to components on the terminal boards are as follows:

- The output of each relay (coil current) is monitored and checked against the command at the frame rate. If there is no agreement for five consecutive frames, then an alarm is generated.
- The solenoid excitation voltage is monitored downstream of the fuses and an alarm is latched if it falls below 12 V dc.
- If any one of the outputs goes unhealthy a composite diagnostics alarm, L3DIAG_xxxx occurs.
- Each terminal board connector has its own ID device that is interrogated by the I/O pack. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the JA1/JR1/JS1/JT1 connector location. When the chip is read by the I/O pack and mismatch is encountered, a hardware incompatibility fault is created.
- Relay contact voltage is monitored.
- Details of the individual diagnostics are available in the configuration application. The diagnostic signals can be individually latched, and then reset with the RSTDIAG signal if they go healthy.

8.6.6 TRLY_1B Configuration

Board adjustments are made as follows:

- Jumpers JP1 through JP12. If power is required for relay outputs 1-12, insert jumpers for selected relays.
- Fuses FU1 through FU12. If power is required for relays 1-6, two fuses should be placed in each power circuit supplying those relays. For example, FU1 and FU7 supply relay output 1.

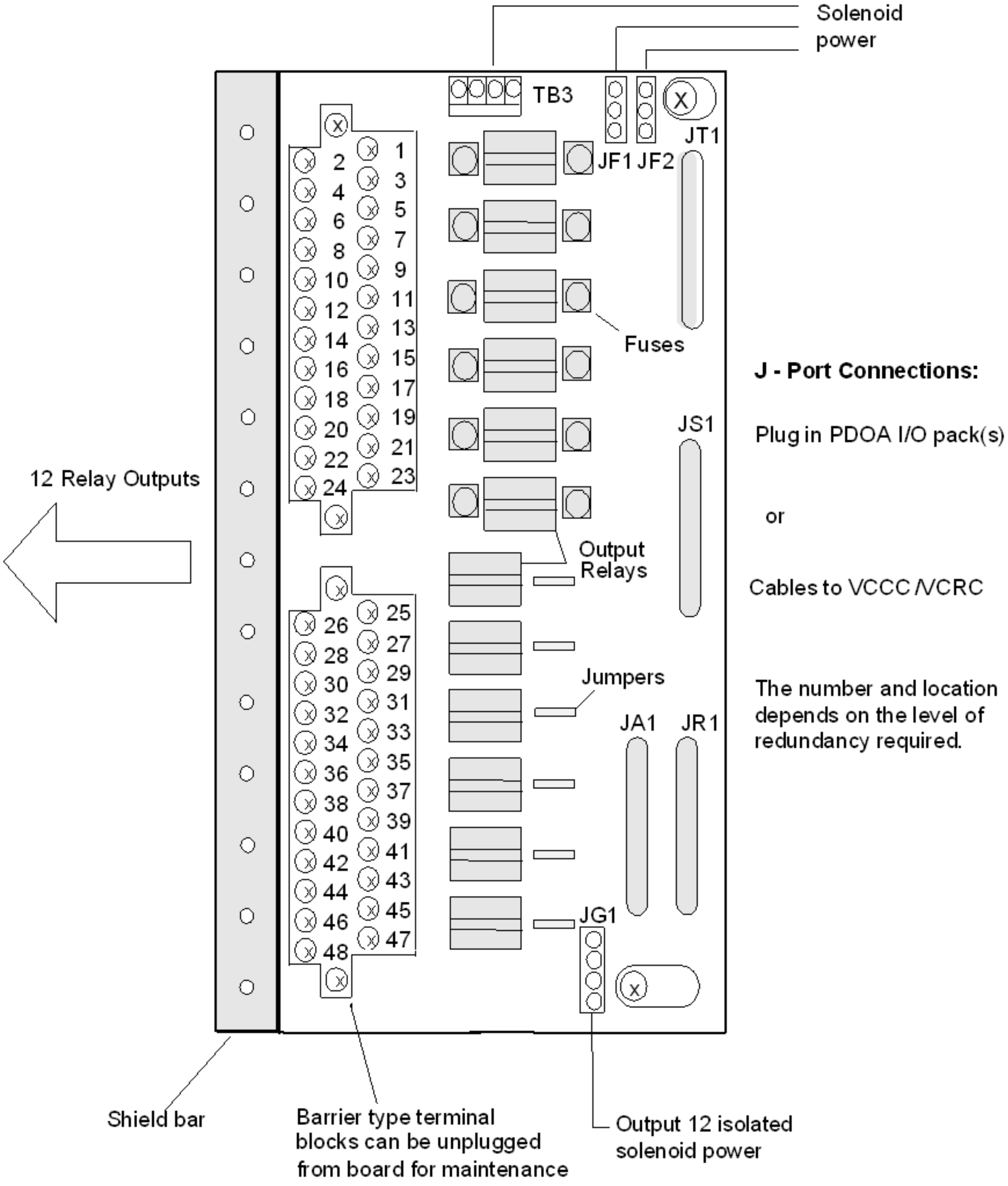
8.7 TRLYH#C Relay Output with Contact Sensing

The Relay Output with contact sensing (TRLYH#C) terminal board holds 12 plug-in magnetic relays. The first six relay circuits are Form-C contact outputs to drive external solenoids. TRLYH1C has a standard 125 V dc or 115 V ac source with fuses and on-board suppression is provided for field solenoid power. TRLYH2C has a standard 24 V dc source with fuses and on-board suppression is provided for field solenoid power.

The next five relays (7-11) are unpowered, isolated Form-C contacts. Output 12 is an isolated Form-C contact with non-fused power supply, used for ignition transformers. For example, 12 NO contacts have jumpers to apply or remove the feedback voltage sensing.

TRLYH#C is the same as the standard TRLYH1B board except for the following:

- Six jumpers for converting the solenoid outputs to dry contact type are removed. These jumpers were associated with the fuse monitoring.
- Input relay coil monitoring is removed from the 12 relays.
- Relay contact voltage monitoring is added to the 12 relays. Individual monitoring circuits have voltage suppression and can be isolated by removing their associated jumper.
- High-frequency snubbers are installed across the NO and SOL terminals on the six solenoid driver circuits and on the special circuit, output 12.



TRLYH#C Relay Output Terminal Board With Voltage Sensing

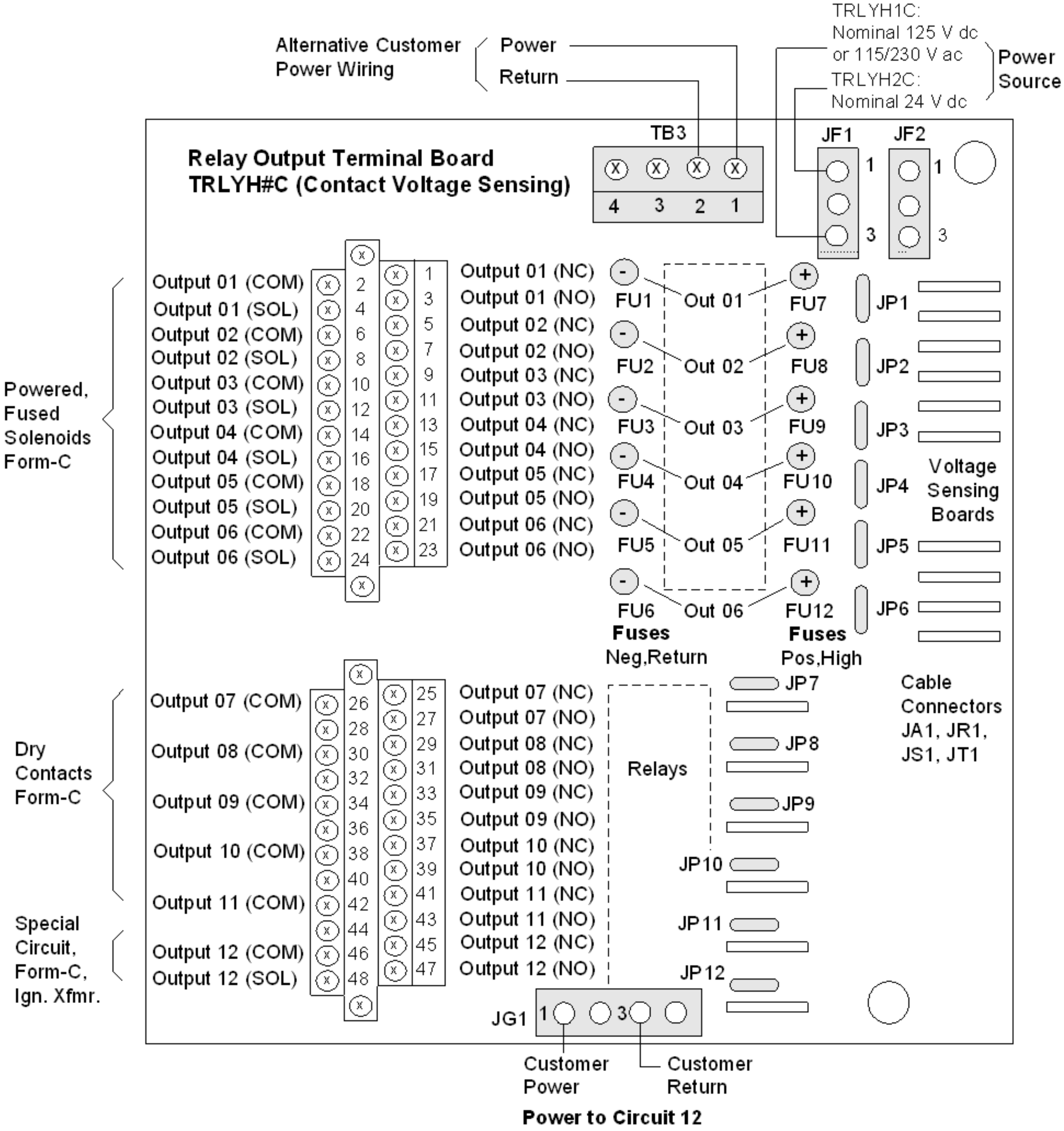
8.7.1 TRLYH#C Installation

The TRLYH#C works with the PDOA I/O pack and supports simplex and TMR applications. The PDOA plugs into the DC-37 pin connectors on the terminal board. Connector JA1 is used on simplex systems, and connectors JR1, JS1, and JT1 are used for TMR systems.

Connect the wires for the 12 relay outputs directly to two I/O terminal blocks on the terminal board as displayed in the figure, *TRLYH#C Terminal Board Wiring*. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield terminal strip attached to chassis ground is located immediately to the left of each terminal block.

Connect the solenoid power for outputs 1-6 to JF1 normally. JF2 can be used to daisy-chain power to other TRLYs. Alternatively, power can be wired directly to TB3 when JF1/JF2 are not used. Connect power for the special solenoid, Output 12, to connector JG1.

Jumpers JP1-12 remove the voltage monitoring from selected outputs.

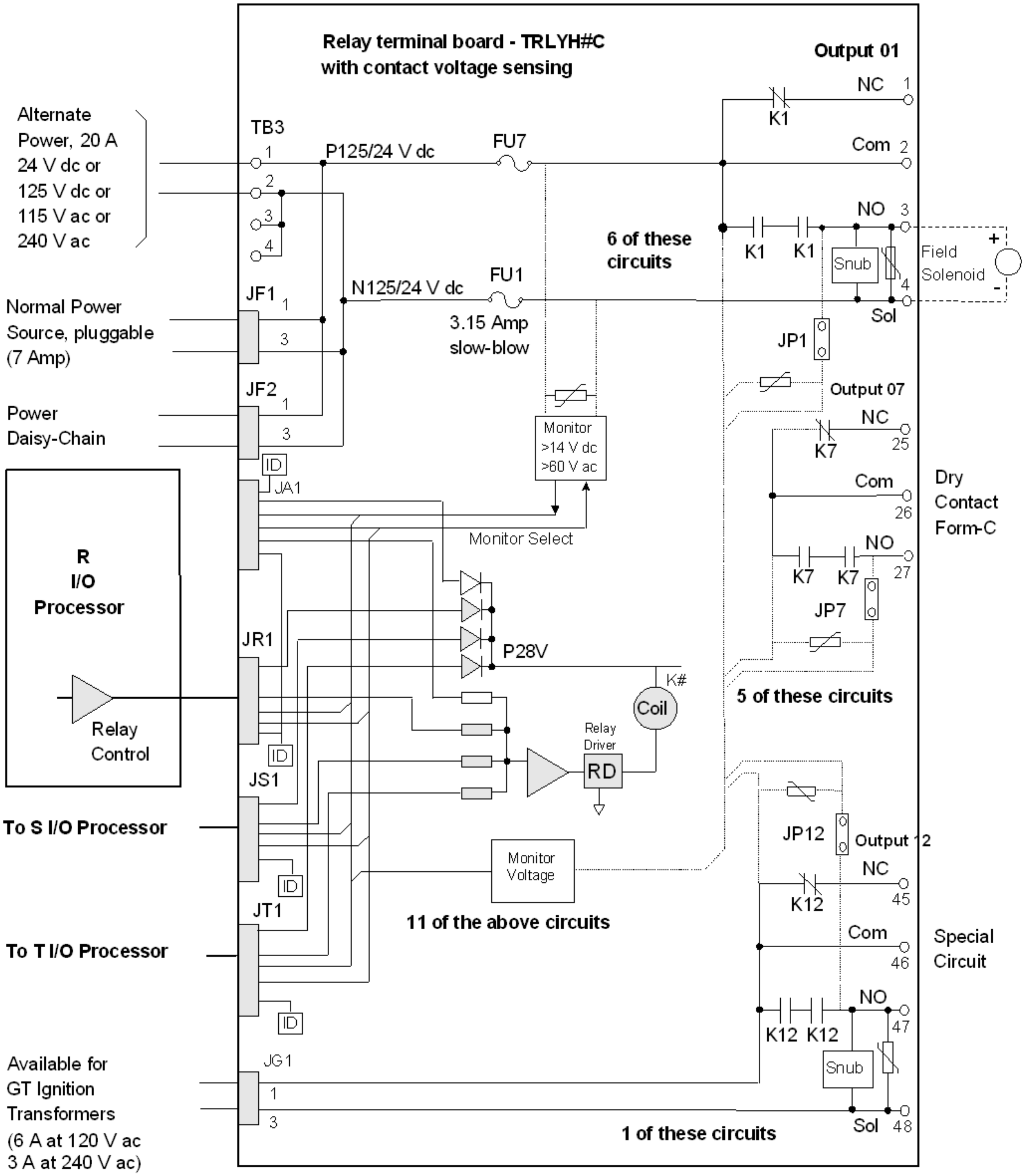


TRLYH#C Terminal Board Wiring

8.7.2 TRLYH#C Operation

Relay drivers, fuses, and jumpers are mounted on the TRLYH#C. Relays 1-6 have a 250 V MOV for transient suppression between the NO and power return terminals. Relays are driven at the frame rate and have a 3.0 A ac rating. The typical time to operate is 10 ms. The relay outputs have a fail-safe feature that votes to de-energize the corresponding relay when a cable is unplugged or communication with the associated I/O pack is lost.

For simplex operation, a connector carries control signals and monitor feedback voltages between the I/O pack and TRLY through JA1. For TMR applications, relay control signals are fanned into TRLY from the three I/O packs/boards R, S, and T through plugs JR1, JS1, and JT1. These signals are voted and the result controls the corresponding relay driver. The 28 V power for the relay coils comes in from all three I/O packs and is diode-shared. The following figure displays a TRLYH#C in a TMR system.



TRLYH#C Circuits in a TMR System

8.7.3 TRLYH#C Specifications

Item	TRLYH#C Specifications
Number of Relay Channels on One Terminal Board	12 total: 6 relays with solenoid driver voltages 5 relays with dry contacts only 1 relay with 7 A rating
Rated Voltage on Relays	TRLYH1C: nominal 125 V dc or 115/230 V ac TRLYH2C: nominal 24 V dc
Max Load Current	0.6 A for 125 V dc operation 3.0 A for 24 V dc operation 3.0 A for 115/230 V ac, 50/60 Hz operation 6 A at 115 V ac for relay 12 only
Relay Contact Rating	24 V dc voltage current rating 10 A, resistive current rating 2 A, L/R = 7 ms, without suppression
	125 V dc voltage current rating 0.5 A, resistive current rating 0.2 A, L/R = 7 ms, without suppression
	125 V dc voltage current rating 0.5 A, resistive current rating 0.65 A, L/R = 150 ms, with suppression (MOV) across the load
Max Response Time On	25 ms typical
Max Response Time Off	25 ms typical
H1C Contact Feedback Threshold	70-145 V dc, nominal 125 V dc, threshold 45 to 65 V dc 90-132 V rms, nominal 115 V rms, 47-63 Hz, threshold 45 to 72 V ac 190-264 V rms, nominal 230 V rms, 47-63 Hz, threshold 45 to 72 V ac
H2C Contact Feedback Threshold	16-32 V dc, nominal 24 V dc, threshold 10 to 16 V dc
Max Response Time Off	25 ms typical
Contact Material	Silver cad-oxide
Contact Life	Electrical operations: 100,000 Mechanical operations: 10,000,000
Fault Detection	Loss of relay excitation current NO contact voltage disagreement with command Unplugged cable or loss of communication with I/O pack; relays de-energize if communication with associated I/O pack is lost
Size	17.8 cm wide x 33.02 cm high (7.0 in x 13.0 in)

8.7.4 TRLYH#E Diagnostics

Diagnostic tests to components on the terminal boards are as follows:

- The output of each relay (coil current) is monitored and checked against the command at the frame rate. If there is no agreement for five consecutive frames, an alarm is generated.
- The solenoid excitation voltage is monitored downstream of the fuses and an alarm is latched if it falls below 12 V dc.
- If any one of the outputs goes unhealthy a composite diagnostics alarm, L3DIAG_xxxx occurs.
- Each terminal board connector has its own ID device that is interrogated by the I/O pack. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the JA1/JR1/JS1/JT1 connector location. When the chip is read by the I/O pack and mismatch is encountered, a hardware incompatibility fault is created.
- Relay contact voltage is monitored.
- Details of the individual diagnostics are available in the configuration application. The diagnostic signals can be individually latched, and then reset with the RSTDIAG signal if they go healthy.

8.7.5 TRLYH#C Configuration

Board adjustments are made as follows:

- Jumpers JP1 through JP12. If contact voltage sensing is required, insert jumpers for selected relays.
- Fuses FU1 through FU12. If power is required for relays 1-6, two fuses should be placed in each power circuit supplying those relays. For example, FU1 and FU7 supply relay output 1.

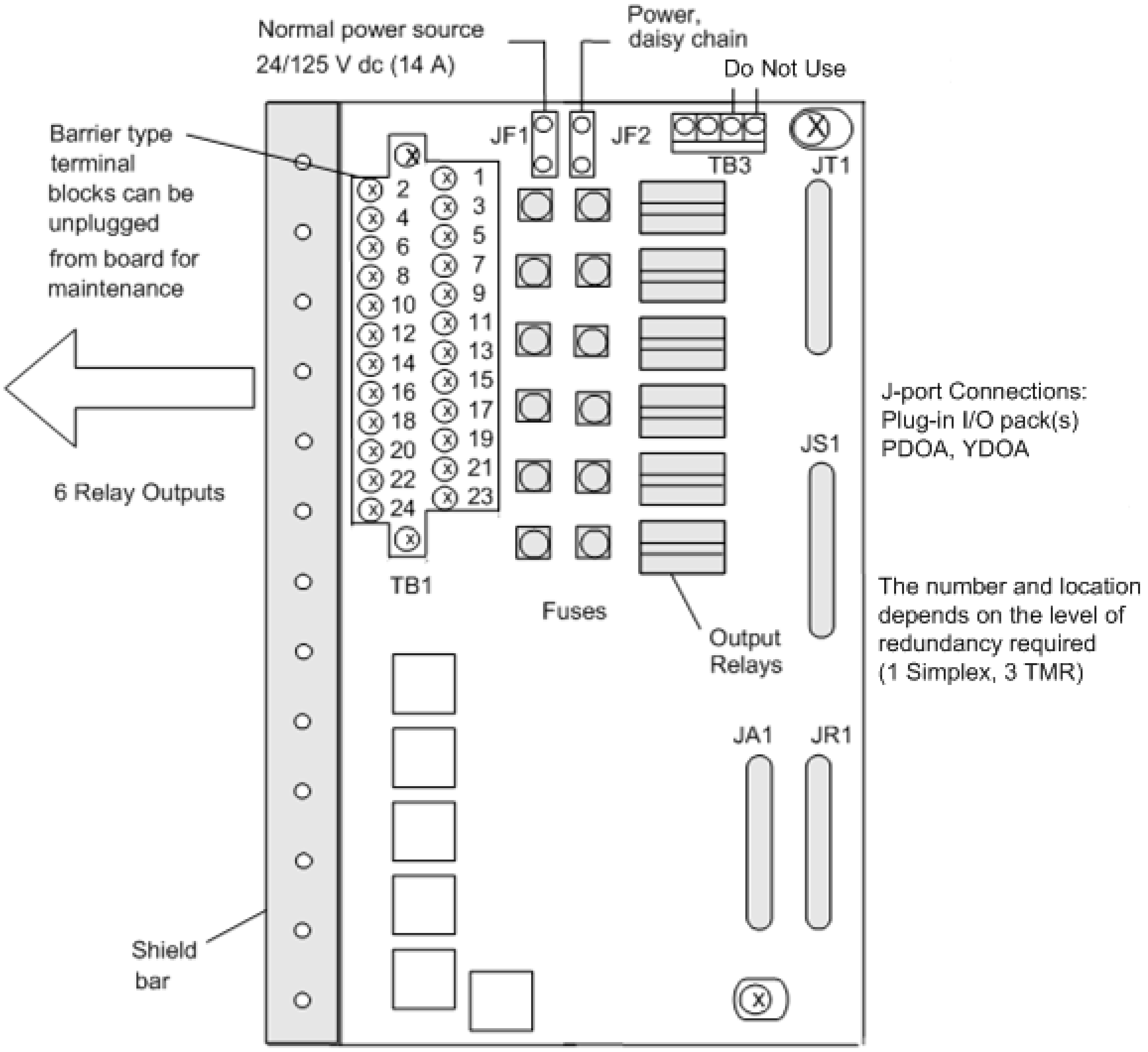
Note Refer to the figure, *TRLYH#C Terminal Board Wiring* for more information.

8.8 TRLYH1D, S1D Relay Output with Solenoid Integrity Sensing

The Relay Output with Solenoid Integrity Sensing (TRLY_1D) terminal board holds six plug-in magnetic relays. The six relay circuits are Form-C contact outputs, powered and fused to drive external solenoids. A standard 24 V dc or 125 V dc source can be used. The board provides special feedback on each relay circuit to detect a bad external solenoid. Sensing is applied between the NO output terminal and the SOL output terminal.

TRLY_1D is similar to the standard TRLY_1B board except for the following:

- There are six relays.
- The board is designed for 24/125 V dc applications only.
- Relay circuits have a NO contact in the return side as well as the source side.
- The relays cannot be configured for dry contact use.
- Input relay coil monitoring is removed.
- The terminal board provides monitoring of field solenoid integrity.
- There is no special-use relay for driving an ignition transformer.



TRLY_1D Block Diagram

8.8.1 TRLY_1D Compatibility

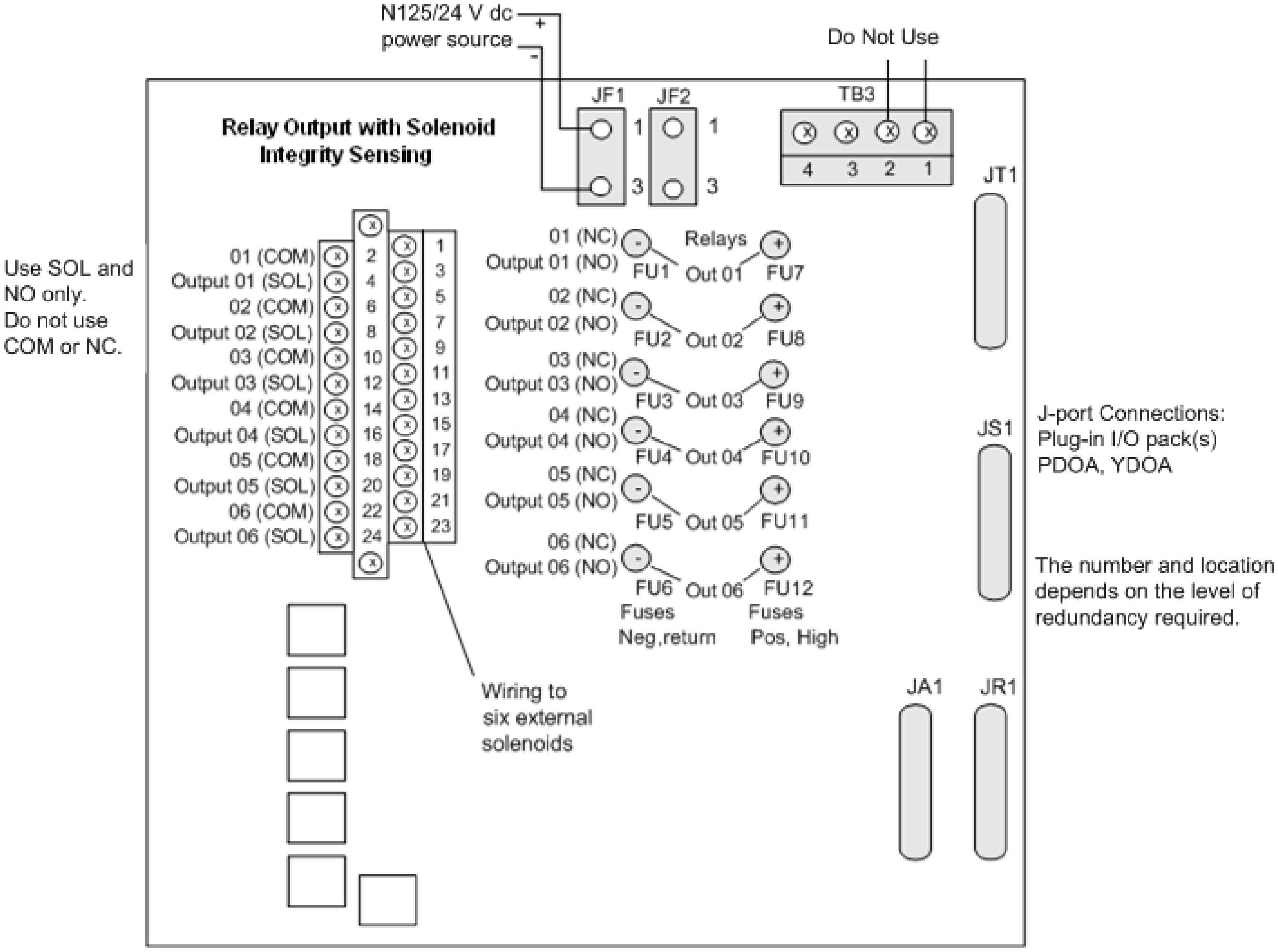
Connector JA1 is used for a simplex I/O pack, and connectors JR1, JS1, and JT1 are used for TMR I/O packs.

Board Revision	Mark VIe Control IS220PDOA, IS420PDOA	Mark VIeS Safety Control IS220YDOA, IS420YDOA	Comments
TRLYH1D	Yes, all versions	No	
TRLYS1D	Yes, all versions	Yes, all versions	IEC 61508 safety certified with Mark VIeS YDOA

8.8.2 TRLY_1D Installation

Connect the wires for the six relay outputs directly to the TB1 terminal block on the terminal board. The block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield terminal strip, attached to chassis ground, is located immediately to the left of the terminal block.

Connect the solenoid power for outputs 1-6 to JF1. JF2 can be used to daisy-chain power to other TRLYs. Do not use TB3.

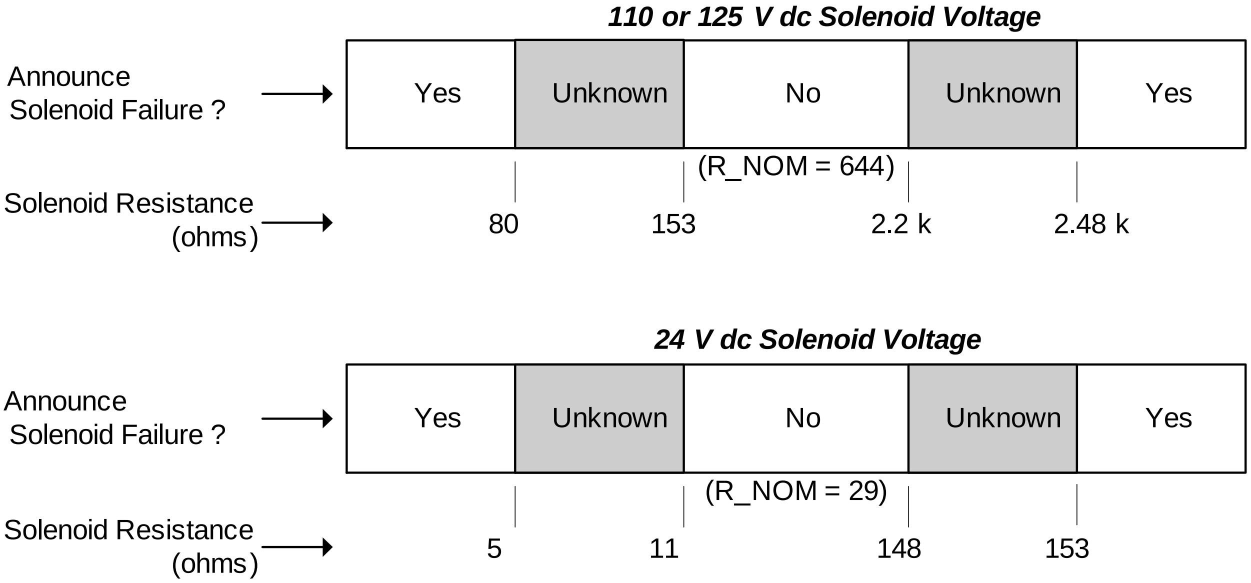


TRLY_1D Terminal Board Wiring

8.8.3 TRLY_1D Operation

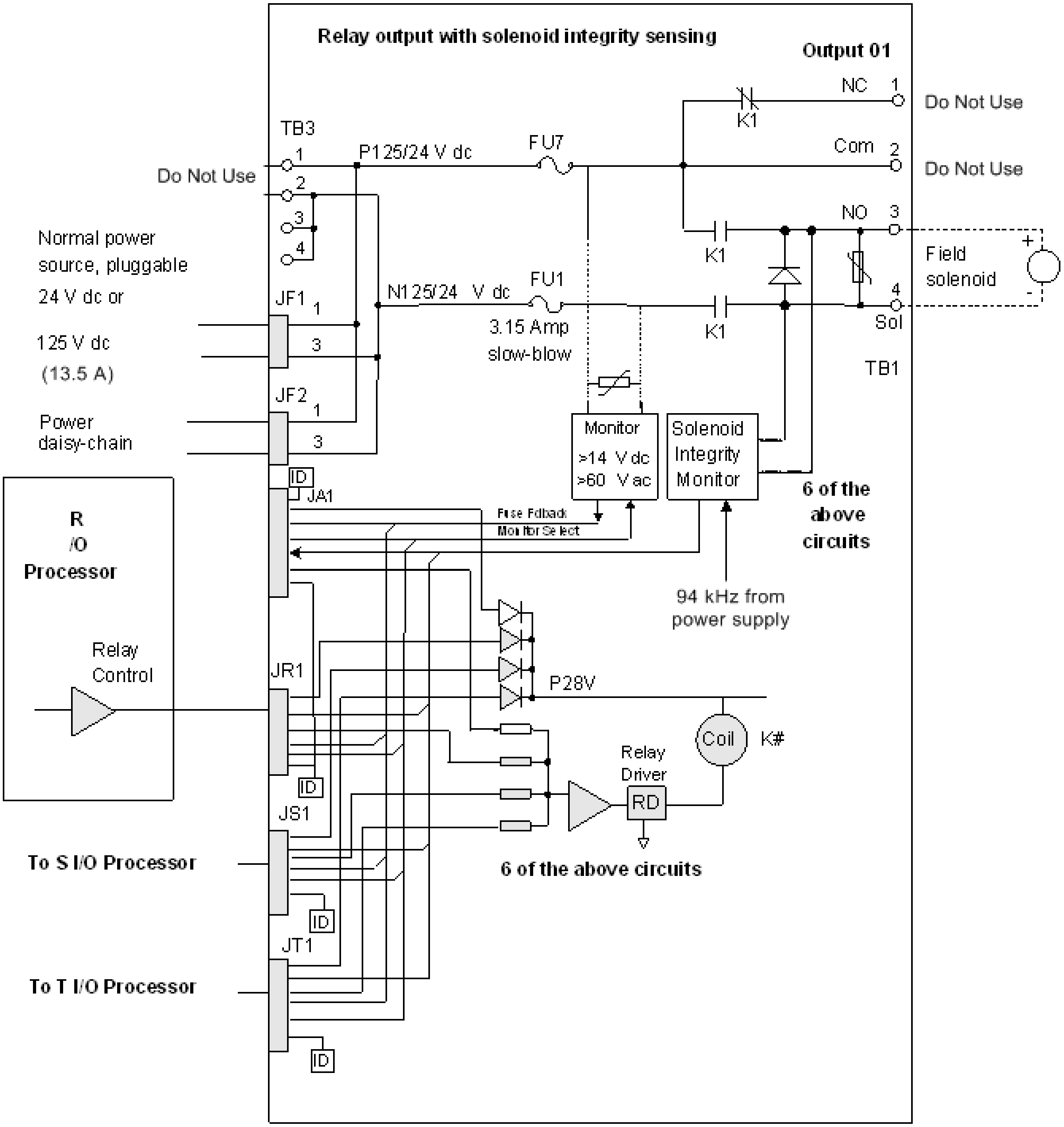
The six relays have a MOV and clamp diode for transient suppression between the NO and power return terminals. The relay outputs have a fail-safe feature that votes to de-energize the corresponding relay when a cable is unplugged or communication with the associated I/O pack is lost.

The TRLY_1D monitors each solenoid between the NO and SOL output terminals. When the relay is de-energized, the circuit applies a bias of less than 8% nominal voltage to determine if the load impedance is within an allowable band. An alarm is generated when the contact is open and the impedance is too low or too high for 20 consecutive scans (500 ms frame rate = 10 seconds). The contacts must be open for at least 1.3 seconds to get a valid reading.


110 or 125 V dc Solenoid Voltage
Announce Solenoid Failure ?
Yes
Unknown
No
Unknown
Yes
(R_NOM = 644)
Solenoid Resistance (ohms)
80
153
2.2 k
2.48 k
24 V dc Solenoid Voltage
Announce Solenoid Failure ?
Yes
Unknown
No
Unknown
Yes
(R_NOM = 29)
Solenoid Resistance (ohms)
5
11
148
153

TRLY_1D Solenoid Fault Announcement

For simplex operation, cables carry control signals and solenoid monitoring feedback voltages between the I/O pack and TRLY_1D through JA1. For TMR applications, relay control signals are fanned into TRLY_1D from the three I/O packs R, S, and T through plugs JR1, JS1, and JT1. These signals are voted and the result controls the corresponding relay driver. Power for the relay coils comes in from all three I/O packs and is diode-shared.



TRLY_1D Circuits (TMR)

8.8.4 TRLY_1D Specifications

Item	TRLY_1D Specification
Number of Relay Channels	Six relays with special customer solenoid monitoring
Rated Voltage on Relays	Nominal 125 or 24 V dc
Wetting Power, JF1/JF2	13.5 A max
Relay Contact Rating for 24 V dc Solenoids	Current rating 2.25 A, resistive Current rating 2 A, L/R = 7 ms, without suppression
Relay Contact Rating for 125 V dc Solenoids	Current rating 0.5 A, resistive Current rating 0.2 A, L/R = 7 ms, without suppression Current rating 0.5 A, L/R = 150 ms, with suppression (MOV) across the load
Maximum Response Time On	25 ms typical
Maximum Response Time Off	25 ms typical
Contact Life	Electrical operations: 100,000
Board Size	17.8 x 33.0 cm (7 x 13 in)
Fault Detection	Loss of solenoid voltage supply (fuse monitor) Solenoid resistance measured to detect open and short circuits Unplugged cable or loss of communication with I/O pack (relays de-energize if communication with associated I/O pack is lost)
Size	17.8 wide x 33.02 cm high (7.0 x 13.0 in)

8.8.5 TRLY_1D Diagnostics

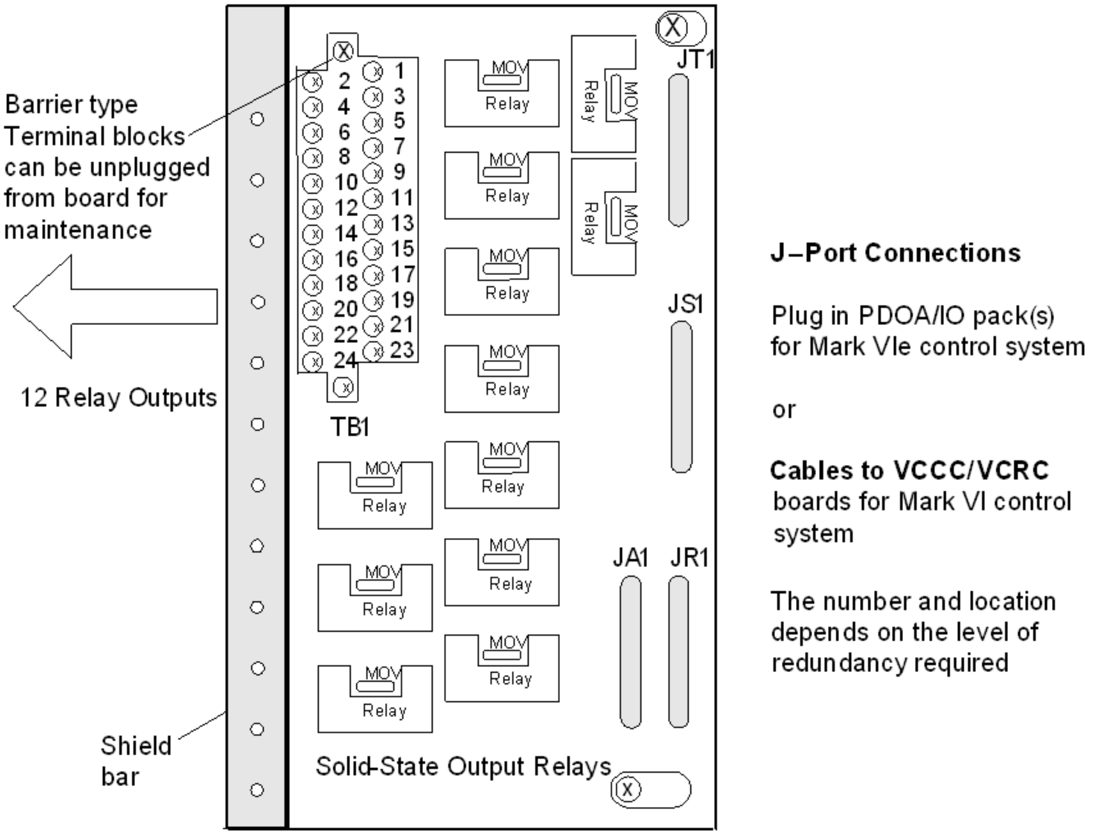
Diagnostic tests to components on the terminal boards are as follows:

- The solenoid excitation voltage is monitored downstream of the fuses and an alarm is latched if it falls below 12 V dc.
- If any one of the outputs goes unhealthy a composite diagnostics alarm, L3DIAG_xxxx occurs.
- Each terminal board connector has its own ID device that is interrogated by the I/O pack. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the JA1/JR1/JS1/JT1 connector location. When the chip is read by the I/O pack and mismatch is encountered, a hardware incompatibility fault is created.
- Details of the individual diagnostics are available in the configuration application. The diagnostic signals can be individually latched, and then reset with the RSTDIAG signal if they go healthy.

8.9 TRLYH#E Solid-State Relay Output

The solid-state Relay Output (TRLYH#E) terminal board is a 12-output relay board using solid-state relays for the outputs and featuring isolated output voltage feedback on all 12 circuits. Unlike the form-C contacts provided on the mechanical relay boards, all 12 outputs on TRLYH#E are single, NO, contacts. There is no user solenoid power distribution on the board. The use of solid-state relays requires three different board types:

- TRLYH1E for 115 V ac applications
- TRLYH2E for 24 V dc applications
- TRLYH3E for 125 V dc applications



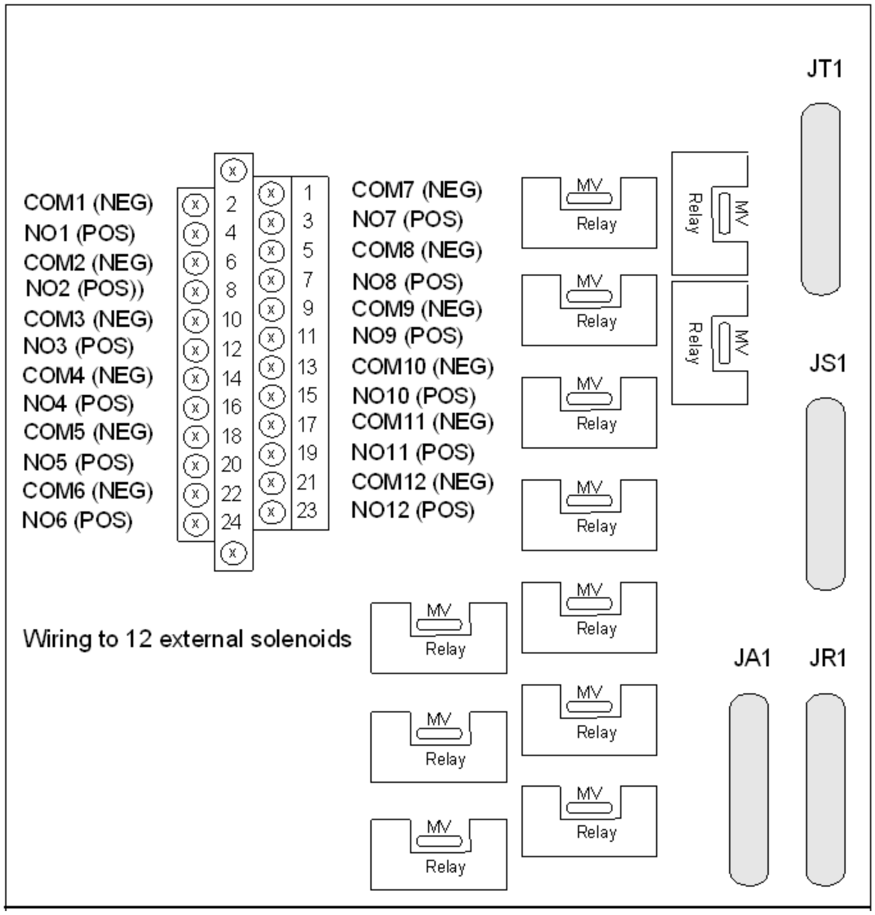
Barrier type Terminal blocks can be unplugged from board for maintenance
12 Relay Outputs
Shield bar
TB1
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
MOV
Relay
JT1
JS1
JA1
JR1
Solid-State Output Relays
J–Port Connections
Plug in PDOA/IO pack(s) for Mark VIe control system
or
Cables to VCCC/VCRC boards for Mark VI control system
The number and location depends on the level of redundancy required

TRLYH#E Solid-State Relay Output Terminal Board

8.9.1 TRLYH#E Installation

The TRLYH#E works with the PDOA I/O pack and supports simplex and TMR applications. The PDOA plugs into the DC-37 pin connectors on the terminal board. Connector JA1 is used on simplex systems, and connectors JR1, JS1, and JT1 are used for TMR systems.

Connect the wires for the 12 solenoids directly to the I/O terminal block on the terminal board as displayed in the following figure. The terminal block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. The dc relays are unidirectional, so care should be taken about polarity when connecting load to these relays. A shield terminal strip attached to chassis ground is located immediately to the left of each terminal block. The solenoids must be powered externally by the customer.



J – Port Connections:

Plug in PDOA I/O packs(s) for Mark VIe control system

or

Cables to VCCC/VCRC boards for Mark VI control system

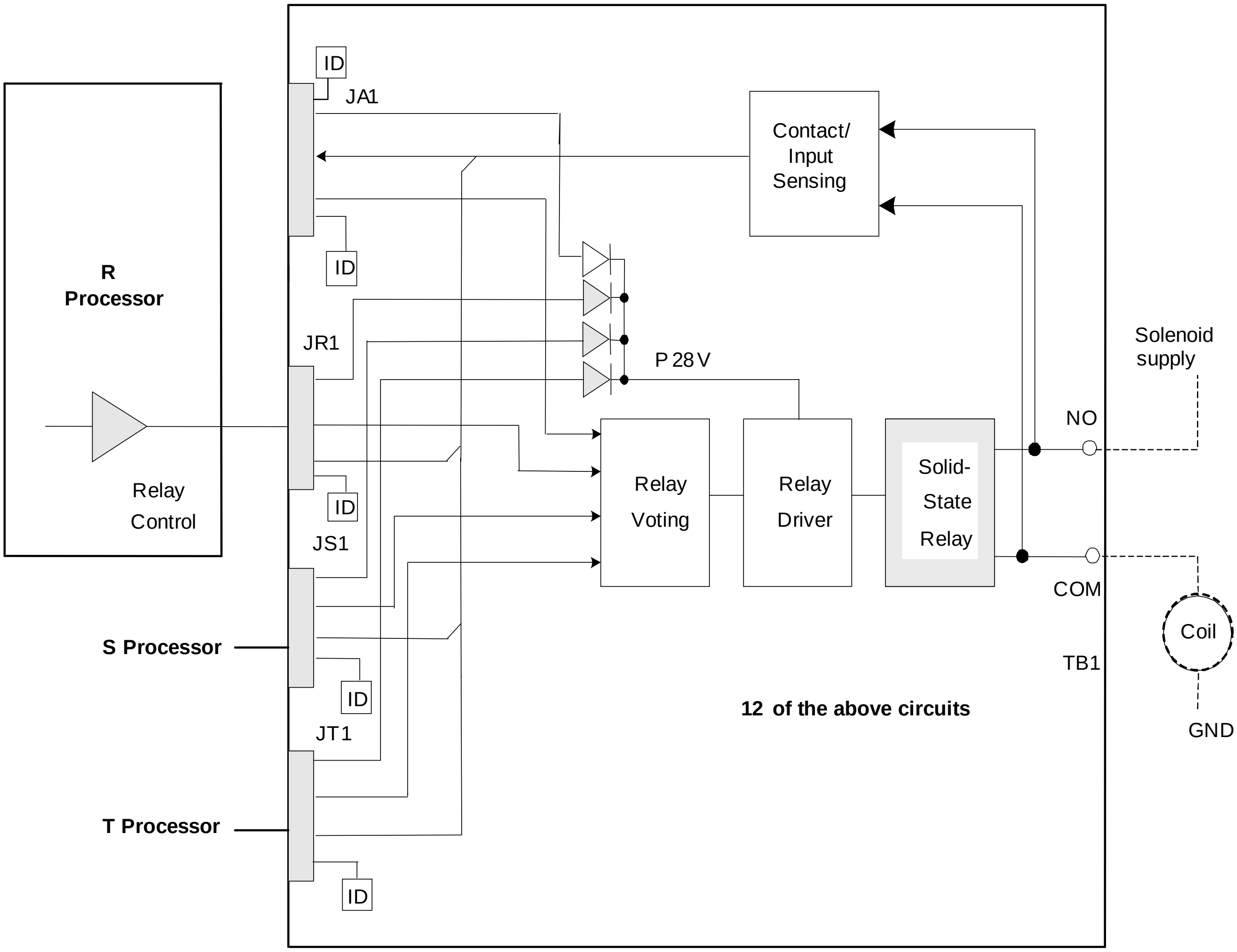
The number and location depends on the level of redundancy required.

TRLYH#E Terminal Board Wiring

TRLYH#E Operation

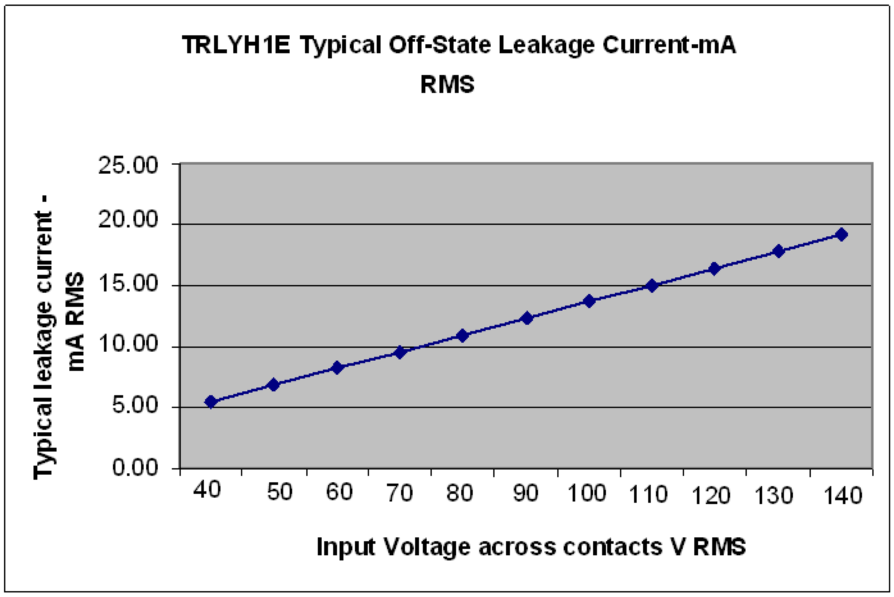
Normally Open (NO) solid-state relays, relay drivers, and output monitoring are mounted on TRLYH#E. During startup, relays stay de-energized while connected to any control. The relay outputs have a fail-safe feature that votes to de-energize the corresponding relay when a cable is unplugged or communication with the associated I/O pack is lost.

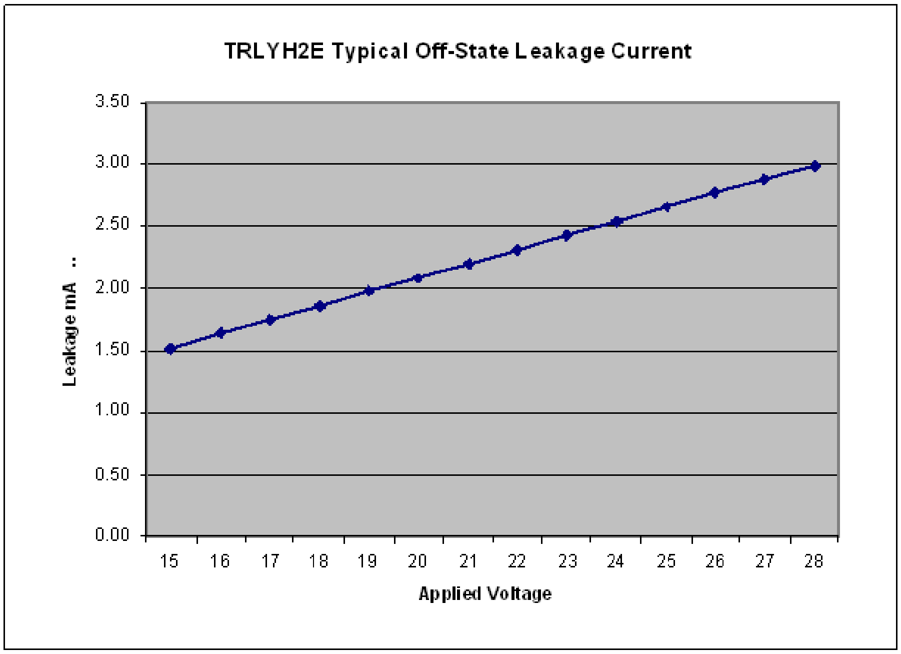
For simplex operation, control signals and relay output voltage feedback signals pass between the I/O pack and TRLY through JA1. For TMR applications, relay control signals are fanned into TRLY from the three I/O packs R, S, and T through plugs JR1, JS1, and JT1. These signals are voted and the result controls the corresponding relay driver. Power for the relay drivers comes in from all three I/O packs and is diode-shared.

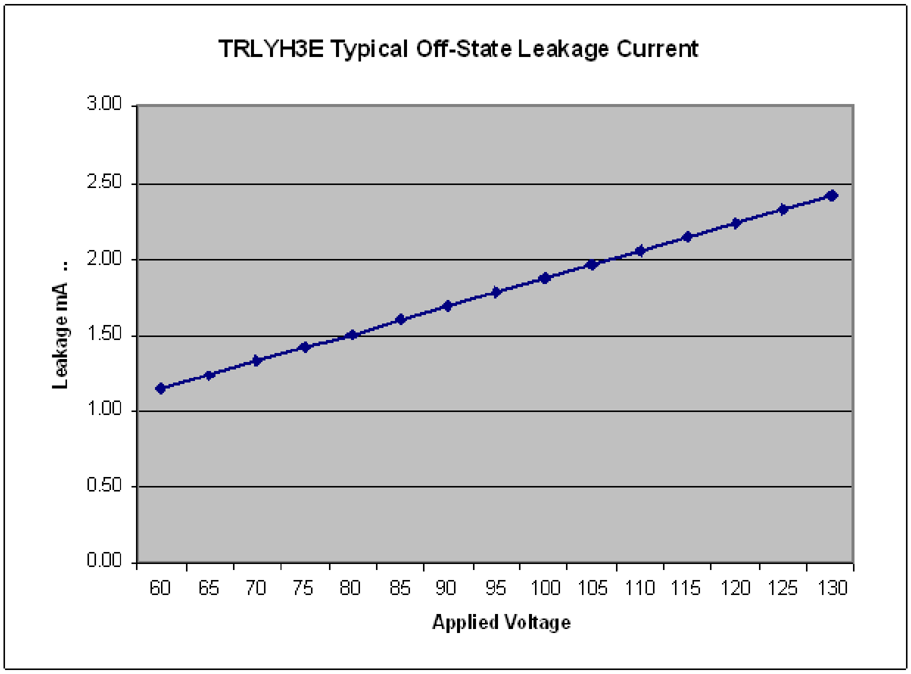


.1 Contact Voltage Feedback

In TRLYH#E, isolated feedback of voltage sensing is connected to the relay outputs. This allows the control to observe the voltage across the relay outputs without a galvanic connection. One contact sensing circuit is provided with each relay. This feature is similar to the voltage sensing on TRLYH#C but with simpler hardware. The voltage sensing circuit allows a small leakage current to pass to power the isolated circuit. The typical leakage current is the sum of the leakage through the turned off solid-state relay and the current through the voltage sensing circuit. The following charts indicate the typical leakage current as a function of the applied voltage for the three board types.







Due to the permitted leakage current, the board may give false indications if used in series with a low input current load, including common contact input circuits such as those found on or STCI. To ensure correct operation, the maximum load resistances for the three board types are as follows:

- TRLYH1E: Maximum load resistance at nominal 115 V ac is 2.5 kΩ.
- TRLYH2E: Maximum load resistance at nominal 24 V dc is 4.5 kΩ.
- TRLYH3E: Maximum load resistance at nominal 125 V dc is 25 kΩ.

Load resistance may be decreased by applying a resistor in parallel with the load so the parallel combination satisfies the maximum resistance requirement.

.2 Contact Voltage Rating

Solid-state relays have a finite transient voltage capability and require coordinated voltage protection. TRLYH1E for ac applications uses a load control device that turns off on a current zero crossing. This turn-off characteristic ensures that no inductive energy is present in the load at turn-off time. Basic protection of the ac relay is provided on TRLYH1E using a MOV with clamp voltage coordinated with relay voltage rating. In addition, there is an R-C snubber circuit on the relay output using a 56 Ω resistor in series with a 0.25 µF capacitor.

Both the TRLYH2E (for 24 V dc applications) and the TRLYH3E (for 125 V dc applications) can interrupt currents in large inductive loads. Because a wide range of loads may be encountered, an appropriate R-C or diode snubber circuit must be selected for each application. The snubber should be applied at the load device using common engineering practices. If the applied snubber does not fully control inductive switching voltage transients, both board versions contain an active voltage clamp circuit. This circuit activates at approximately 50-55 V dc for the H2E and at approximately 164-170 V dc for the H3E (both values below the rating of the relay). While the clamp circuit has a finite ability to absorb energy, it can handle the wiring inductance of a resistive load.

8.9.2 TRLYH#E Specifications

Item	TRLYH#E Specification
Number of Relay Channels on One TRLYH#E	12 relays: H1E: 115 V ac operation H2E: 24 V dc operation H3E: 125 V dc operation
Max Operating Voltage and Max Load current with Free Convection Air Flow	H1E: 250 V rms at 47-63 Hz, 10 A at 25ºC (77 ºF) maximum de-rate current linearly to 6 A at 65ºC (149 ºF) maximum
	H2E: 28 V dc, 10 A dc at 40ºC (104 ºF) maximum de-rate current linearly to 7 A dc at 65ºC (149 ºF) maximum
	H3E: 140 V dc, 3 A dc at 40ºC (104 ºF) maximum de-rate current linearly to 2 A dc at 65ºC (149 ºF) maximum
Max Off State Leakage *Refer to the charts of leakage compared to applied voltage in the section Contact Voltage Feedback.*	H1E: 20 mA rms at 140 V rms
	H2E: 3 mA dc at 28 V dc
	H3E: 2.5 mA dc at 130 V dc
Max Response Time On	1 ms for dc relays; 0.5 cycle for ac relay
Max Response Time Off	300 micro seconds for dc relays; 0.5 cycle for ac relay
Relay MTBF	H1E: 50 years H2E: 37 years H3E: 47 years
Relay Contact Voltage Sensing Threshold	H1E: 115 V ac, 70 V ±10% ac rms H2E: 24 V dc, 15 V ±2 V dc H3E: 125 V dc, 79 V ±10% dc
Operating Humidity	5 to 95% non-condensing
Fault Detection	Relay current disagreement with command Unplugged cable or loss of communication with I/O pack; relays de-energize if communication with associated I/O pack is lost
Size	17.8 cm wide x 33.02 cm high (7.0 in x 13.0 in)

8.9.3 TRLYH#E Diagnostics

Diagnostic tests to components on the terminal boards are as follows:

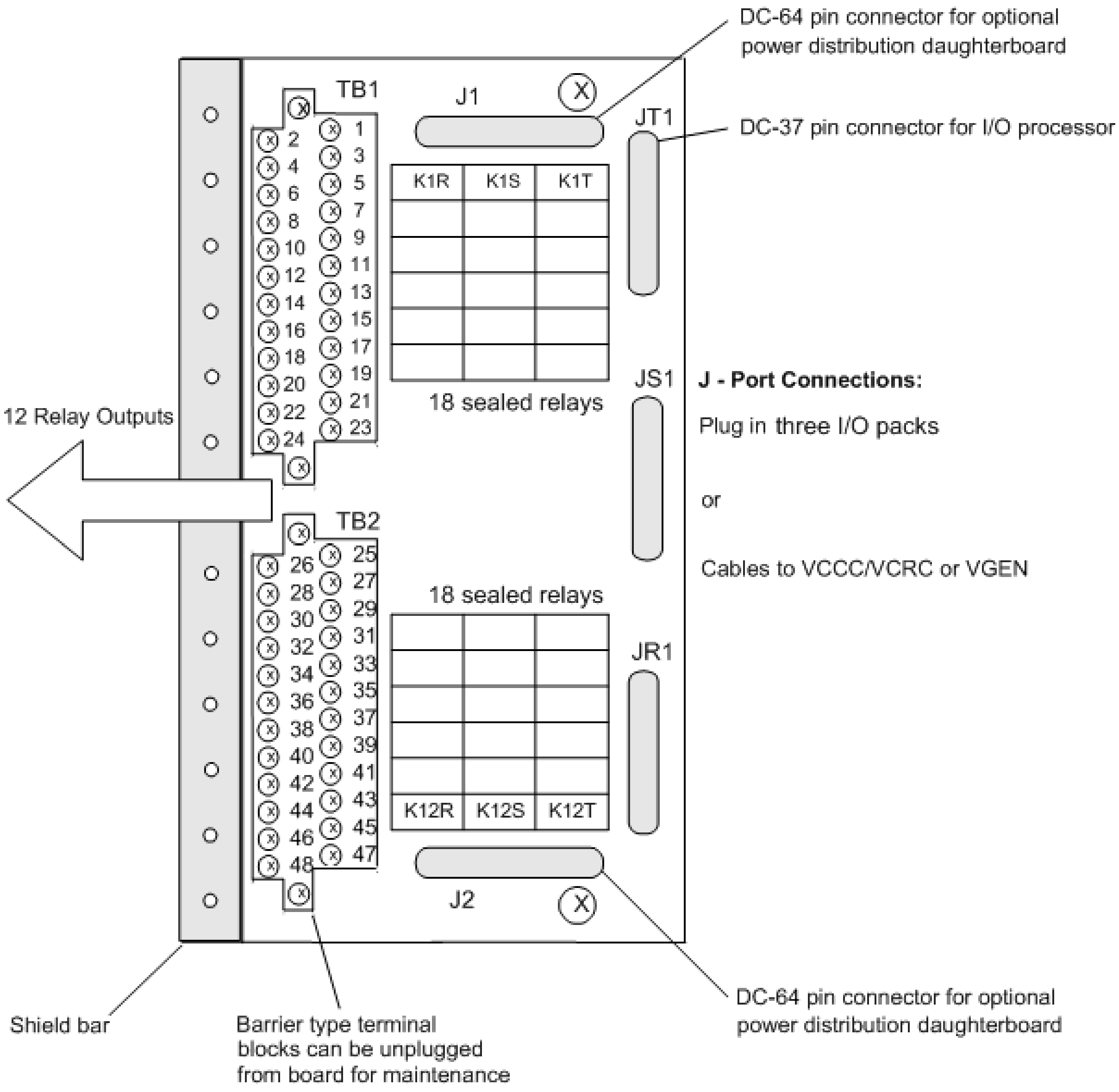
- The output of each relay (coil current) is monitored and checked against the command at the frame rate. If there is no agreement for five consecutive frames, an alarm is generated.
- The solenoid excitation voltage is monitored downstream of the fuses and an alarm is latched if it falls below 12 V dc.
- If any one of the outputs goes unhealthy a composite diagnostics alarm, L3DIAG_xxxx occurs.
- Each terminal board connector has its own ID device that is interrogated by the I/O pack. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the JA1/JR1/JS1/JT1 connector location. When the chip is read by the I/O pack and mismatch is encountered, a hardware incompatibility fault is created.
- Relay contact voltage is monitored.
- Details of the individual diagnostics are available in the configuration application. The diagnostic signals can be individually latched, and then reset with the RSTDIAG signal if they go healthy.

8.10 TRLYH#F, S#F Relay Output – TMR Contact Voting

The Relay Output with TMR contact voting (TRLY_1F and TRLY_2F) terminal boards provides 12 contact-voted relay outputs. The board holds 12 sealed relays in each TMR section, for a total of 36 relays. The relay contacts from R, S, and T are combined to form a voted Form A (NO) contact with TRLY_1F or the voted contacts are Form B (NC) output with TRLY_2F. Either 24/125 V dc or 115 V ac can be applied. TRLY_F boards do not support simplex applications and do not have power distribution.

An optional power distribution board, IS200WPDFH1A, can be added so that a standard 125 V dc or 115 V ac source, or an optional 24 V dc source with individual fuses, can be provided for field solenoid power. IS200WPDFH2A provides a single fuse in the high side (pin 1 of J1–J4) of each power distribution circuit for ac applications where a fuse in neutral return wire (pin 3 of J1–J4) is not desirable.

To reduce confusion in troubleshooting this highly interactive board set and to reduce mean time-to-repair, for first-stage troubleshooting the TRLY_#F/WPDF should be treated as the lowest replaceable unit (LRU) and replaced as a set when the diagnostic messages indicate that either is involved. If necessary, when time and conditions permit, the individual failed board can be further isolated using *golden* boards (a board previously known to be good) to match with the individual suspect board.



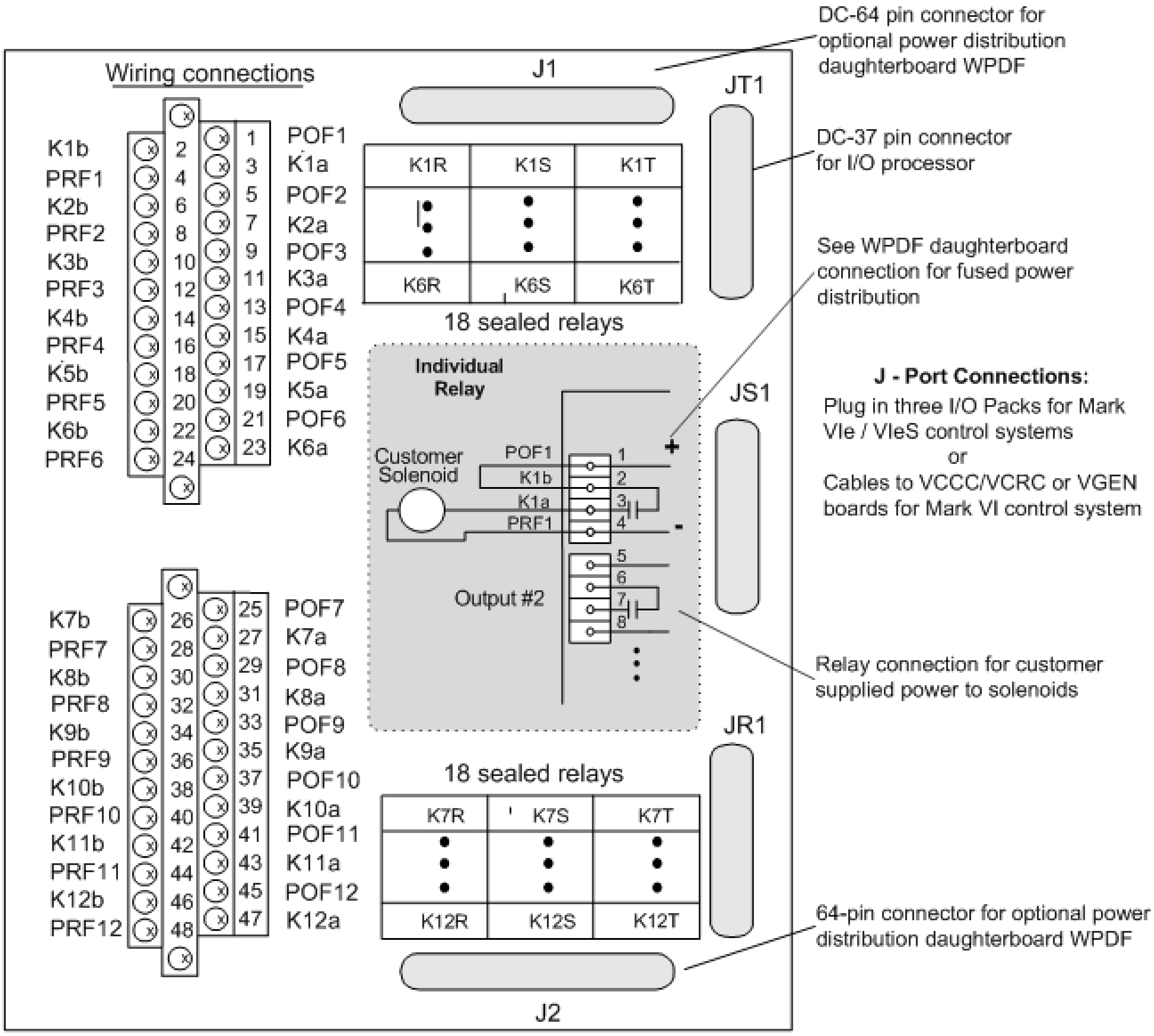
8.10.1 TRLY_F Compatibility

The TRLY_1F and TRLY_2F terminal boards only supports TMR applications. Three TMR I/O packs plug into the JR1, JS1, and JT1 37-pin D-type connectors on the terminal board.

Board Revision	Mark VIe Control PDOA	Mark VIeS Safety Control YDOA	Comments
TRLYH1F	Yes, all versions	No	Normally open contacts
TRLYH2F	Yes, all versions	No	Normally closed contacts
TRLYS1F	Yes, all versions	Yes, all versions	Normally open contacts, IEC 61508 safety certified with Mark VIeS YDOA
TRLYS2F	Yes, all versions	Yes, all versions	Normally closed contacts, IEC 61508 safety certified with Mark VIeS YDOA

8.10.2 TRLY_F Installation

Connect the wires for the 12 solenoids directly to two I/O terminal blocks on the terminal board. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield termination strip attached to chassis ground is located immediately to the left side of each terminal block. Solenoid power for outputs 1-12 is available if the WPDF daughterboard is used. Alternatively, customer power may be wired to the terminal block. The 28 V dc power for the terminal board relay coils and logic comes from the three I/O packs connected at JR1, JS1, and JT1.



DC-64 pin connector for optional power distribution daughterboard WPDF

DC-37 pin connector for I/O processor

See WPDF daughterboard connection for fused power distribution

J - Port Connections:
Plug in three I/O Packs for Mark VIe / VIeS control systems
or
Cables to VCCC/VCRC or VGEN boards for Mark VI control system

Relay connection for customer supplied power to solenoids

64-pin connector for optional power distribution daughterboard WPDF

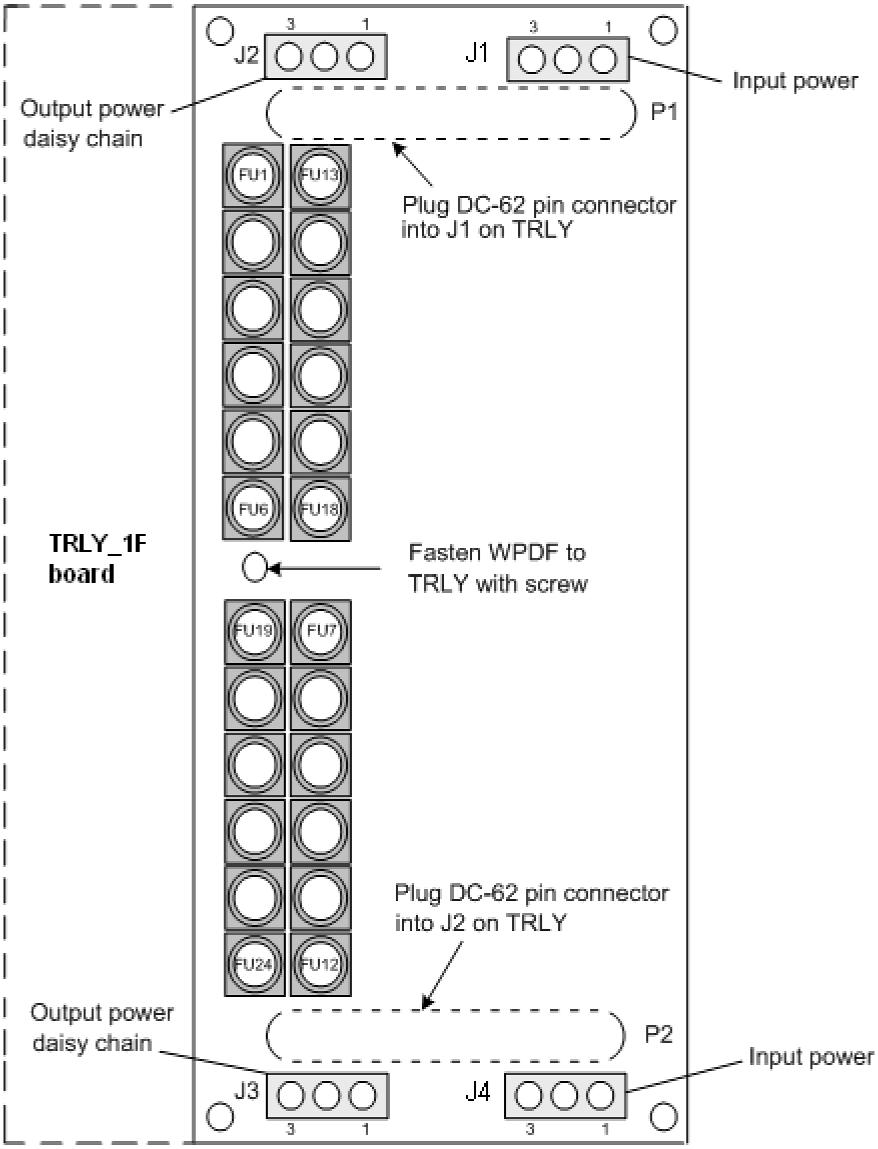
Signal Name	Description, n=1...12
POFn	Power Out Fused #n
PRFn	Power Return Fused #n
Kna	Resulting voted relay contact #n
Knb	Resulting voted relay contact #n

TRLY_1F Terminal Board Wiring

8.10.2.1 WPDF Power Distribution Board

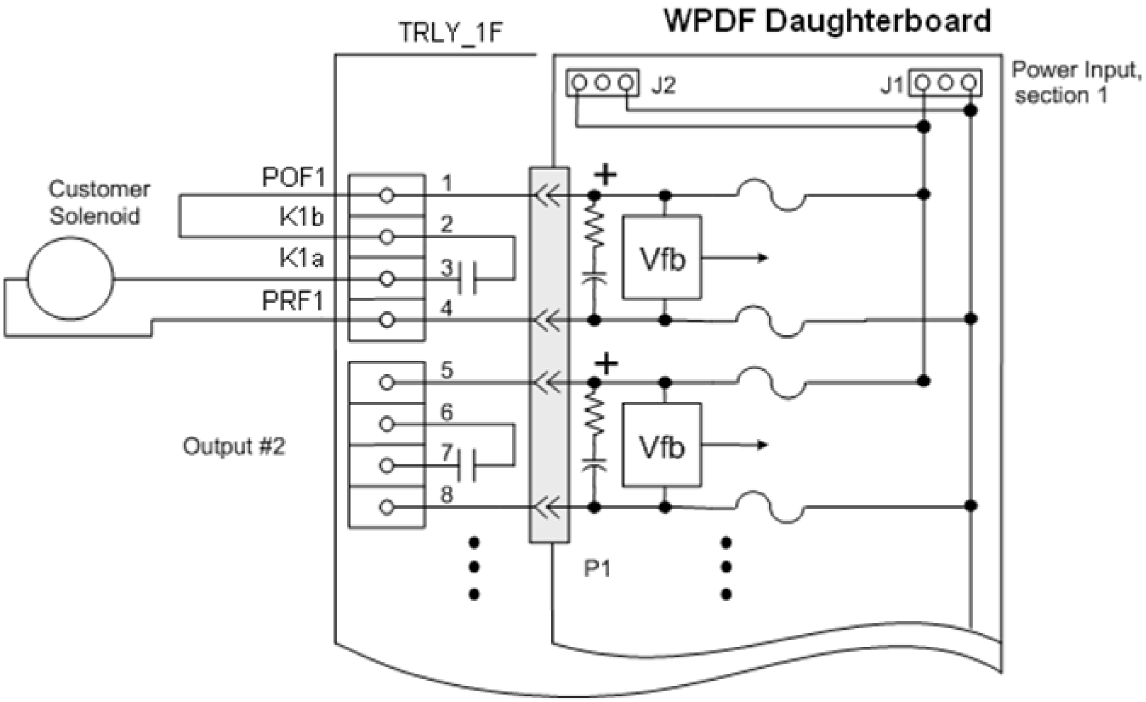
If using the optional WPDF power distribution board, mount it on top of the TRLY on the J1 and J2 connectors. Secure the WPDF to the TRLY by fastening a screw in the hole located at the center of WPDF. Connect the power for the two sections of the board on the three-pin connectors J1 and J4. Power can be daisy-chained out through the adjacent plugs, J2 and J3.

Note Refer to *GEH-6723, Mark VIeS Safety Control, Safety Instruction Guide* for restrictions when used with the Mark VIeS Safety control.



WPDF Power Distribution Board

The solenoids must be wired as displayed in the following figure. If the WPDF is not used, the customer must supply power to the solenoids.



Wiring to Solenoid using WPDF

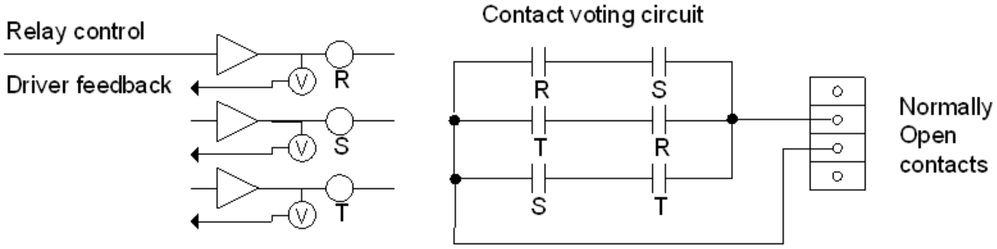
8.10.3 TRLY_F Operation

The 28 V dc power for the terminal board relay coils and logic comes from the three I/O packs connected at JR1, JS1, and JT1. The same relays are used for ac voltages and dc voltages. The TRLY_#F terminal board uses the same relays with differing circuits.

Relay drivers are mounted on the TRLY_#F and drive the relays at the frame rate. The relay outputs have a fail-safe feature that votes to de-energize the corresponding relay when a cable is unplugged or communication with the associated I/O pack is lost.

This board only supports TMR applications. The relay control signals are routed into TRLY_#F from the three I/O packs R, S, and T through plugs JR1, JS1, and JT1. These signals directly control the corresponding relay driver for each TMR section R, S, and T. Power for each section's relay coils comes in from its own I/O pack and is not shared with the other sections.

TRLY_#F features TMR contact voting. The relay contacts from R, S, and T are combined to form a voted Form A (NO) contact with TRLY_1F or a Form B (NC) output with TRLY_2F. 24/125 V dc or 115 V ac can be applied. The following figure displays the TMR voting contact circuit.

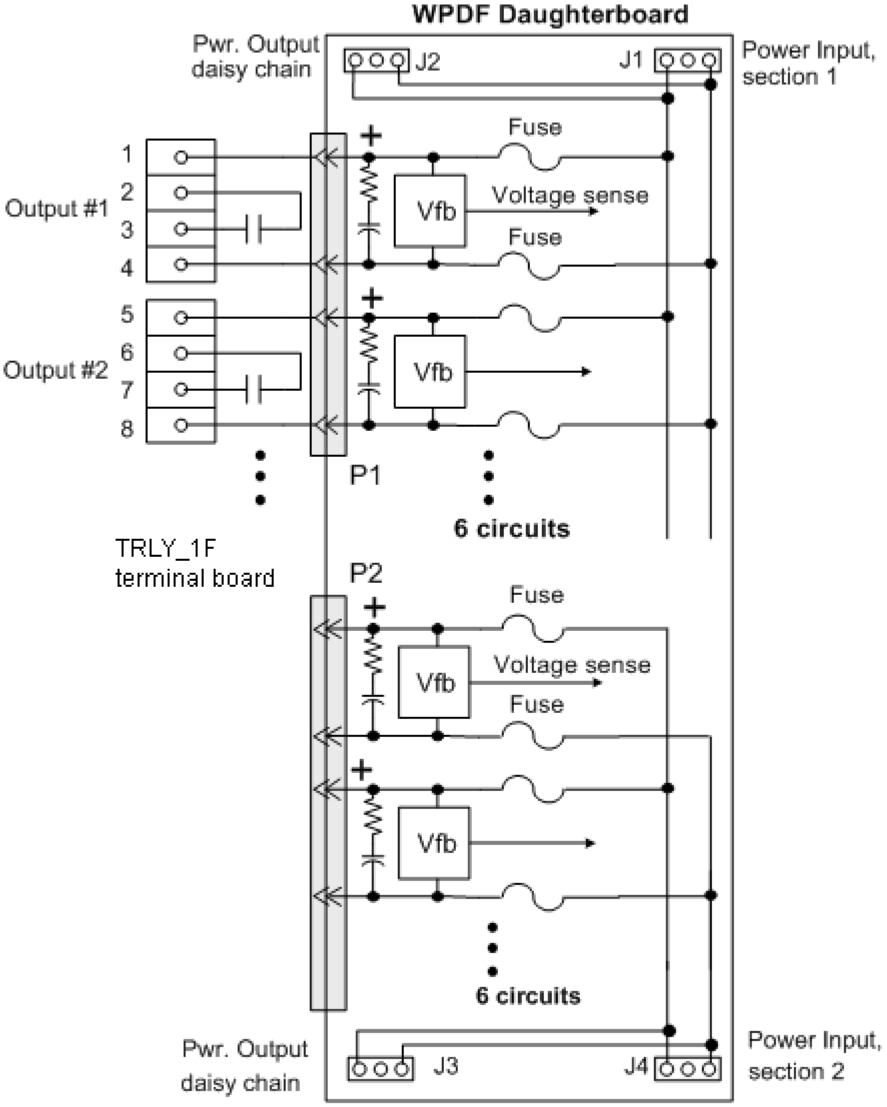


TRLY_1F Contact Arrangement for TMR Voting

8.10.3.1 Field Solenoid Power Option

The WPDFH1A daughterboard supplies power to the terminal board solenoids. The WPDF holds two power distribution circuits, which can be independently used for standard 125 V dc, 115 V ac, or 24 V dc sources. Each section consists of six fused branches that provide power to TRLY_#F. Each branch has its own voltage monitor across its secondary fuse pair. Each voltage detector is fanned to three independent open-collector drivers for feedback to each of the I/O pack R, S, and T. IS200WPDFH2A provides a single fuse in the high side (pin 1 of J1–J4) of each power distribution circuit for ac applications where a fuse in the neutral return wire (pin 3 of J1–J4) is not desirable).

The WPDF should not be used without the terminal board. Fused power flows through this board down to the terminal board points. The terminal board controls the fuse power feedback. The following figure displays the TRLY_#F/WPDF solenoid power circuit.



Solenoid Power Supply WPDF

Relationship Between Fuses and Terminals

Terminal	Name	Fuse
1	POF1	FU1
4	PRF1	FU13
5	POF2	FU2
8	PRF2	FU14
9	POF3	FU3
12	PRF3	FU15
13	POF4	FU4
16	PRF4	FU16
17	POF5	FU5
20	PRF5	FU17
21	POF6	FU6
24	PRF6	FU18
25	POF7	FU7
28	PRF7	FU19
29	POF8	FU8
32	PRF8	FU20
33	POF9	FU9
36	PRF9	FU21
37	POF10	FU10
40	PRF10	FU22
41	POF11	FU11
44	PRF11	FU23
45	POF12	FU12
48	PRF12	FU24

8.10.4 TRLY_F Specifications

Item	TRLY_#F Specification
Number of Output Relay Channels	12
Board Types	H1F, S1F: NO contacts
	H2F, S2F: NC contacts
Rated Voltage on Relays	Nominal 100/125 V dc or 24 V dc
	Nominal 115 V ac
Max Load Current	0.5/0.3 A resistive for 100/125 V dc operation
	5.0 A resistive for 24 V dc operation
	5.0 A resistive for 115 V ac
Max Response Time On	25 ms
Contact Life	Electrical operations: 100,000
Fault Detection	Coil Voltage disagreement with command Blown fuse indication (with WPDF power daughterboard) Unplugged cable or loss of communication with I/O pack; relays de-energize if communication with associated I/O pack is lost
Size	17.8 cm wide x 33.02 cm high (7.0 in x 13.0 in)
Technology	Surface-mount

Item	WPDF Solenoid Power Distribution Board Specification
Number of Power Distribution Circuits (PDC)	2: each rated 10 A, nominal 115 V ac or 125 V dci'm
Number of Fused Branches	12: six for each PDC
Fuse Rating	3.15 A at 25ºC (77 ºF) 2.36 A is the recommended maximum usage at 65ºC (149 ºF)
Voltage Monitor, Max Response Delay	60 ms typical
Voltage Monitor, Min Detection Voltage	16 V dc 72 V ac
Voltage Monitor, Max Current (Leakage)	3 mA
Size - WPDF	10.16 cm wide x 33.02 cm high (4.0 in x 13.0 in)
Technology	Surface-mount

8.10.5 TRLY_F Diagnostics

Diagnostic tests to components on the terminal boards are as follows:

- The voltage to each relay coil is monitored and checked against the command at the frame rate. If there is no agreement for five consecutive frames, an alarm is latched.
- The voltage across each solenoid power supply is monitored and if it goes below 16 V ac/dc, an alarm is created.
- If any one of the outputs goes unhealthy a composite diagnostic alarm, L3DIAG_xxxx occurs.
- Each terminal board connector has its own ID device that is interrogated by the I/O pack. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the JR1/JS1/JT1 connector location. When an ID chip is read by the I/O pack and a mismatch is encountered, a hardware incompatibility fault is created.

The diagnostic signals can be individually latched, and then reset with the RSTDIAG signal if they go healthy.

8.11 SRLYH#A, S#A Simplex Relay Output

The Simplex Relay Output (SRLY) terminal board is a simplex S-type terminal board accepting a PDOA or YDOA I/O pack and providing 12 form C relay output circuits through 48 customer terminals. The SRLY has the same physical size, customer terminal locations, and I/O pack mounting as other S-type terminal boards. There will be no components higher than an attached I/O pack, permitting double stacking of terminal boards. Each relay on SRLY uses an isolated contact pair as position feedback to the I/O pack.

The SRLY has two groups:

- IS200SRLY_1A has fixed Euro style box-type terminal blocks and no ability to accept option boards.
- IS200SRLY_2A has pluggable Euro style box-type terminal blocks and two connectors that accept a variety of different option boards.

There are three option boards available that plug onto SRLY_2A:

- IS200WROB turns SRLY into the functional equivalent of the TRLY_1B. This option provides fused and sensed power distribution to the first six relays and dedicated power to the last relay.
- IS200WROF puts a single fuse in series with each relay common connection. Fuse voltage feedback is included.
- IS200WROG distributes power from an input connector to each relay through a single fuse. Fuse voltage feedback is included.

Note When using WROB, WROF, or WROG, the incoming wetting voltage can be either ac or dc.

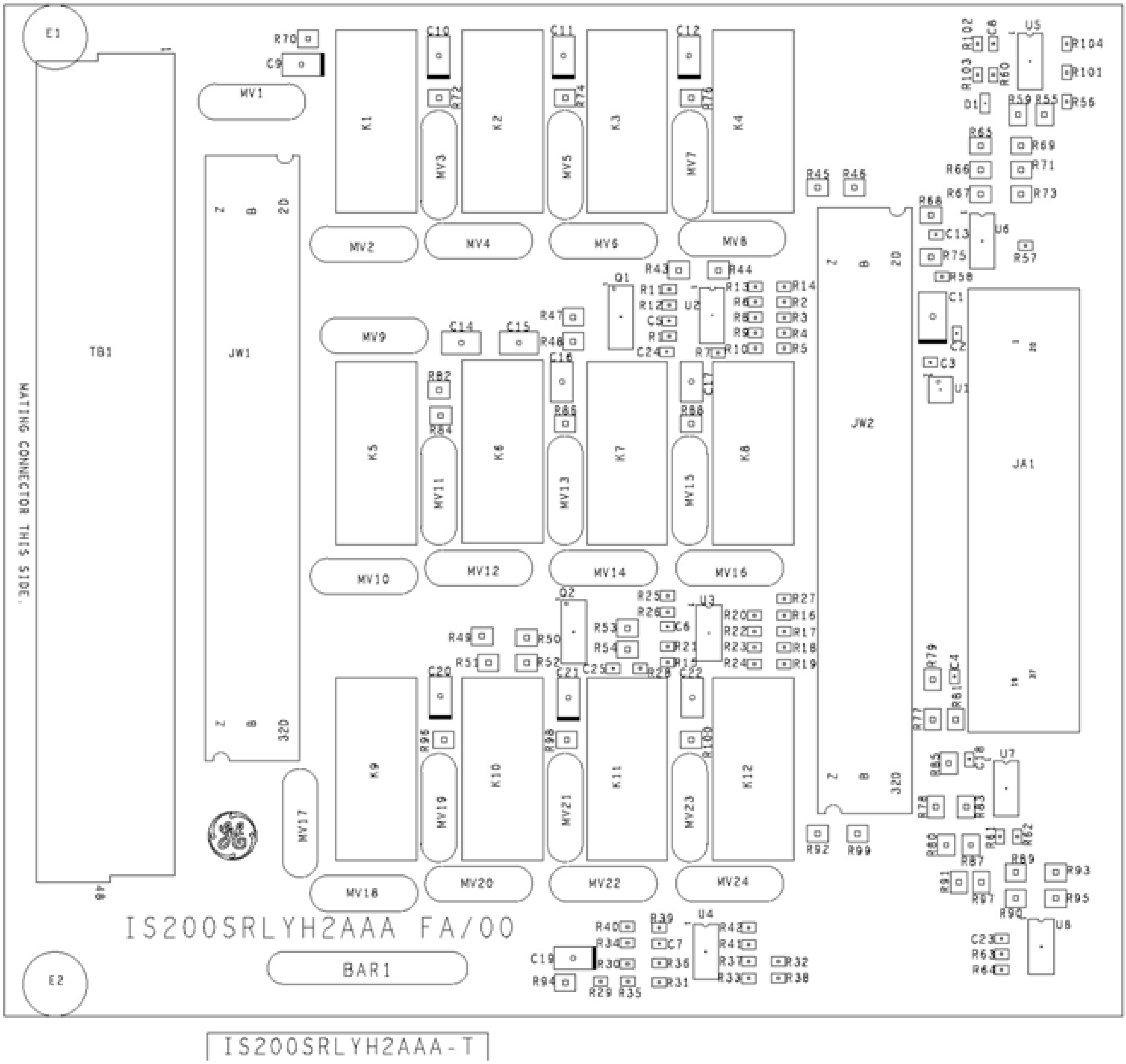
SRLY Compatibility

Revision	PDOA I/O Pack	YDOA I/O Pack	Comments
SRLYH1A	Yes, all versions	No	Fixed terminals
SRLYH2A	Yes, all versions	No	Pluggable terminals
SRLYH2A + WROB	Yes, all versions	No	Pluggable terminals, six dual-fused powered outputs, one unfused powered output.
SRLYH2A + WROF	Yes, all versions	No	Pluggable terminals, one fuse in series with each relay common terminal Can be used for feedback from 9 to 240 V ac or from 12 to 125 V dc
SRLYH2A + WROG	Yes, all versions	No	Pluggable terminals, twelve single-fused powered outputs Can be used for feedback from 9 to 240 V ac or from 12 to 125 V dc
SRLYS1A	Yes, all versions	Yes, all versions	Fixed terminals, IEC 61508 safety certified with YDOA
SRLYS2A	Yes, all versions	Yes, all versions	Pluggable terminals, IEC 61508 safety certified with YDOA
SRLYS2A + WROB	Yes, all versions	Yes	*
SRLYS2A + WROF	Yes, all versions	Yes	* Pluggable terminals, one fuse in series with each relay common terminal Can be used for feedback from 9 to 240 V ac or from 12 to 125 V dc
SRLYS2A + WROG	Yes, all versions	Yes	* Pluggable terminals, twelve single-fused powered outputs Can be used for feedback from 9 to 240 V ac or from 12 to 125 V dc
* Refer to *GEH-6723, Mark VIeS Safety Control, Safety Instruction Guide* for restrictions.			

8.11.1 Installation

SRLY and a plastic insulator mounts on a sheet metal carrier and is then mounted to a cabinet by screws. If an option board is used, it plugs onto SRLYH2A or SRLYS2A and is held in place by the force of the connectors.

- NC – normally closed contact of a form C relay
- COM – common point of a form C relay contact
- NO – normally open contact of a form C relay
- SOL – return circuit path for a solenoid that is powered by the relay board
- VSENSE – the input to a voltage sensor that looks between VSENSE and COM
- RETURN – return power path for devices powered by the WROG option



SRLY Terminal Board Layout

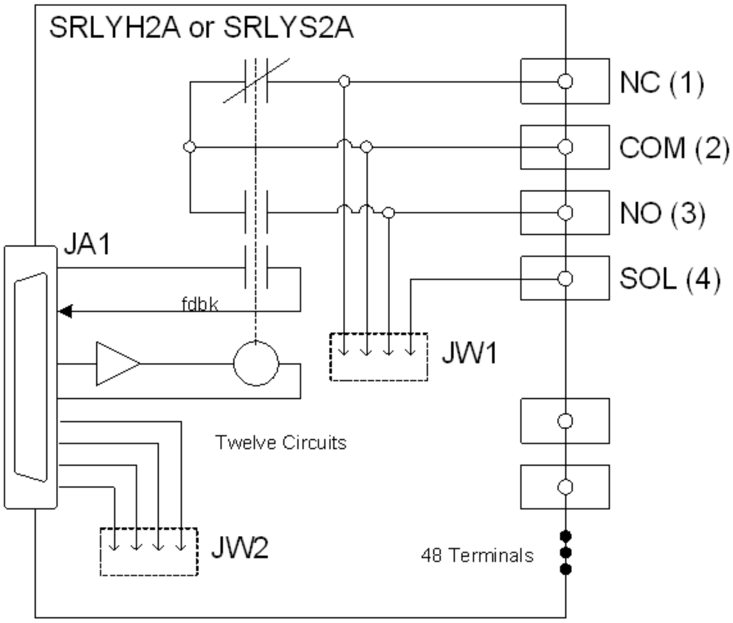
Function of Each Terminal Point as Related to an Option Board

Output Terminal	Relay	SRLY	SRLY + WROB	SRLY/WROF with Fuses	SRLY/WROF without Fuses	SRLY + WROG
1	1	NC	NC	NC	NC	NC
2		COM	COM	COM (unfused)	COM	POWER
3		NO	NO	NO	NO	NO
4			SOL	COM (fused)	VSENSE	RETURN
5	2	NC	NC	NC	NC	NC
6		COM	COM	COM (unfused)	COM	POWER
7		NO	NO	NO	NO	NO
8			SOL	COM (fused)	VSENSE	RETURN
9	3	NC	NC	NC	NC	NC
10		COM	COM	COM (unfused)	COM	POWER
11		NO	NO	NO	NO	NO
12			SOL	COM (fused)	VSENSE	RETURN
13	4	NC	NC	NC	NC	NC
14		COM	COM	COM (unfused)	COM	POWER
15		NO	NO	NO	NO	NO
16			SOL	COM (fused)	VSENSE	RETURN
17	5	NC	NC	NC	NC	NC
18		COM	COM	COM (unfused)	COM	POWER
19		NO	NO	NO	NO	NO
20			SOL	COM (fused)	VSENSE	RETURN
21	6	NC	NC	NC	NC	NC
22		COM	COM	COM (unfused)	COM	POWER
23		NO	NO	NO	NO	NO
24			SOL	COM (fused)	VSENSE	RETURN
25	7	NC	NC	NC	NC	NC
26		COM	COM	COM (unfused)	COM	POWER
27		NO	NO	NO	NO	NO
28				COM (fused)	VSENSE	RETURN
29	8	NC	NC	NC	NC	NC
30		COM	COM	COM (unfused)	COM	POWER
31		NO	NO	NO	NO	NO
32				COM (fused)	VSENSE	RETURN
33	9	NC	NC	NC	NC	NC
34		COM	COM	COM (unfused)	COM	POWER
35		NO	NO	NO	NO	NO
36				COM (fused)	VSENSE	RETURN
37	10	NC	NC	NC	NC	NC
38		COM	COM	COM (unfused)	COM	POWER
39		NO	NO	NO	NO	NO
40				COM (fused)	VSENSE	RETURN
41	11	NC	NC	NC	NC	NC
42		COM	COM	COM (unfused)	COM	POWER
43		NO	NO	NO	NO	NO
44				COM (fused)	VSENSE	RETURN
45	12	NC	NC	NC	NC	NC
46		COM	COM	COM (unfused)	COM	POWER
47		NO	NO	NO	NO	NO
48			SOL	COM (fused)	VSENSE	RETURN

8.11.2 Operation

8.11.2.1 Board Groups

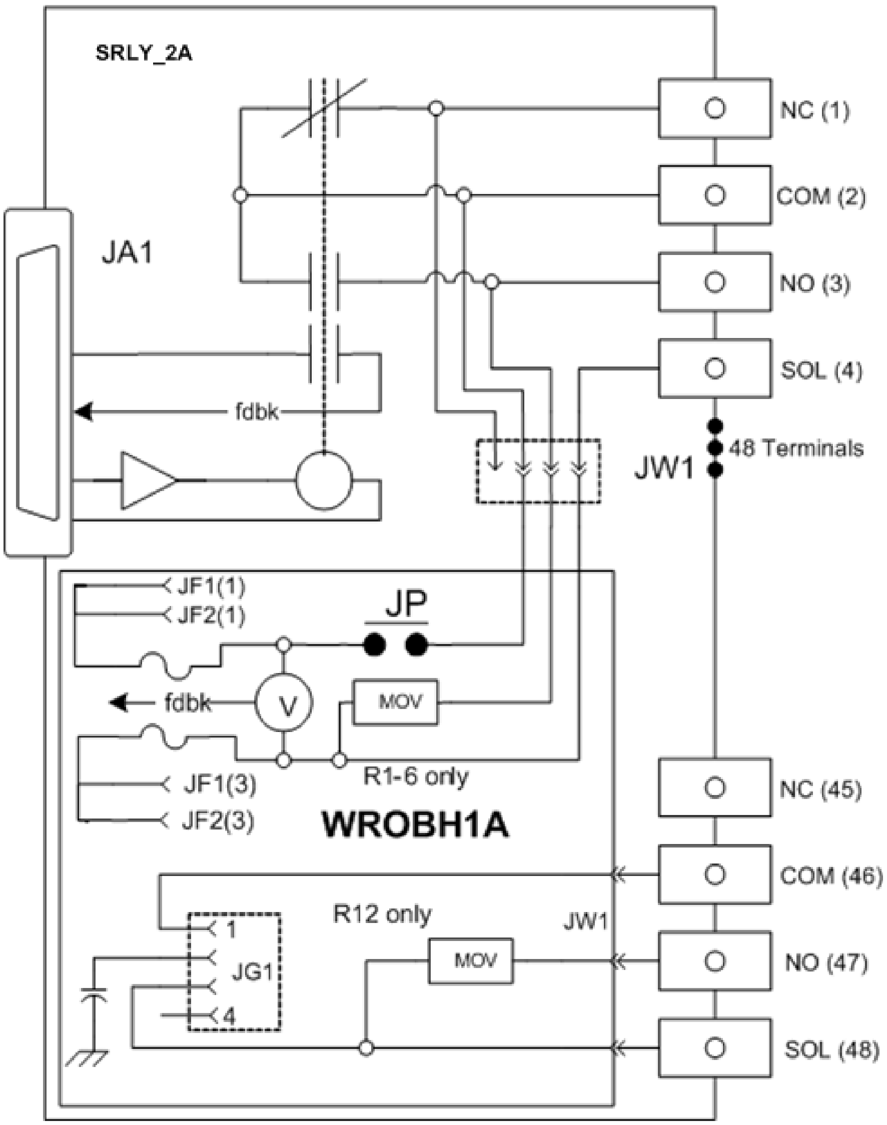
The SRLY is available in two groups. The SRLY_1A comes with fixed box terminals and omits option board connectors JW1 and JW2. The SRLY_2A uses pluggable type terminals and has connectors JW1 and JW2 supporting option board connection. Electrically, the SRLY_2A has the following circuit for each of the 12 relays:



Without an option board, the SOL terminal associated with each relay has no connection. SRLY is designed to support a current rating of 5 A and voltage clearance greater than is needed for 250 V ac on all customer screw and JW1 circuits. The relay rating is the limiting item for each application.

8.11.2.2 SRLY + WROB

Option board IS200WROBH1A adds capability to the SRLY_2A to yield a combination that has the same functionality as the TRLY_1B terminal board when used simplex. Included are fused sensed power distribution to the first six relays and dedicated power to the last relay. Electrically, the SRLY_2A plus IS200WROBH1 together have the circuitry displayed in the following figure. IS200WROBH1 has default fuse values of 3.15 A. Connector JW2 and its connections to JA1 are omitted for clarity.



SRLY_2A + WROB Circuitry

Both sides of the power distribution on relays 1-6 are fused allowing the board to be used in systems where dc power is floating with respect to earth. Fuse voltage feedback is compatible with 24 V, 48 V, and 125 V dc applications as well as 120 V and 240 V ac applications.

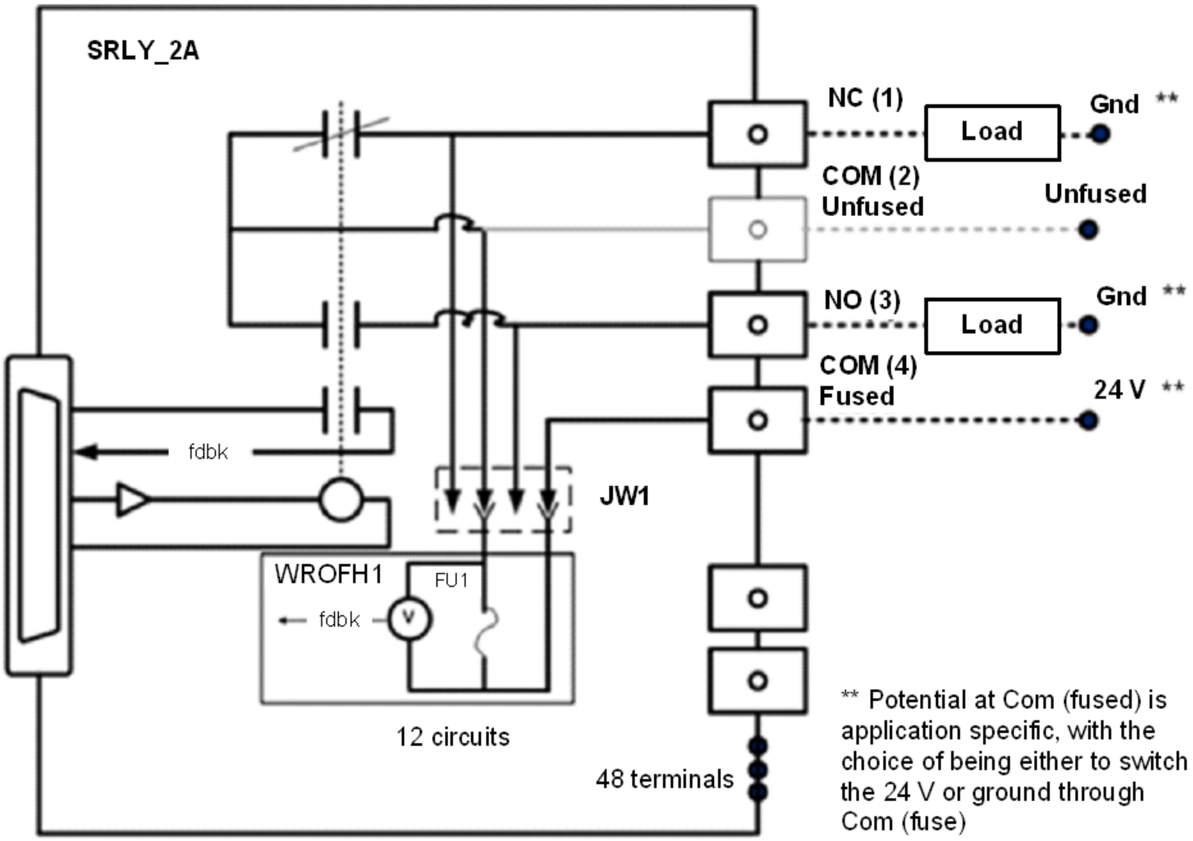
The following table lists the relationship between fuses, jumpers, relays, and terminals.

Relay	+Fuse	-Fuse	Jumper	Terminals
1	FU7	FU1	JP1	1-4
2	FU8	FU2	JP2	5-8
3	FU9	FU3	JP3	9-12
4	FU10	FU4	JP4	13-16
5	FU11	FU5	JP5	17-20
6	FU12	FU6	JP6	21-24

8.11.2.3 SRLY + WROF Fused in Series

Option board IS200WROFH1A adds an optional fuse in series with the COM connection for each relay by using the SOL terminal in place of COM. Isolated voltage sensing that is not polarity sensitive is provided for each fuse. Refer to the *SRLY Compatibility* table for compatible applications. IS200WROFH1 has default fuse values of 3.15 A.

With the original application for this board, each relay output has a fuse in series with power applied from an external source. In the following figure, connector JW2 and its connections to JA1 are omitted for clarity. Fuses FU1 through FU12 are associated with relay circuits 1 through 12 respectively.

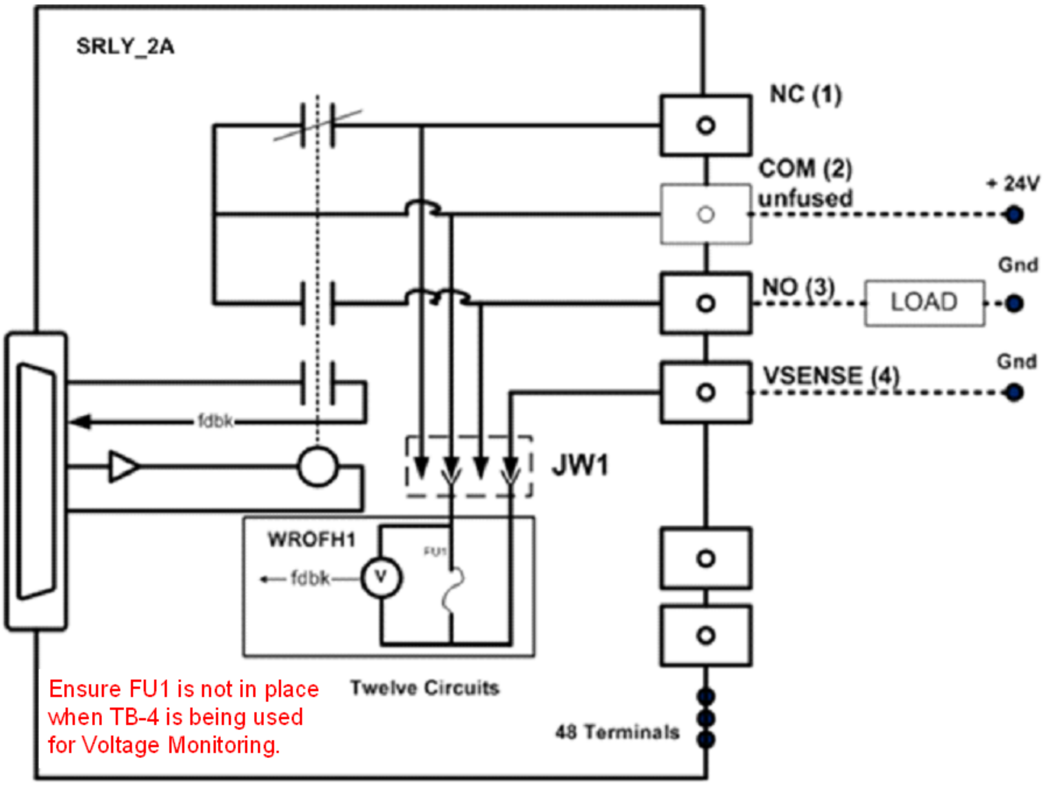

SRLY_2A
NC (1)
Load
Gnd **
COM (2)
Unfused
Unfused
NO (3)
Load
Gnd **
COM (4)
Fused
24 V **
fdbk
JW1
WROFH1
FU1
fdbk
V
12 circuits
48 terminals
** Potential at Com (fused) is application specific, with the choice of being either to switch the 24 V or ground through Com (fuse)

Fused in Series

8.11.2.4 SRLY + WROF Isolated Contact Voltage Feedback

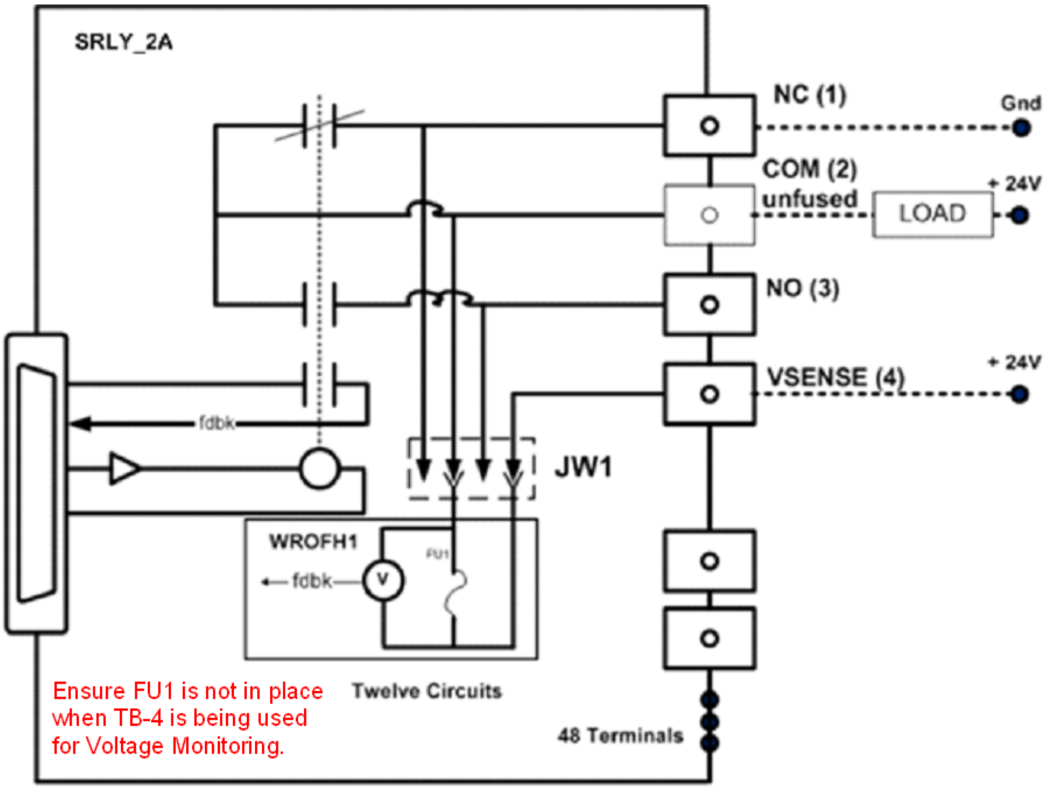
With the alternate application of this board, if the fuse is removed from a circuit, the isolated voltage detector remains. The fourth terminal may now be wired to either the NC or NO terminal to provide isolated contact voltage feedback. I/O pack firmware has a configuration option to turn off fuse blown alarm generation for a given relay if it is being used in this fashion.

Note Refer to the section, *Installation*. The fourth screw is Vsense.



Normally Open

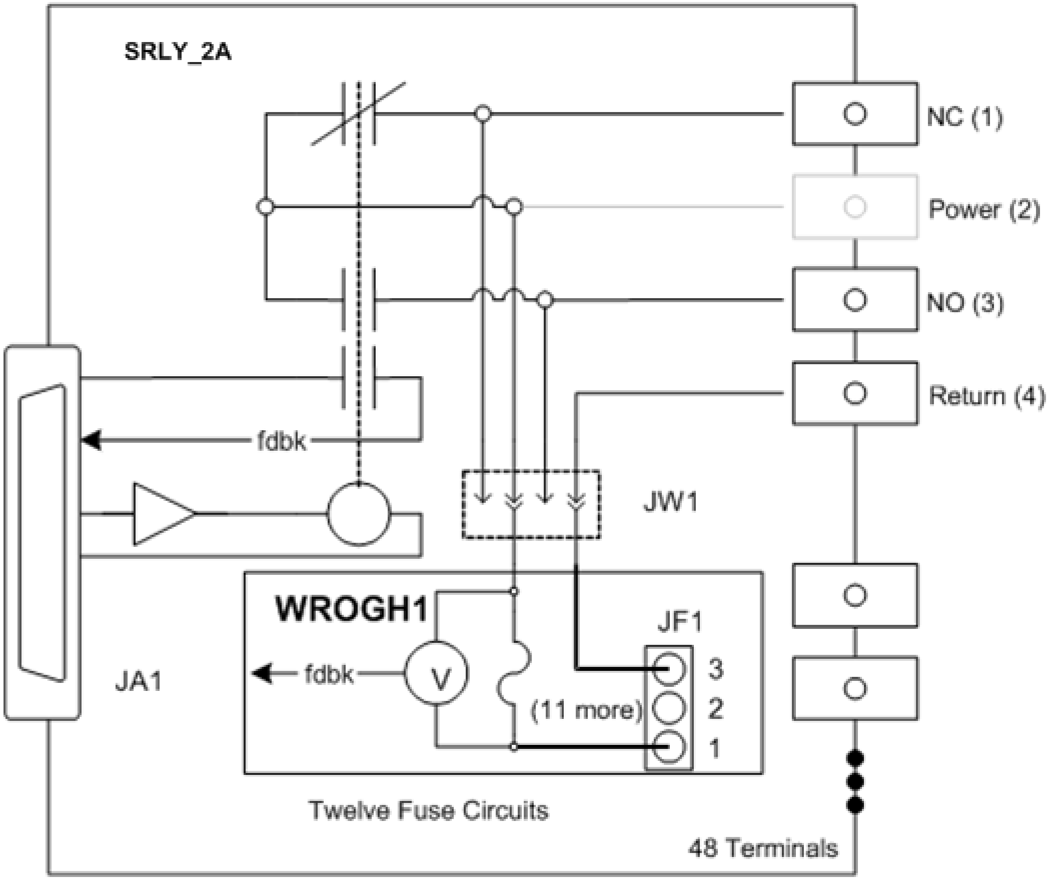
Note These connections are application specific and can be connected in either the normally open or normally closed way.



Normally Closed

8.11.2.5 SRLY + WROG

Option board IS200WROGH1A adds fused power distribution for all twelve relays. Isolated voltage sensing that is not polarity sensitive is provided for each fuse. Refer to the *SRLY Compatibility* table for compatible applications. IS200WROGH1 has default fuse values of 3.15 A. Electrically, SRLY_2A plus IS200WROGH1 together have circuitry displayed in the following figure. Fuses FU1 through FU12 are associated with relay circuits 1 through 12 respectively. Connector JW2 and its connections to JA1 are omitted for clarity.



SRLY_2A + WROG Circuitry

8.11.3 Specifications

Item	SRLY Specification
Number of Relay Channels on One SRLY Board	12
Rated Voltage on Relays	Nominal 24 V dc, 48 V dc, or 125 V dc Nominal 120 V ac or 240 V ac
Max Load Current	0.6 A for 125 V dc operation 1.2 A for 48 V dc operation 3.15 A for 24 V dc operation 3.15 A for 120/240 V ac, 50/60 Hz operation
Max Response Time On	25 ms typical
Max Response Time Off	25 ms typical
Contact Material	Silver cad-oxide
Contact Life	Electrical operations: 100,000 Mechanical operations: 10,000,000
Fault Detection	Relay position feedback using contact pair separate from load contacts.
Size	15.9 cm high x 17.8 cm wide (6.25 in x 7.0 in)
WROBH1 Option Board	
Powered Output Circuits	6 fused, associated with relays 1-6, fed from parallel connectors JF1 and JF2. Both sides of the power source are fused for each output. 1 unfused, associated with relay 12, fed from connector JG1
WROFH1 Option Board	
Fused Output Circuits	12 fused circuits, one per relay
WROGH1 Option Board	
Powered Output Circuits	12 fused circuits, one associated with each relay. Single side fusing of the power is associated with the power input on JF1 pin 1. Return power path through JF1pin 3 is not fused.

8.11.4 Diagnostics

Terminal board connectors have their own ID device that is interrogated by the I/O pack. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and plug location. When the chip is read by PDOA and a mismatch is encountered, a hardware incompatibility fault is created. Each of the option boards also contains an ID device that uniquely identifies the board.

The SRLY provides diagnostic feedback to PDOA indicating each relay position by monitoring an isolated set of contacts on each relay. When WROB is used with SRLY, isolated voltage feedback is used to detect fuse status for the six fuse pairs on the board. The solenoid excitation is monitored downstream of the fuses and an alarm is latched if it falls below 9 V dc.

When WROF is used with SRLY, isolated voltage feedback is used to monitor each fuse. If voltage is present and the fuse is open a diagnostic alarm is generated. This alarm can be disabled in the ToolboxST application for PDOA configuration to use the feedback circuit without the fuse. When WROG is used with SRLY, isolated voltage feedback is used to monitor each fuse. If voltage is present and the fuse is open, a diagnostic alarm is generated.

8.11.5 Configuration

There are no jumpers associated with the SRLY terminal board.

Option board WROBH1 includes six jumpers that are used to apply or remove power from a relay. Boards are produced with all six jumpers in place. The jumper is removed from the board when a relay is to be used as dry contacts and power distribution is not desired.

There are no jumpers associated with the WROFH1 board. For each relay the inclusion or exclusion of a series fuse is determined by the terminal point used as the relay common. In addition for each relay the associated WROF fuse may be removed to allow direct use of the fuse voltage sensing circuit as a voltage detector.

There are no jumpers associated with the WROGH1 board.

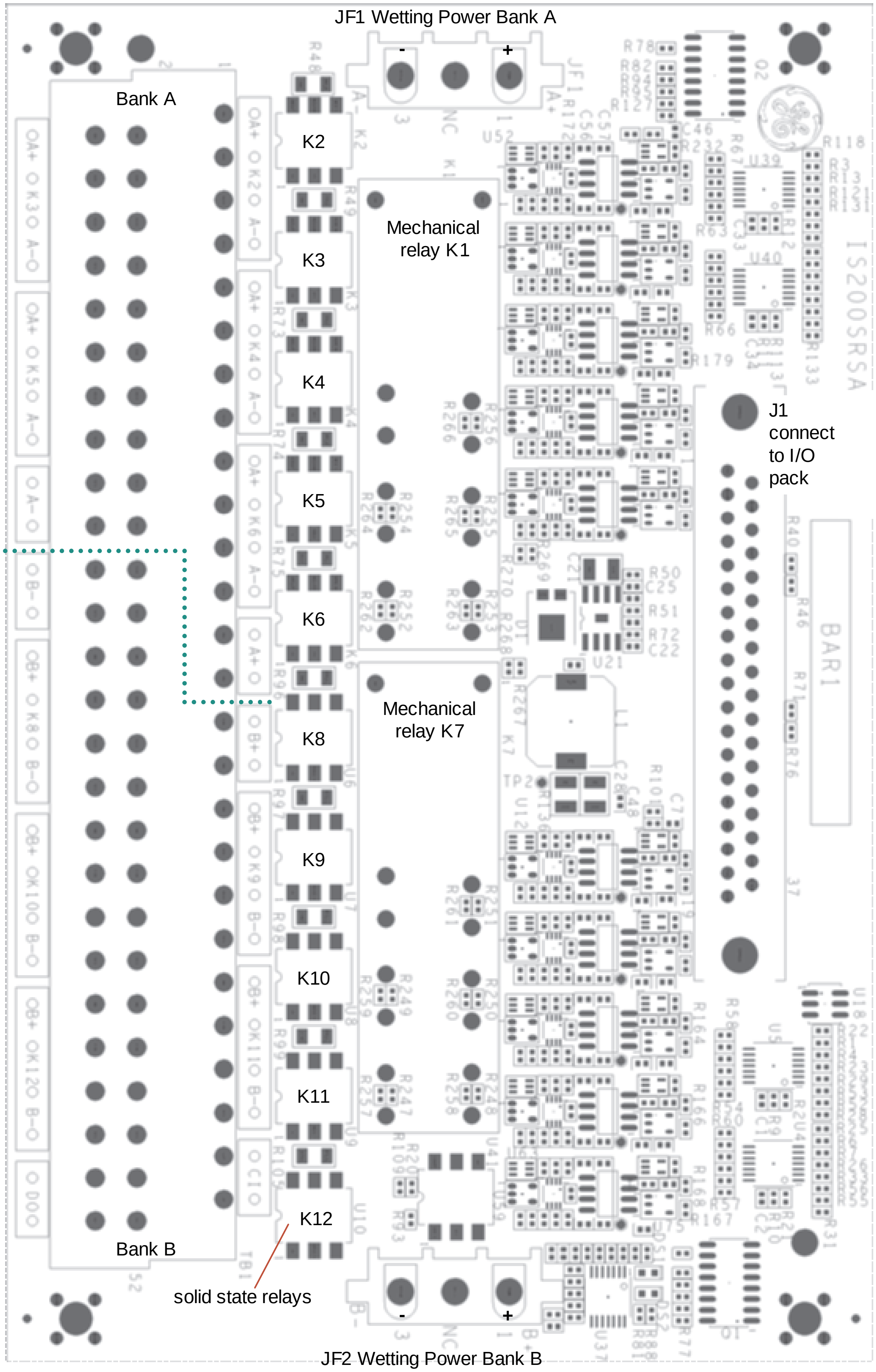
8.12 SRSA Compact Digital Output

The SRSA is a simplex S-type terminal board that accepts a single YDOA I/O pack and provides 10 relay outputs (grouped as 5 per bank). Its compact design enables use in applications where space constraints are a concern. Physical characteristics include:

- Dimensions of 15.9 cm length (6.25 in) x 10.2 cm width (4.0 in) x 4.3 cm (1.7 in) thickness
- 4 mounting holes (corners of the board) are 0.156 mm diameter each

The following is information on three SRSA board versions. For hardware availability, contact the nearest GE Sales or Service Office, or an authorized GE Sales Representative.

Board Revision	**Terminal Block (TB1)**	**Wetting Power Connectors (JF1, JF2)**	**Mechanical Relays (K1, K7)**
SRSAH1A	Yes	Yes	Yes
SRSAS1A ‡	Yes	Yes	Yes
SRSAH2A	Yes	Yes	No
SRSAS3A ‡	No	No	Yes
‡ Compatible with YDOAS1B firmware V05.00 or later. Compatible with the YDOAS1A firmware V04.11.			


JF1 Wetting Power Bank A
-
+
Bank A
K2
K3
K4
K5
K6
Mechanical relay K1
J1 connect to I/O pack
Mechanical relay K7
K8
K9
K10
K11
K12
Bank B
solid state relays
-
+
JF2 Wetting Power Bank B

8.12.1 Specifications

Item	SRSA Specification
Number of Relay Channels	Two banks of 5 channels each, for 10 total relay channels
Rated Voltage on Relays	Nominal 28 V dc or 24 V dc
Max Load Current	1.5 A per channel, 6 A max per bank
Max Response Time On	Solid State Relays 5.0 ms typical
	Mechanical relays 15 ms typical
Max Response Time Off	Solid State Relays 0.5 ms typical
	Mechanical relays 16 ms typical
Max Inrush Current	5 A for 100 ms, non-repetitive
Contact Material	Silver alloy
Contact Life for Mechanical Relay	Solid state operations: 2,000,000 at 1.5 A (resistive)
	Mechanical operations: 250,000 at 1.5 A (resistive)
Solid State Relay Feedback Current Detection Threshold	< 50 mA guaranteed, < 35 mA typical, no hysteresis
Terminal to Terminal Resistance	< 0.25 Ω max, < 0.15 Ω typical
Wetting Connections	JF1 for power bank A, unfused JF2 for power bank B, unfused
Fault Detection	Loss of coil power
	Coil current disagreement with command
	Relays de-energize if communication with YDOA is lost
Size	Length 15.9 cm (6.25 inches) x width 10.2 cm (4.0 inches) x thickness 4.3 cm (1.7 inches)

8.12.2 Installation

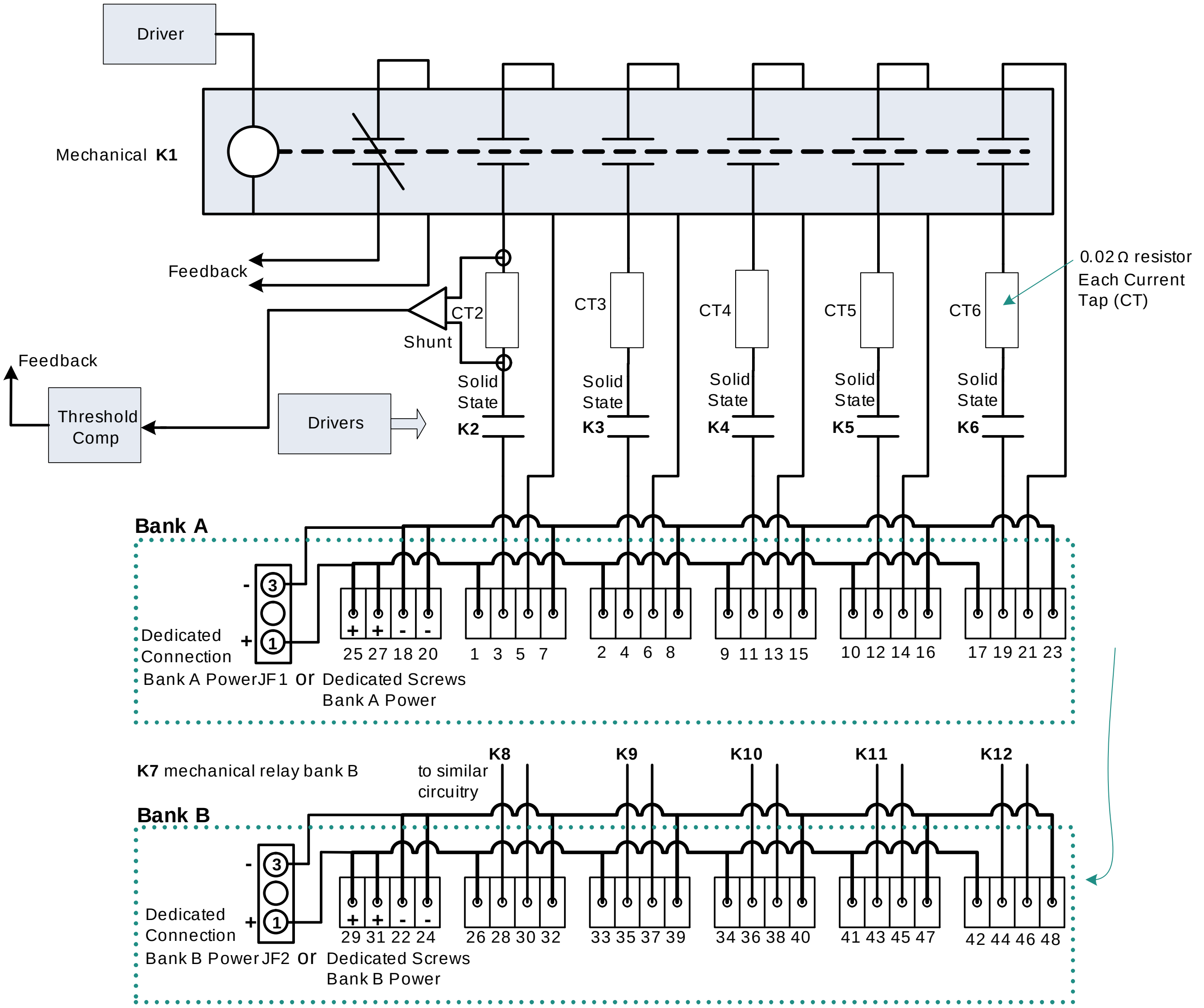
The SRSA and a plastic insulator mount on a sheet metal carrier and are then mounted to a cabinet by screws. The SRSA receives P28 system power from the I/O pack. The SRSA_1A and 2A include a removable euro-style box terminal block. The SRSAS3A does not include a terminal block, therefore field wiring is soldered to the board.

Field Wire Connections

#	Signal	Description	#	Signal	Description
1	PWRA2_P	K2 Power Input A Positive	2	PWRA3_P	K3 Power Input A Positive
3	NO2	K2 Normally Open Contact	4	NO3	K3 Normally Open Contact
5	COM2	K2 Return	6	COM3	K3 Return
7	PWRA2_N	K2 Power Input A Negative	8	PWRA3_N	K3 Power Input A Negative
9	PWRA4_P	K4 Power Input A Positive	10	PWRA5_P	K5 Power Input A Positive
11	NO4	K4 Normally Open Contact	12	NO5	K5 Normally Open Contact
13	COM4	K4 Return	14	COM4	K5 Return
15	PWRA4_N	K4 Power Input Bank A Negative	16	PWRA5_N	K5 Power Input Bank A Negative
17	PWRA6_P	K6 Power Input Bank A Positive	18	PWRA_N1	Dedicated Power Input Bank A Negative
19	NO6	K6 Normally Open Contact	20	PWRA_N2	Dedicated Power Input Bank A Negative
21	COM6	K6 Return	22	PWRB_N1	Dedicated Power Input Bank B Negative
23	PWRA6_N	K6 Power Input A Negative	24	PWRB_N2	Dedicated Power Input Bank B Negative
25	PWRA_P1	Dedicated Power Input Bank A Positive	26	PWRB8_P	K8 Power Input Bank B Positive
27	PWRA_P2	Dedicated Power Input Bank A Positive	28	NO8	K8 Normally Open Contact
29	PWRB_P1	Dedicated Power Input Bank B Positive	30	COM8	K8 Return
31	PWRB_P2	Dedicated Power Input Bank B Positive	32	PWRB8_N	K8 Power Input Bank B Negative
33	PWRB9_P	K9 Power Input Bank B Positive	34	PWRB10_P	K10 Power Input Bank B Positive
35	NO9	K9 Normally Open Contact	36	NO10	K10 Normally Open Contact
37	COM9	K9 Return	38	COM10	K10 Return
39	PWRB9_N	K9 Power Input Bank B Negative	40	PWRB10_N	K10 Power Input Bank B Negative
41	PWRB11_P	K11 Power Input Bank B Positive	42	PWRB12_P	K12 Power Input Bank B Positive
43	NO11	K11 Normally Open Contact	44	NO12	K12 Normally Open Contact
45	COM11	K11 Return	46	COM12	K12 Return
47	PWRB11_N	K11 Power Input Bank B Negative	48	PWRB12_N	K12 Power Input Bank B Negative
49	RFU1	Reserved for future use	50	NC	No Connection
51	RFU2	Reserved for future use	52	RFU3	Reserved for future use

8.12.3 Operation

The SRSA provides 10 relay channels, grouped as bank A and bank B. Each bank contains 5 outputs as a series combination of *force-guided* relay contacts and a solid state relay. The primary disconnect operation should use solid state relays. Mechanical relays are provided for redundancy and safety purposes.



8.12.4 Diagnostics

Terminal board connectors have their own ID device that is interrogated by the I/O pack. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and plug location. When the chip is read by YDOA and a mismatch is encountered, a hardware incompatibility fault is created. Each of the option boards also contains an ID device that uniquely identifies the board. The SRSA provides diagnostic feedback to YDOA indicating relay current of solid state relays.

9 PFFA FOUNDATION Fieldbus Linking Device

The Mark* VIe FOUNDATION Fieldbus™ linking device (PFFA) is used to interconnect H1 fieldbus networks and segments to FOUNDATION high-speed Ethernet (HSE) to create a larger system and provides a standardized communications and controls system for installing components from various manufacturers. The PFFA is designed in accordance with class 42c of the FOUNDATION HSE profile. There are two platforms, H1B and H1A; however, H1A is obsolete and any new orders must use PFFAH1B.

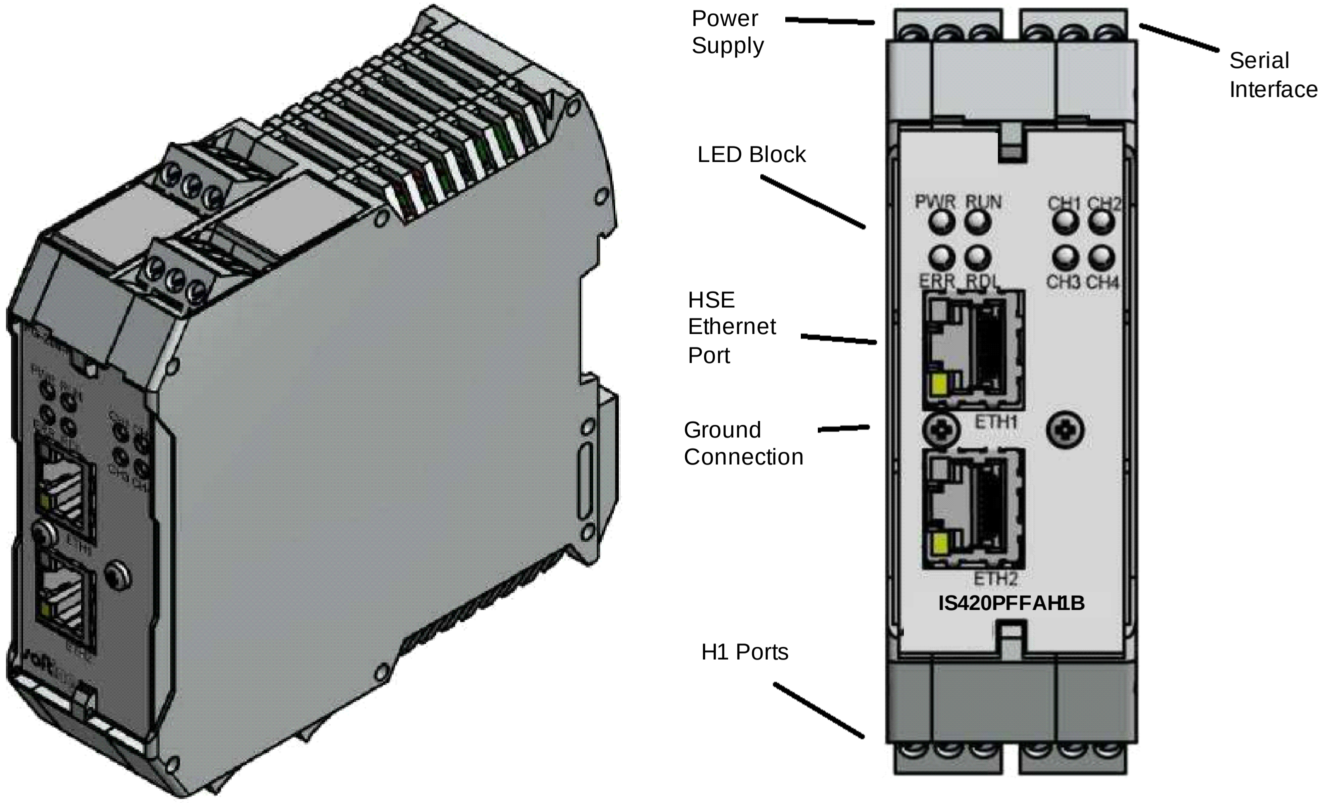
9.1 PFFAH1B Linking Device

The PFFAH1B linking device operates on 24 V dc and provides the following:

- One serial communications connector for redundant operation
- One LAN port for HSE subnet connection
- Four fieldbus H1 ports, each supporting 16 FF-H1 field devices

Two separate screw connections are provided for grounding in addition to the ground wire that is required as part of the power supply connection. The linking device serves as a gateway between the HSE and four onboard ports. For each of the ports, the linking device operates as the Link Master (LM) and as the system management (SM) time publisher. The linking device supports Hot Backup operation, it is fanless, and its compact size allows it to be used in a DIN-rail assembly.

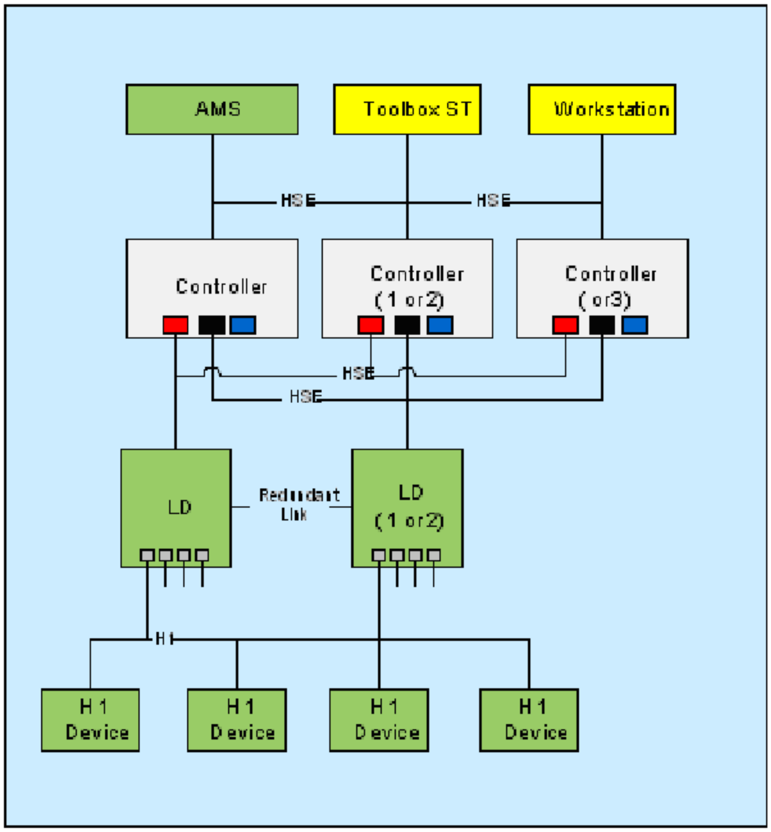
The linking device sends processed data from one H1 link to another H1 link, and sends and receives data from the H1 link to the HSE. It also provides access to the components attached to the H1 links for configuration and identification, including access to the component function blocks.



PFFAH1B Linking Device

9.1.1 PFFAH1B Functionality

A PFFAH1B linking device is used to interconnect 31.25 kilobits/sec fieldbuses and make them accessible to an HSE backbone running at 100 megabits/sec or 1 gigabit/sec. It acts as the gateway between the FOUNDATION fieldbus HSE subnet and FOUNDATION fieldbus H1 links and supports device redundancy.



Basic FOUNDATION Fieldbus Layout

PFFAH1B Linking Device functionality includes the following:

- Gateway between an Ethernet (HSE) port and four fieldbus (H1) ports
- Supports up to 16 field devices per segment
- Supports up to four separate H1 links. In each of these links, the Linking Device operates as the Link Master and the System Management (SM) Time Publisher.
- Identification of the devices connected to the H1 links
- Configuration of the connected H1 devices by System Management and Network Management through HSE
- Access to the function blocks of the connected H1 devices through HSE
- Republishing of process data from one H1 link to another
- Republishing of process data from H1 to HSE and vice versa

Note For a full description of terms and additional details, refer to the *Mark VIe Control FOUNDATION Fieldbus Interface Application Guide* (GEH-6761) or the Fieldbus FOUNDATION's documentation.

HSE subnet functions include:

- System Management Agent
- Network Management Agent
- Server providing object access to H1 devices
- Publishing/subscribing of process data from/to H1 components

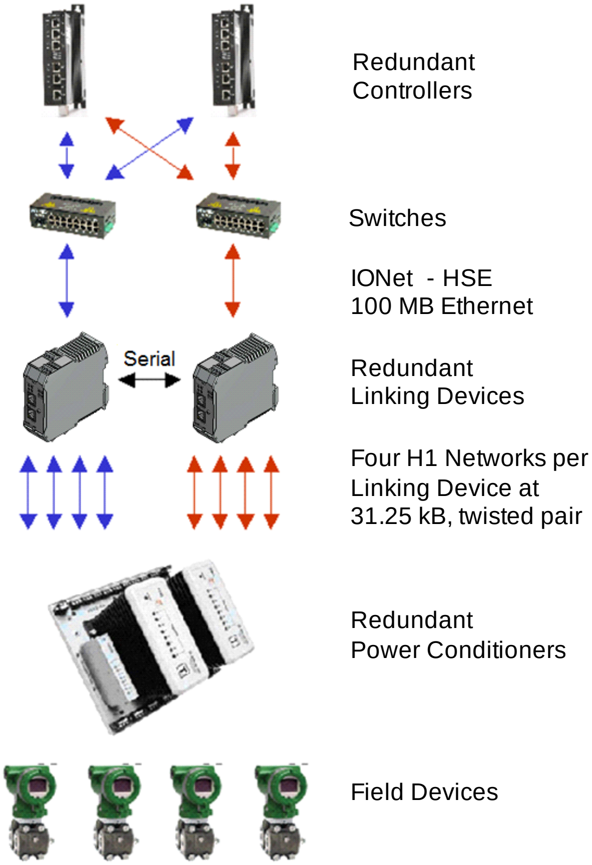
H1 link functions include:

- System Management Manager
- Network Management Manager
- Client for object access to H1 components
- Publisher and subscriber of process data
- Link Master, SM Time Publisher

9.1.2 Compatibility

The PFFAH1B linking device supports Simplex and Hot Backup redundant operations. In Hot Backup mode, two physical linking devices are connected by a serial connector to form one logical linking device (redundant set). Redundancy control information is shared over the serial redundancy connector. One linking device operates as the Primary device while the other operates as the Secondary device. In a redundant set, both linking devices are connected to the same H1 components and HSE subnet. The PFFAH1B linking device is compatible with Mark VIe I/O packs and controllers available in the ToolboxST application V07.01 or later.

To ensure continuity and continuous operation, the Secondary device automatically takes over if the Primary device fails. When the failed linking device is replaced, it is automatically configured to match the now Primary device and to take over as the Secondary device in the redundant set. If an H1 segment connector gets disconnected from the Primary linking device it switches roles to the Secondary linking device only if there are two or more H1 devices on the segment. If there is not a device, or if there is only one, the linking device does not switch roles.



PFFAH1B Redundant Linking Devices and Power Conditioners

Backwards Compatibility with PFFAH1A

The PFFAH1B is functionally equivalent and backwards compatible with the PFFAH1A. However, a PFFAH1A and a PFFAH1B cannot be combined to form a Hot Backup redundant set due to different serial connectors. When replacing a PFFAH1A with a PFFAH1B, both devices in a Hot Backup set must be replaced at the same time.

9.1.3 PFFAH1B Specifications

Item	PFFAH1B Specification
Power Supply	18 – 32 V dc
Power Consumption	Typical: 200 mA Max: 1 A (considering the in-rush current at switch-on)
Dimensions	36 x 108 x 111 mm (1.39 x 4.23 x 4.34 in)
Ambient Rating for Enclosure Design†	0 to 55°C (32 to 131 °F)
Ethernet Interface	1 – Ethernet 10Base-T/100Base-TX, RJ-45 port *ETH2 is currently not supported*
Ethernet Transfer Rate	10 mbps or 100 mbps (auto-sensing)
H1 Fieldbus Interface	4 – FF H1 3-pole screw terminals (pluggable), transformer coupling ports
H1 Fieldbus Transfer Rate	31.25 kbps
Serial Interface	1 – TX/RX/GND Cable

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

9.1.4 Installation and Troubleshooting

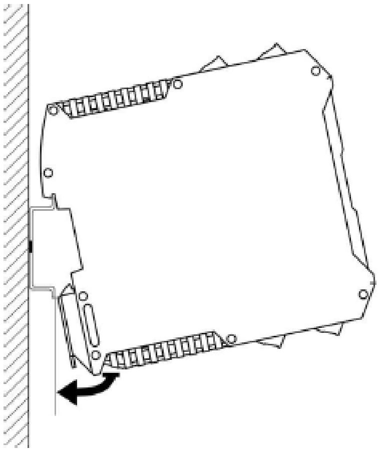
9.1.4.1 PFFAH1B Mounting and Installation

Warning

This equipment contains a potential hazard of electric shock, burn, or death. Ensure that all Lockout/Tag Out (LOTO) procedures are followed prior to replacing terminal boards. Only personnel who are adequately trained and thoroughly familiar with the equipment and the instructions should install, operate, or maintain this equipment.

➢ **To mount and install the PFFAH1B linking device**

1. Securely mount the linking device. On a DIN-rail (35 mm), attach the two upper notches to the rail. Press the linking device down towards the rail until it locks into place.



PFFAH1B DIN-rail Mounting

2. Connect the H1 links to the H1 ports.

Note The linking device does not provide power to the H1 links, so a power supply, power conditioner, and a bus termination must be provided for each link.

3. Connect the LAN port to an Ethernet switch or hub.
4. Connect a 24 V dc power supply to the linking device.
5. Turn on the power supply. The startup process takes ~50 seconds. Refer to the section *PFFAH1B LEDs* for indication of proper operation.
6. Configure the PFFAH1B using the ToolboxST application. Refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703), the chapter *Mark VIe FOUNDATION Fieldbus Interface*, the section *Configuration*.

➢ **To dismount the PFFAH1B linking device:** slide a screw driver horizontally underneath the housing into the locking bar, and slide the bar downwards without tilting the screw driver, then fold the device upwards.

9.1.4.2 Adding a Second Linking Device for Hot Backup

One linking device operates as a Primary with no backup. Add a second linking device to form a redundant set and provide failure protection to the H1 links connected to the linking device.

➢ To add a second linking device to form a redundant set

1. From the ToolboxST *Add Module Wizard* or *Modify Module* (if PFFA module is already added) dialog box, change the *I/O Pack Module Redundancy* selection to **HotBackup**. Add the new linking device's Device ID to the Mark VIe controller, then download to the controller to assign the IP address and subnet mask to the linking device. Follow the ToolboxST prompts to complete the download. Refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703), the chapter *Mark VIe FOUNDATION Fieldbus Interface*, the section *Configuration*.
2. Securely *mount* the PFFAH1B linking device.
3. Connect the H1 links, ensuring they are installed on the same port (FF 1, FF 2, FF 3, or FF 4) on both linking devices.
4. Connect the second linking device to an Ethernet switch or hub different than the one to which the Primary linking device is connected.
5. Connect the serial ports of both linking devices with the serial connector cable.
6. Connect a 24 V dc power supply to the second linking device. Use a separate or redundant power supply.
7. Turn on the power supply to the second linking device. The boot process takes ~50 seconds. The configuration of the Primary device is copied to the new device and it takes the role of Secondary device in the redundant set. Refer to the table *Device Status Indications* in the section *PFFAH1B LEDs* for indication of proper operation.
8. Configure PFFAH1B linking device redundancy using the ToolboxST application.

9.1.4.3 Power On and Start Up Troubleshooting

Similar to other I/O packs, the PFFAH1B uses DHCP to get an IP address assigned from the controller. The first three octets of the IP address are the subnet of the controller's IONet that the PFFAH1B is connected on, and the last octet is the module ID of the PFFAH1B. This IP address gets assigned by the controller every time the PFFAH1B is powered on.

For a redundant set in a Simplex configuration, the Linking Device that is powered on first operates as the Primary device. If both linking devices are powered on at the same time, the one with the lower IP address operates as the Primary device. If both linking devices in the redundant set are powered on without the serial link installed, they both act as independent, non-redundant Primary devices. If they previously operated as a redundant set, their configuration is identical and they use the same H1 node addresses. This will cause problems on the H1 links. To correct this issue, turn off the power to both linking devices, install the serial link, and turn the power on to both devices.

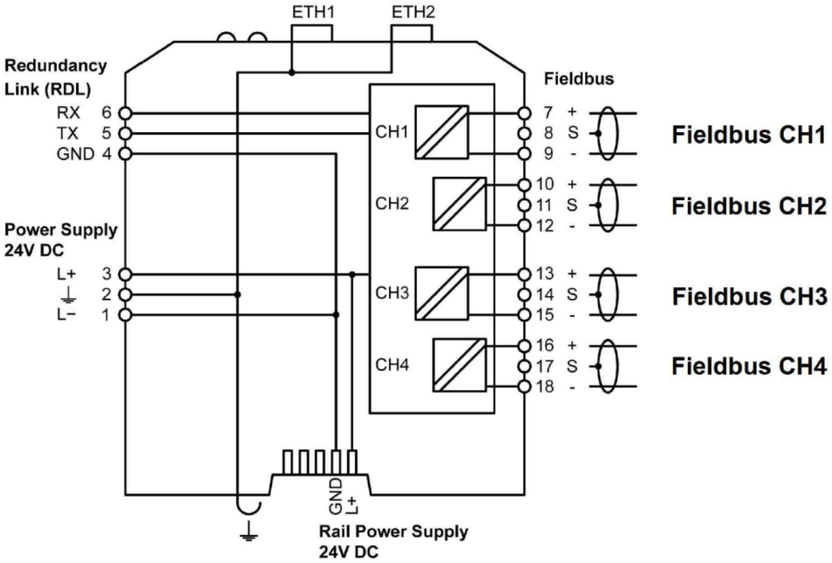
The Primary Linking Device follows the designated controller, regardless of order of startup. This means that if the R controller is the designated controller, the Linking Device on the R IONet will attempt to be the Primary device. If for some reason it cannot be the Primary, then the other linking device on the S IONet becomes the Primary and a diagnostic is generated. A diagnostic is generated in this case because there is an issue with the linking device under the dual controller that does not allow it to switch, which means there is no redundancy.

For a redundant set, wait at least one minute between checks of redundant operations such as removing the power supply, the Ethernet cable, or the serial connector cable from the Primary device. These operations cause a redundancy change-over and the Secondary device must be operational before the next check is done. If the Secondary device is still starting up from the prior change-over, the system breaks down or the configuration information can be lost.

9.1.5 PFFAH1B Operation

9.1.5.1 Connection Overview

The following diagram provides an overview of the PFFAH1B plugs and interfaces.

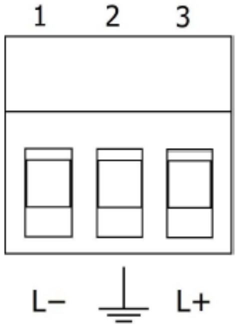


PFFAH1B Connection Diagram

9.1.5.2 Power Supply

The power supply voltage (18 — 32 V dc) is supplied by a 3-pole terminal block with a cross section of 0.75 – 1.5 mm^2 (0.03 – 0.06 in^2), AWG 18 – 16 wire. The L-connection wire must have a cross section of 1.5 mm^2 (0.06 in^2).

Note The physical device may be labeled with pin 1 as Ground and pin 2 as Functional Earth. However, pin 1 is the negative voltage rail.



PFFAH1B Power Supply Terminal Block

9.1.5.3 Ethernet Port

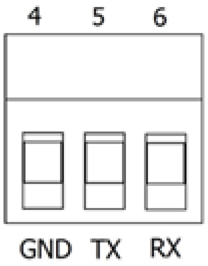
The Ethernet port supports auto negotiation and corresponds to IEEE® 802.3 10Base-T/100Base-TX standards. There are two Ethernet ports on the PFFAH1B, however, the second port is not currently supported.

PFFAH1B HSE Ethernet Port Pin Assignment

Pin	Signal	Description
1	TX+	Transmit signal positive
2	TX-	Transmit signal negative
3	RX+	Receive signal positive
4	Not used	Drain wire
5	Not used	Drain wire
6	RX-	Receive signal negative
7	Not used	Drain wire
8	Not used	Drain wire

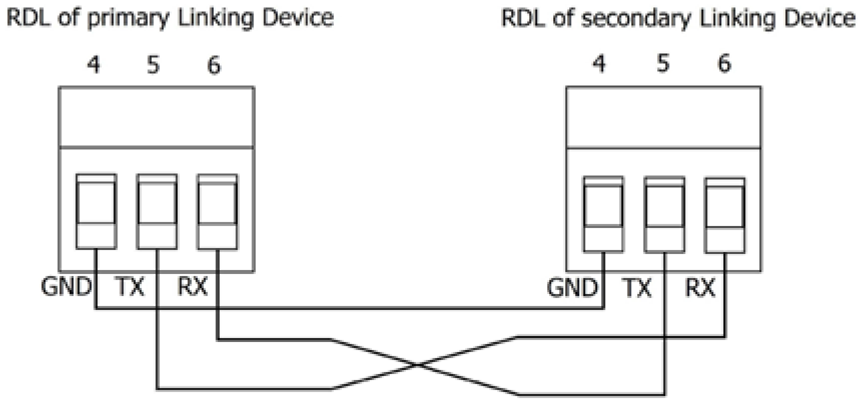
9.1.5.4 Serial Port (Redundancy Link Interface)

When using two PFFAH1B modules as a redundant, Hot Backup set, the redundancy link must be connected by the cable. The link must be installed before power up to operate in redundant mode. The maximum cable length is 0.5 m (3.3 ft).



Redundancy Link Terminal Block

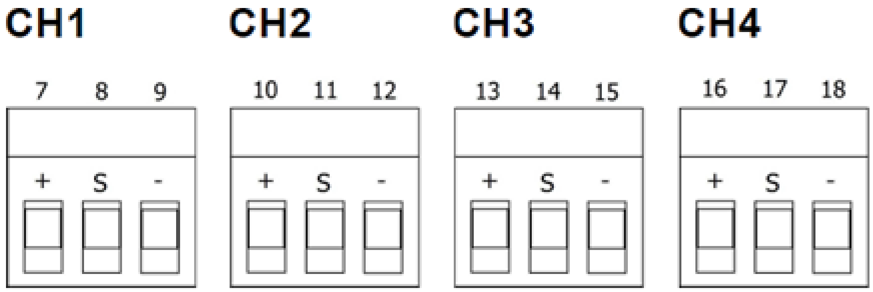
Note The receive (RX) and transmit (TX) signals must be cross-linked to function in redundant mode (TX to RX and RX to TX as illustrated in the following figure).


RDL of primary Linking Device
4
5
6
GND
TX
RX
RDL of secondary Linking Device
4
5
6
GND
TX
RX

9.1.5.5 H1 Connections

The four H1 connections are 3-pole terminal blocks that function as FOUNDATION fieldbus interfaces to the H1 network and comply with type 114 of the FOUNDATION fieldbus physical layer profile. The H1 connections have no intrinsic safety; they operate in standard power signaling and voltage mode, and are separately powered (galvanically isolated). FOUNDATION fieldbus cables can be interchanged and use wires with a cross section of 0.75 – 1.5 mm^2 (0.03 – 0.06 in^2), AWG 18 – 16 wire.

Note PFFA is not rated for Intrinsic Safety (IS) but IS is part of the H1 standard. Refer to drawing 238A7779 for guidelines, rules, and technology for using IS with H1.



PFFAH1B H1 3-pole Terminal Block

PFFAH1A H1 Pin Connections

Channel	Pin	Signal	Description
1	7	+	Fieldbus +
1	8	S	Fieldbus shield
1	9	-	Fieldbus -
2	10	+	Fieldbus +
2	11	S	Fieldbus shield
2	12	-	Fieldbus -
3	13	+	Fieldbus +
3	14	S	Fieldbus shield
3	15	-	Fieldbus -
4	16	+	Fieldbus +
4	17	S	Fieldbus shield
4	18	-	Fieldbus -

9.1.6 Startup Self-tests

Several hardware components are tested during startup. The test is divided into several sections for runtime reasons. The first part of the test is performed with every start of the PFFAH1B linking device and following items are checked:

- Access to Random Access Memory (RAM)
- Checksum test flash content (firmware)
- H1 channel (transmission and reception using an internal loopback)
- Interrupt triggering of the H1 controllers

Note System and H1 device diagnostics can be viewed from the ToolboxST application Hardware tab for the linking device.

The RAM test checks whether the entire RAM memory space can be accessed and of the data is consistent. The checksum test checks the consistency of the flash memory content. If an error is found during this process, startup is stopped. This may require replacing the linking device.

9.1.7 PFFAH1B LEDs

The LED block contains the LEDs listed in the following table.

LEDs

LED	Color	Indication
PWR	Red / Green	Power supply
LAN	Red / Green	Running
ERR	Red / Green	Error status
RDL	Red / Green	Redundancy Link
CH1	Green	Link Status Channel 1
CH2	Green	Link Status Channel 2
CH3	Green	Link Status Channel 3
CH4	Green	Link Status Channel 4

During startup, all LEDs are switched on briefly for an optical performance test.

The following tables provide diagnostic information indicated by the LED indications.

Device Status Indications

LED	Display	Description
PWR Power Supply	Off	No supply voltage
	Permanent Green	24 V supply voltage present and ok

Device Status Indications – Simplex Mode

LED	Display	Description
ERR/RUN Error/Ready Combination	PWR = Green ERR = Off RUN = Off RDL = Off	Startup phase (~7 seconds) During this phase the redundancy role is determined.
	PWR = Green ERR = Off RUN = Green RDL = Off	Non-redundant device, ready The device is operational; it is not part of a redundant set.
	PWR = Green ERR = Red RUN = Green RDL = Off	Permanent hardware fault detected during startup A fatal error has been detected during startup self-tests.

Device Status Indications – Hot Backup Mode

LED	Display	Description
ERR/RUN Error/Ready Combination	PWR = Green ERR = Off RUN = Off RDL = Off	Startup phase (~7 seconds) During this phase the redundancy role is determined.
	PWR = Green ERR = Off RUN = Green RDL = Off	Non-redundant device, ready The device is operational and acting as Primary device in a redundant set. The Secondary device is ready.
	PWR = Green ERR = Red RUN = Green RDL = Off	Permanent hardware fault detected during startup A fatal error has been detected during startup self-tests. Possible failure could be missing Ethernet connection.
	PWR = Green ERR = Flashing Red RUN = Green RDL = Off	Primary device or non-redundant device, hardware failure The device is acting as non-redundant device, but a minor hardware failure has been detected during startup. In the case of a Primary device on a redundant set, the Secondary device is not ready.
	PWR = Green ERR = Red RUN = Flashing Green RDL = Off	Primary device or non-redundant device, failure The device is acting as non-redundant device, but a failure has been detected. OR Secondary device, not ready The device is acting as Secondary device in a redundant set, but it is not ready to take over the Primary role due to reasons such as un-synchronized configuration information or a non-operational redundancy link. OR Primary device or non-redundant device, failure The device is acting as Primary device in a redundant set or as non-redundant device, but a failure has been detected. In the case of a Primary device in a redundant set or as non-redundant set, the Secondary Device is not ready.

Device Status Indications – Hot Backup Mode — Continued

LED	Display	Description
ERR/RUN Error/Ready combination	PWR = Green ERR = Off RUN = Flashing Green, slowly (0.5 Hz) RDL = Flashing Green, slowly (0.5 Hz)	Secondary device, operational The device is operational as Secondary device in a redundant set. The configuration information has been successfully transferred from the Primary device and the redundancy link is operational.
	PWR = Green ERR = Flashing Red RUN = Off RDL = Off	Secondary device, hardware failure The device is acting as Secondary device in a redundant set, but a hardware failure has been detected. Details are available on the web page Diagnostics of the linking device.
	PWR = Green ERR = Flashing Red RUN = Green RDL = Off	Primary with H1 error state
	PWR = Green ERR = Red RUN = Green RDL = Off	Primary not ready
	PWR = Green ERR = Flashing Red RUN = Flashing Green RDL = Off	Secondary with H1 error
	PWR = Green ERR = Flashing Red RUN = Off RDL = Off	Primary, configuration error

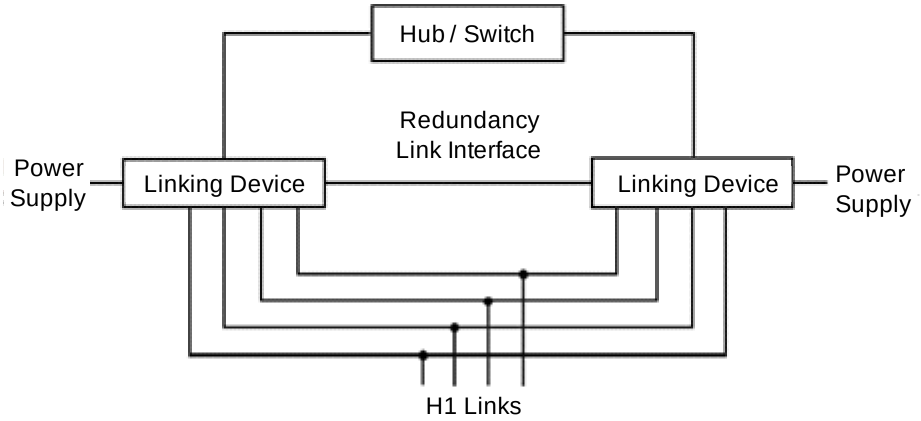
H1 Channel Status Indications

LED	Display	Description
Channel 1–4 Status of H1 Channel	Permanent Green	Visitor mode
	Fast Flashing Green (5 Hz)	Device acts as the Link Active Scheduler (LAS) on H1 channel
	Slow Flashing Green (0.5 Hz)	Device is in logical token ring but does not act as the LAS on H1 channel
	Permanent Red	No Carrier or H1 link is disconnected
	Flashing Red	No token received
	Off	H1 Channel link is not configured or not in the token ring

9.1.8 Configuration

Configuration of PFFAH1B linking devices and attached segments, fieldbus devices, fieldbus blocks, and related parameters and properties is performed in the ToolboxST application. For further information, refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703), the chapter *Mark VIe FOUNDATION Fieldbus Interface*, the section *Configuration*.

9.1.9 Redundancy Mode



PFFAH1B System Topology

A redundant Linking Device consists of two physical Linking Devices that are connected to the same HSE subnet and to the same H1 links. The redundant set of devices behaves like one logical Linking Device. By duplicating the physical Linking Device, it is possible to tolerate one fault in one of the two devices.

In a redundant set of devices, one Linking Device acts as a Primary device and actively performs all communication functions, including the Link Active Scheduler (LAS) function on the H1 links. The Primary device has to be addressed by the Mark VIe control and the configuration tools, similar to the Designated Controller concept except that ControlST does communicate to both devices through the IONet.

The Secondary Linking Device acts as a backup device. It automatically receives the same configuration as the Primary device, but uses different node addresses on the H1 links and a different IP address on the HSE. If the Primary device fails, the Secondary device is able to take over the functionality of the Primary device. In which case, the Linking Device is reduced to a non-redundant system that is not able to tolerate any further failure. Therefore, it is necessary to replace the defective device as soon as possible to recover redundancy. The Secondary device acts as Backup Link Master on each H1 link and attempts to take over the LAS role if required.

The two devices forming a redundant set communicate through a redundancy link interface and over Ethernet. The serial line is used to establish a redundant set of devices, to exchange signs of life, and to control redundancy switch-over. Ethernet is used to transfer configuration information from the Primary device to the Secondary device. An operational serial communication path and an operational Ethernet path between both devices are required for proper operation.

A Heartbeat message is used to control switch-over in the Mark VIe control system. This message is sent from the Primary device to the Secondary device through the Mark VIe controller. If the Secondary device does not receive this message for a certain length of time, it informs the Primary device through the redundancy serial connector that it is taking over the role of Primary device in the system.

9.1.9.1 Redundancy Troubleshooting

Fault Description	**Primary device fails due to permanent or transient hardware or software fault**
Fault Detection	Device fails completely or software watchdog expires or hardware watchdog expires or exception occurs or failure in H1 interface detected.
Fault Treatment	Primary role actively transferred to or taken by Secondary device
Effect	Redundancy switch-over. System degrades to non-redundant system.
Resolution	Transient fault: automatic reboot. Permanent fault: replace device. Secondary device will reboot and receive configuration data from Primary device.

Fault Description	**Ethernet connection lost between Primary device and Ethernet switch**
Fault Detection	Bad link status of Ethernet port detected. Detection time less than 500 ms.
Fault Treatment	Primary role actively transferred to redundant device
Effect	Redundancy switch-over. System degrades to non-redundant system.
Resolution	Repair or reconnect Ethernet cable. Secondary device will reboot and receive configuration data from Primary device.

Fault Description	**H1 cable broken between Primary device and H1 network**
Fault Detection	Empty live list detected on one H1 port or Primary device while Secondary device still has non-empty live list. Due to the H1 protocol it may take some seconds. Until the live list becomes empty. Detection occurs only if in Primary device and Secondary device the number of active H1 devices in the live list has exceeded the threshold of one.
Fault Treatment	Primary role actively transferred to redundant device, so that access to H1 is possible again.
Effect	Redundancy switch-over. No redundancy concerning the affected H1 link.
Resolution	Repair or reconnect H1 cable.

Fault Description	**Secondary device fails due to permanent or transient hardware or software fault**
Fault Detection	Device fails completely or software watchdog expires or hardware watchdog expires or exception occurs or failure in H1 interface detected.
Fault Treatment	Secondary device assumes and indicates non-operational state.
Effect	System degrades to non-redundant system.
Resolution	Transient fault: automatic reboot. Permanent fault: replace device. Secondary device will reboot and receive configuration data from Primary device.

Fault Description	**Ethernet cable broken between Secondary device and Ethernet switch**
Fault Detection	Bad link status of Ethernet port detected. Detection time less than 500 ms.
Fault Treatment	Secondary device assumes and indicates non-operational state.
Effect	System degrades to non-redundant system.
Resolution	Repair or reconnect H1 cable. Secondary device will reboot and receive configuration data from Primary device.

Fault Description	**H1 cable broken between Secondary device and H1 network**
Fault Detection	No fault detection in Secondary device. Empty live list has to be detected by any HSE client (such as asset monitor).
Fault Treatment	None
Effect	No redundancy concerning the affected H1 link.
Resolution	Repair or reconnect H1 cable.

Fault Description:	**TCP connection lost between Primary device and Secondary device**
Fault Detection	Time-out on TCP connection. Detection time less than 2 sec during activity and less than 7 sec during idle times.
Fault Treatment	Secondary device assumes and indicates non-operational state.
Effect	System degrades to non-redundant system. Secondary device clears configuration.
Resolution	Repair Ethernet connection. Secondary device may reboot in some cases depending on prior state and will receive configuration data from Primary device.

Fault Description	**Redundancy link broken or removed between Primary device and Secondary device**
Fault Detection	Loss of serial communication. Detection time less than 800 ms.
Fault Treatment	Secondary device assumes and indicates non-operational state.
Effect	System degrades to non-redundant system.
Resolution	Repair or reconnect redundancy link. Secondary device will reboot and receive configuration data from Primary device.

9.1.9.2 Duration of Redundancy Switch-over

During redundancy switch-over, the activity on H1 links is interrupted. From the perspective of a single H1 device, PUB/SUB links are interrupted for a period of time, as follows:

Fault detection time:

- 800 ms if Primary device fails
- 1500 ms if Ethernet connection on the Primary device is removed

Redundancy switching time: 500 ms

9.1.10 Fault Domain

9.1.10.1 Transfer from Primary Device to Secondary Device

The Primary device transfers its role to the Secondary device in the following scenarios:

- **If** the Designated Controller in the Mark VIe control system changes, the Primary will change to match it
- **Or** the Primary device detects a failure of its own Ethernet port
- **Or** the Primary device detects a failure on at least one H1 interface
- **Or** the Primary device detects a loss of the connection to all device on an H1 link

The Secondary device accepts the transfer in the following scenarios:

- **If** its H1 interfaces are operation and faultless
- **And** its Ethernet port is operational
- **And** it has a valid configuration

9.1.10.2 Secondary Device Takes Over Primary Role

The Secondary device takes over the Primary role in the following scenarios:

- **If** it doesn’t detect the heartbeat signal through HSE
- **Or** the serial connection to the Primary device is lost
- **And** it acts as a Link Active Scheduler on all configured H1 links
- **And** its Ethernet port is operational

9.1.10.3 Restoring Redundancy

Only one of the faults listed in the following table may be present at one time. Another fault cannot be tolerated until the redundant set has been repaired and a fully operational Secondary device is available.

The required measures for repairing the redundant set of devices depend on the present Fault.

PFFAH1B Redundancy Faults

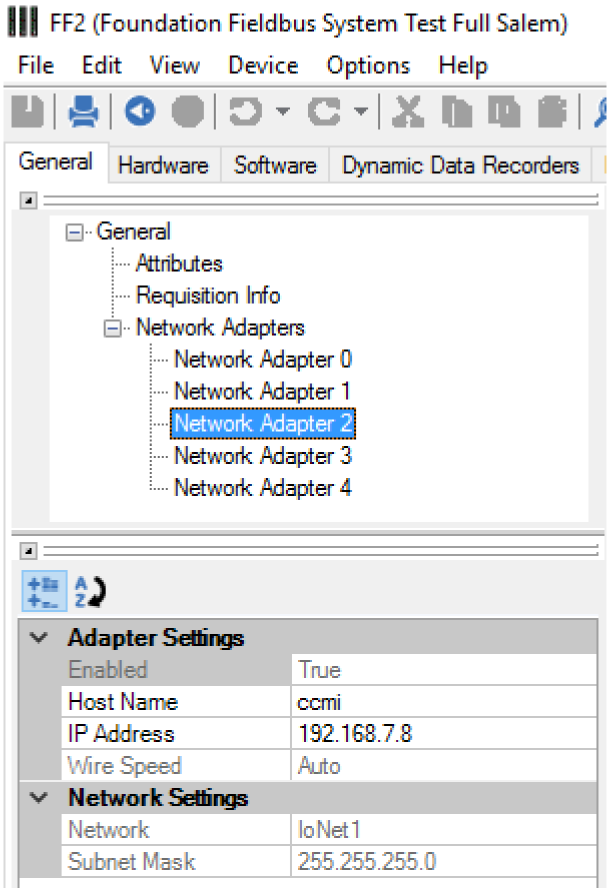
Fault	Solution
Permanent fault within the PFFAH1B	Replacement of the defective PFFAH1B
Transient fault within the PFFAH1B	Restart of the PFFAH1B (performed automatically)
Loss of serial connection between the two PFFAH1Bs	Re-establishment of the serial connection
Loss of the Ethernet connection between the two PFFAH1Bs	Re-establishment of the Ethernet connection
Loss of an H1 connection between the Primary devices and the entire H1 link	Re-establishment of the H1 connection

9.1.11 Web Server

A web server is available on the PFFAH1B to be used for advanced debugging and for firmware upgrades. The web server should only be accessed for these purposes.

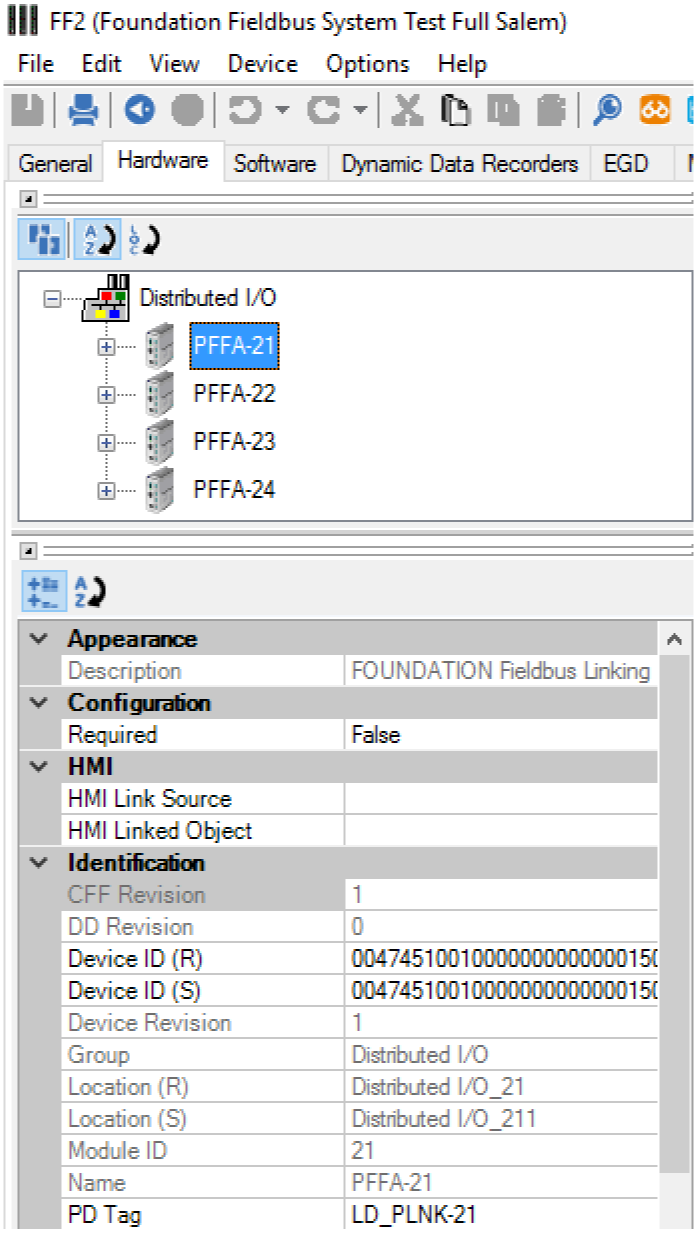
9.1.11.1 Locate IP Address of Linking Device and Web Server

Locate the IONet IP address for your controller using ToolboxST. The following example uses the IP address 192.168.7.8 for the R IONet.



Adapter Settings	
Enabled	True
Host Name	ccmi
IP Address	192.168.7.8
Wire Speed	Auto
Network Settings	
Network	IoNet1
Subnet Mask	255.255.255.0

This means that the IP address of the Linking Device placed on this R IONet will be in this subnet and will end with its Module ID. The Module ID in this example is 21, which means the IP Address of my Linking Device on my R IONet is 192.168.7.21.



Appearance	
Description	FOUNDATION Fieldbus Linking
Configuration	
Required	False
HMI	
HMI Link Source	
HMI Linked Object	
Identification	
CFF Revision	1
DD Revision	0
Device ID (R)	00474510010000000000000015
Device ID (S)	00474510010000000000000015
Device Revision	1
Group	Distributed I/O
Location (R)	Distributed I/O_21
Location (S)	Distributed I/O_211
Module ID	21
Name	PFFA-21
PD Tag	LD_PLNK-21

Therefore, a user can plug their computer into the R IONet switch and access the web server on this Linking Device. The web server address used in this example is http://192.168.7.21/.

9.1.11.2 Assign Second (Local) IP Address for Windows 10

➢ **To assign a second (local) IP address under Windows 10**

1. Open the **Desktop**.
2. Press the **Windows Start key** and select **Control Panel**.
3. Select **Network** and **Internet**.
4. Open **Network and Sharing Center**.
5. Click **Connections** for the network adapter you want to configure.
6. In the Connection Status window click **Properties**.
7. In the item connection list, select **Internet Protocol Version 4 (TCP/IPv4)**.
8. Click **Properties**.
   In the *General* dialog box, the regular (first) IP address, the subnet mask and the standard gateway are displayed.
9. Click **Advanced** to add a second IP address. Then click **[Add]** in the *IP Addresses* dialog box.
10. Enter the IP address and the subnet mask.
    - Make sure the IP address you choose is within the same subnet as the Linking Device to which you are trying to connect.
    - It is recommended to choose a subnet of 255.255.255.0, which means you will have to add two IP addresses: one for the Primary Linking Device and another for the Secondary Linking Device.
11. Click **[Add]**.
12. Confirm all open dialog boxes by clicking **[OK]**.

9.1.11.3 Open the Web Server

To connect directly from a computer to the Linking Device, a cross-linking cable must be used. If a switch or hub is connected between the two, a normal Ethernet cable will work.

Perform a ping test can be used to check for connection to the Linking Device.

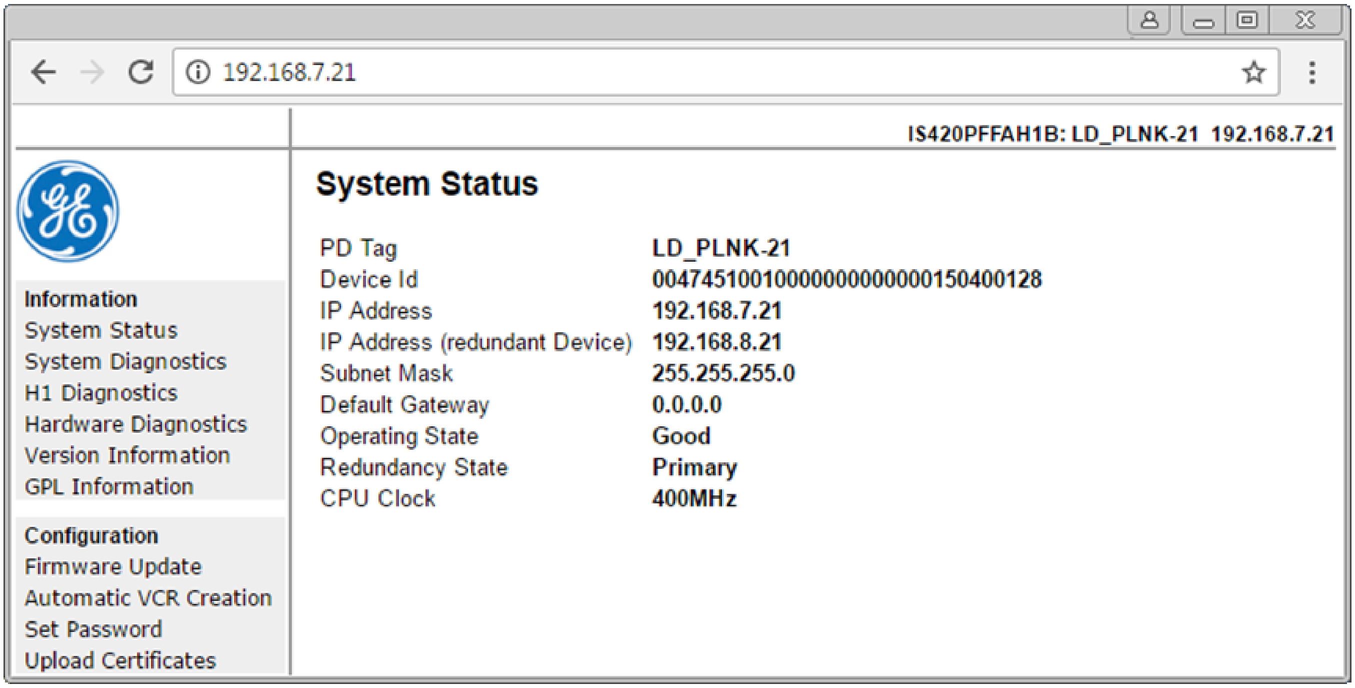
➢ **To ping the connection to the PFFAH1B Linking Device:** where the IP address is the IP address of the Linking Device, ping 192.168.x.x.

After the ping test confirms the connection, open the web server.

➢ **To open the web server:** open a web browser (such as Internet Explorer, Firefox, or Chrome) and enter the IP Address of the Linking Device as http://192.168.x.x.

9.1.11.4 Information Web Page

The System Status page can be used to check the PD Tag, Device ID, IP Address of the Primary and its Hot Backup device, along with its operating state and redundancy state.

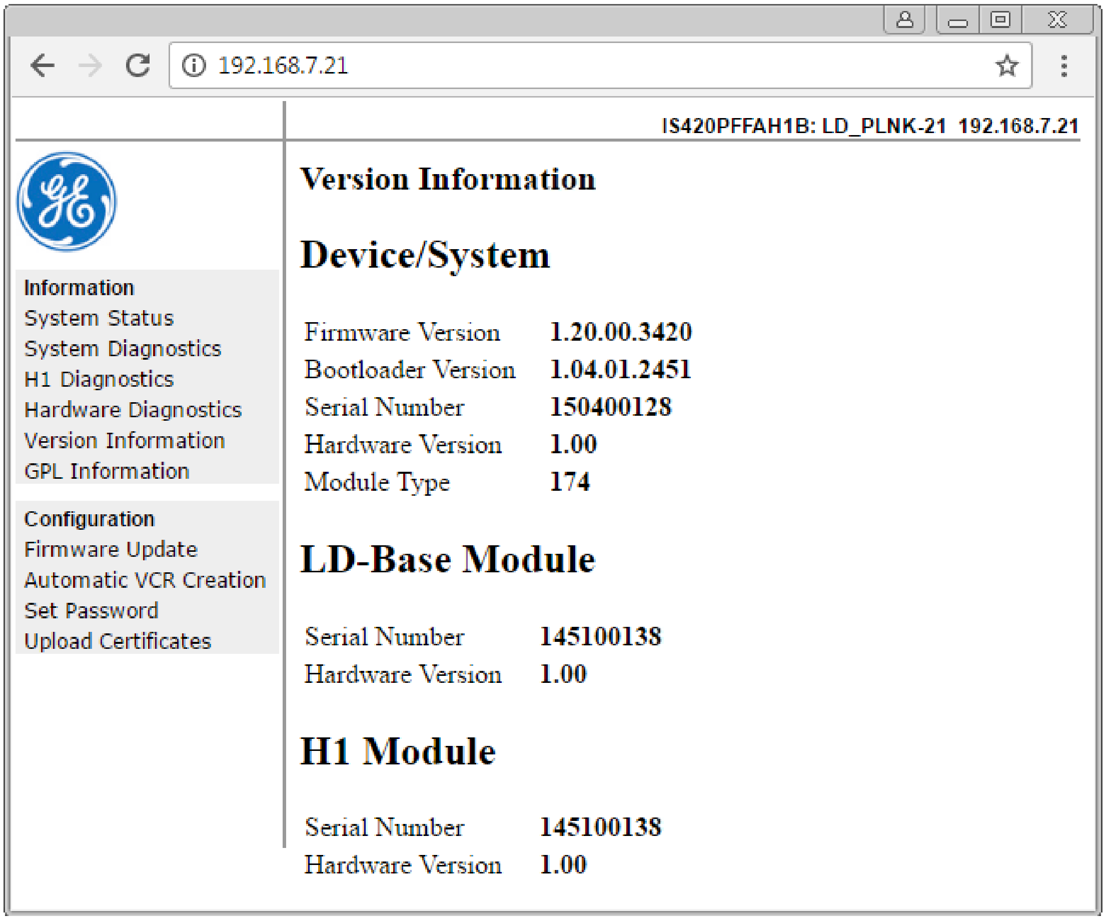


System Status

PD Tag	LD_PLNK-21
Device Id	00474510010000000000000150400128
IP Address	192.168.7.21
IP Address (redundant Device)	192.168.8.21
Subnet Mask	255.255.255.0
Default Gateway	0.0.0.0
Operating State	Good
Redundancy State	Primary
CPU Clock	400MHz

Web Server System Status Page

The *Version Information* page contains information such as Firmware and Bootloader versions, as well as serial numbers.



IS420PFFAH1B: LD_PLNK-21 192.168.7.21

Version Information

Device/System

Firmware Version	1.20.00.3420
Bootloader Version	1.04.01.2451
Serial Number	150400128
Hardware Version	1.00
Module Type	174

LD-Base Module

Serial Number	145100138
Hardware Version	1.00

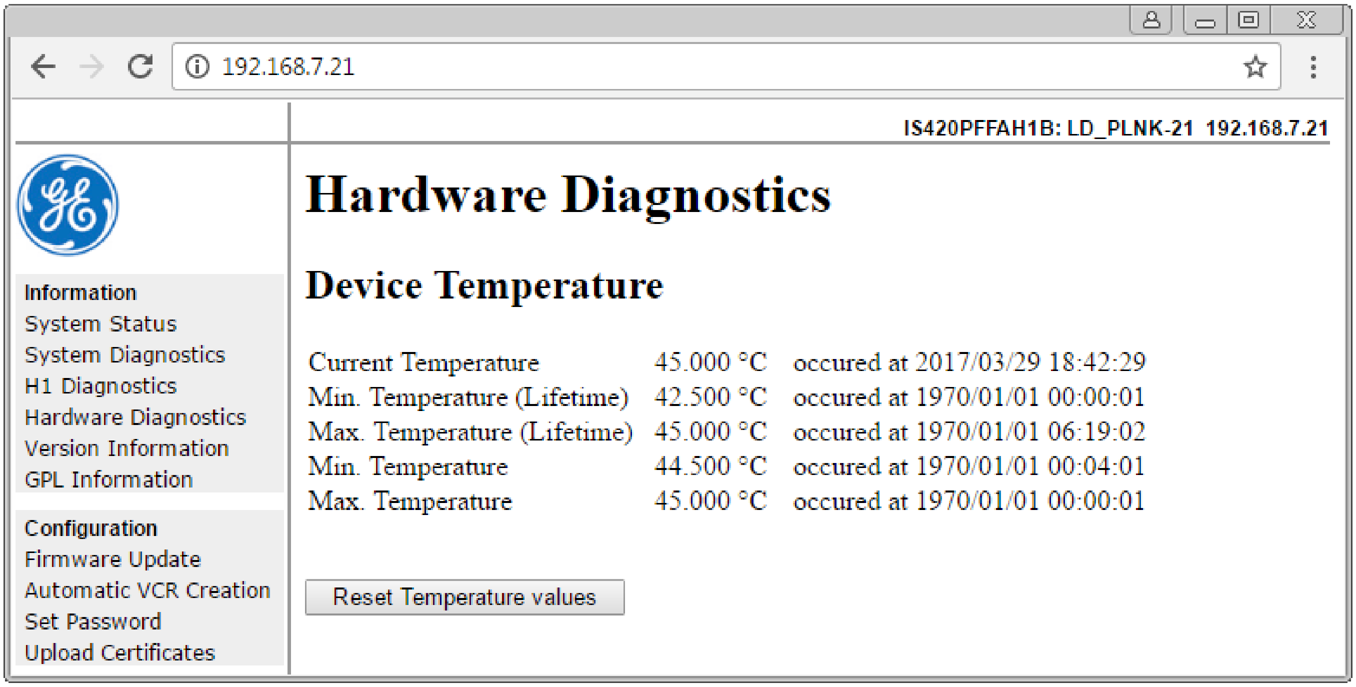
H1 Module

Serial Number	145100138
Hardware Version	1.00

Web Server Version Information Page

9.1.11.5 Diagnostics Web Pages

The *Hardware Diagnostics* page contains information such as device temperature and temperature history.



Hardware Diagnostics

Device Temperature

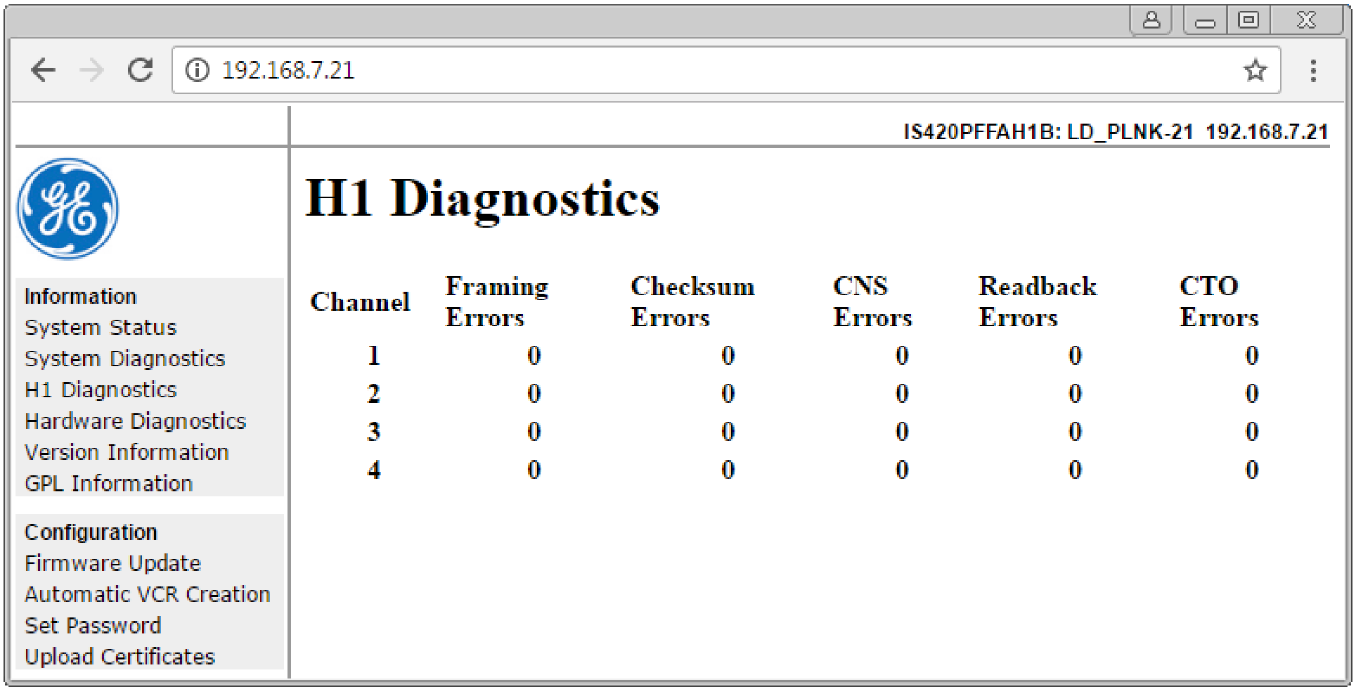
Current Temperature	45.000 °C	occured at 2017/03/29 18:42:29
Min. Temperature (Lifetime)	42.500 °C	occured at 1970/01/01 00:00:01
Max. Temperature (Lifetime)	45.000 °C	occured at 1970/01/01 06:19:02
Min. Temperature	44.500 °C	occured at 1970/01/01 00:04:01
Max. Temperature	45.000 °C	occured at 1970/01/01 00:00:01

Web Server Hardware Diagnostics Page

The *H1 Diagnostics* page provides a table that displays FPGA error statistics in the PFFAH1B. The values of the framing error counters per channel and checksum errors in received packets are available for advanced debugging. High counter values may indicate a bad signal quality in the H1 channel and/or a device that is not operating properly. These values are reset on power up.

The values shown on the following example H1 Diagnostics page are as follows:

- Carrier Not Seen Errors indicates no communication on the fieldbus. This is normal for example if no H1 segments are connected, or during startup when no other devices are communicating on the network. This should not occur during normal operation with active communication.
- Buffer Not Empty might indicate that the H1 network is not connected or not powered.
- Receive Overrun
- Transmit Overrun
- Transmit Readback Error
- Collision Timeout Errors might indicate that the H1 network is not connected or not powered.



H1 Diagnostics

Channel	Framing Errors	Checksum Errors	CNS Errors	Readback Errors	CTO Errors
1	0	0	0	0	0
2	0	0	0	0	0
3	0	0	0	0	0
4	0	0	0	0	0

Example H1 Diagnostic Page

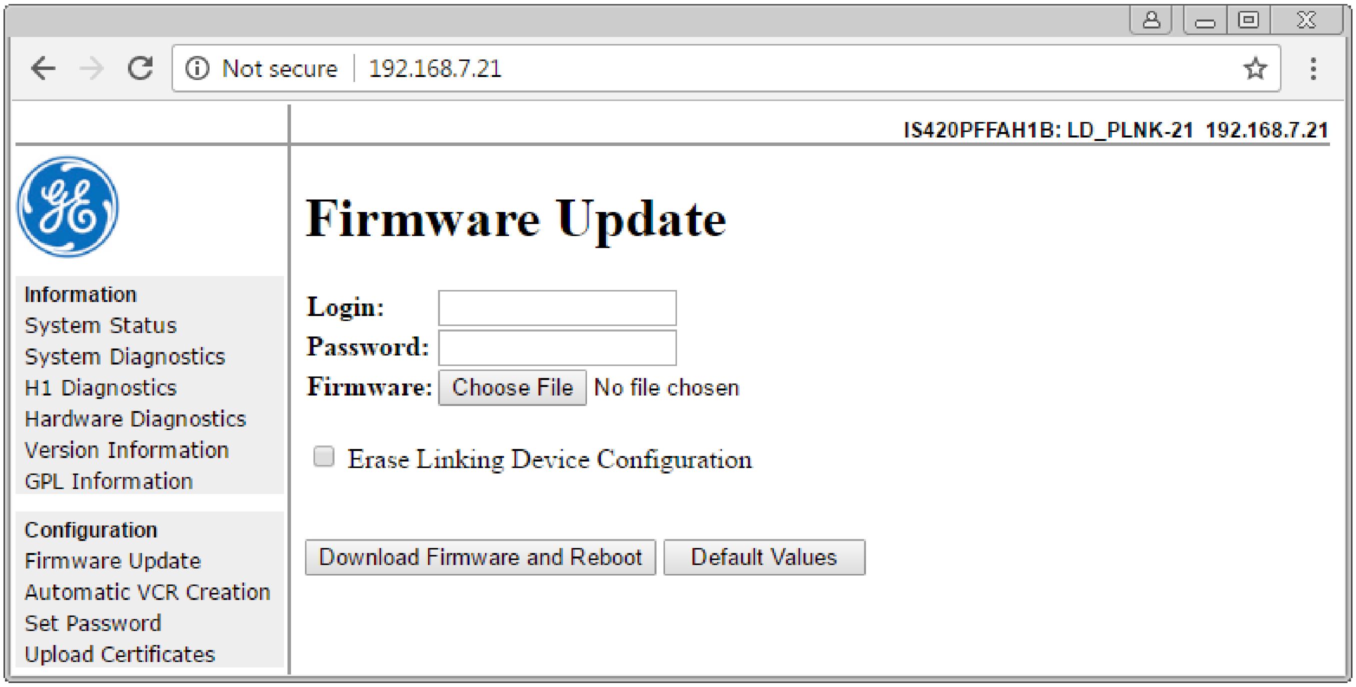
Note The contents of these FPGA registers contains data that is only relevant to GE's customer support for error analysis and troubleshooting.

9.1.11.6 Firmware Update

The *Firmware Update* page can be used to upgrade the firmware version of the Linking Device. For the default login and password credentials, refer to the section *Set Password*.

The firmware file will be a binary (.bin) file (provided by GE). This firmware upgrade is not done through ControlST or ToolboxST and is a file that will be uploaded manually to the web server.

Note If the **Erase Linking Device Configuration** button is checked, all H1 device configurations will be cleared and the PD Tag will be reset to an empty string, but the web page password will not be reset to default.

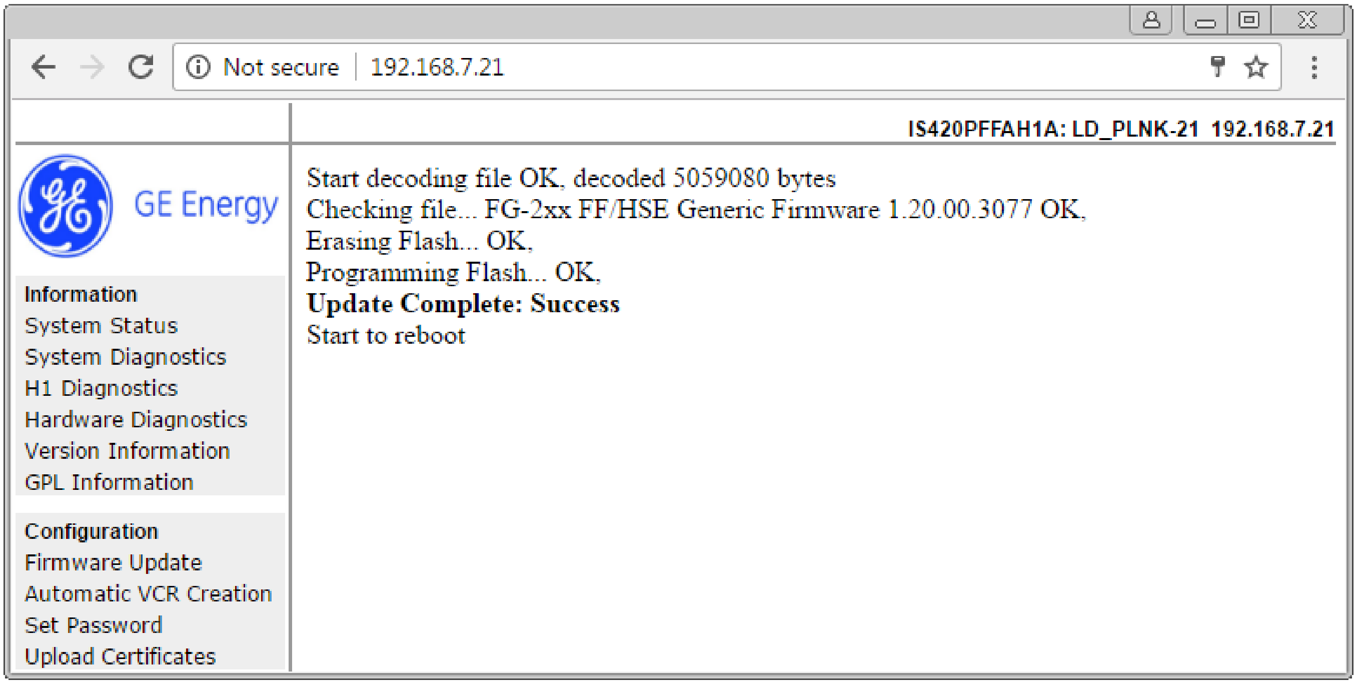


Firmware Update Web Page

Note Do not access or reload the web server of the Linking Device before the *Success* message is displayed in the browser window. If you do so, you will have to clear the cache of your web browser after the boot process has finished, and then re-establish a connection to the web server of the Linking Device.

The end of the boot process is indicated by a continuously lit RUN LED for a Linking Device acting in non-redundant mode or for a Primary device in redundant mode. For a Secondary device it is indicated by a flashing (1 Hz) RUN LED.

The following figure displays a successful firmware update. Once the *Start to reboot* line displays, wait ~10 sec (for the device to successfully complete its reboot) and refresh the web page.

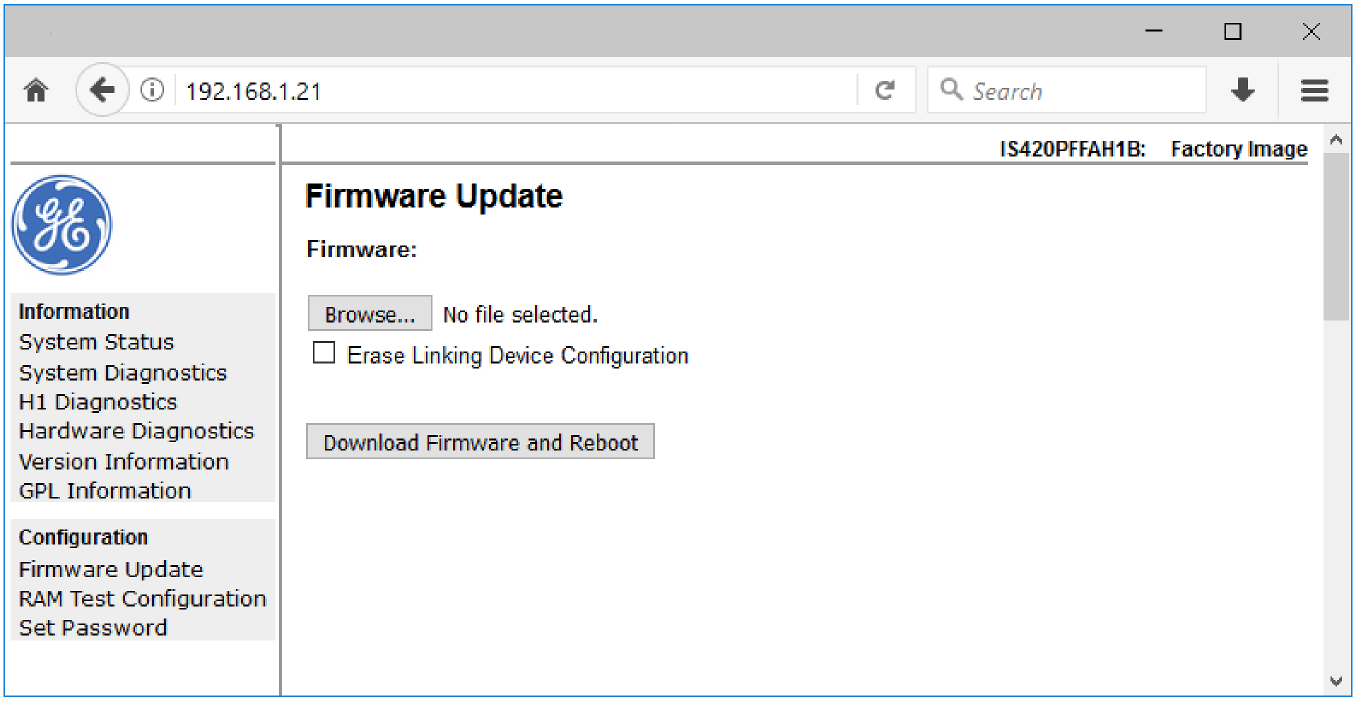


Start decoding file OK, decoded 5059080 bytes
Checking file... FG-2xx FF/HSE Generic Firmware 1.20.00.3077 OK,
Erasing Flash... OK,
Programming Flash... OK,
Update Complete: Success
Start to reboot

Firmware Upgrade Complete

In the event of power loss during firmware update, the PFFAH1B will reboot to its default factory image (the custom image may be corrupted). The PFFAH1B will still request an address from the Mark VIe control and users should upgrade the firmware using the web page.

Note The PFFAH1B will not be shown as connected in ToolboxST because there is no configuration or firmware loaded.



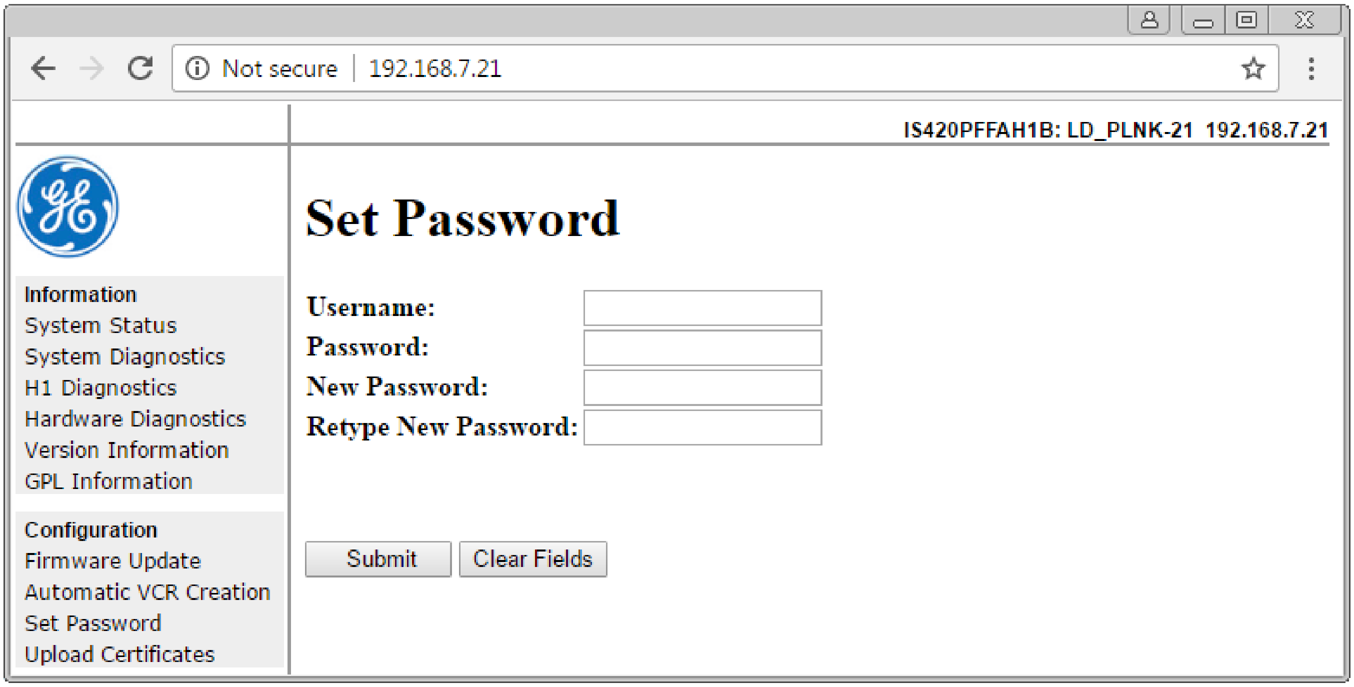
Default Factory Image Web Page

9.1.11.7 Set Password

It is highly recommended to change the default password on the PFFAH1B to help secure your system. The password can be changed from the *Set Password* page. The default login credentials are as follows:

- Username: **administrator**
- Password: **fgadmin**

Note There is no method to reset the password to the factory default. The password can only be changed by entering the current password and then entering a new password.



IS420PFFAH1B: LD_PLNK-21 192.168.7.21

Set Password

Username:
Password:
New Password:
Retype New Password:

Set Password Page

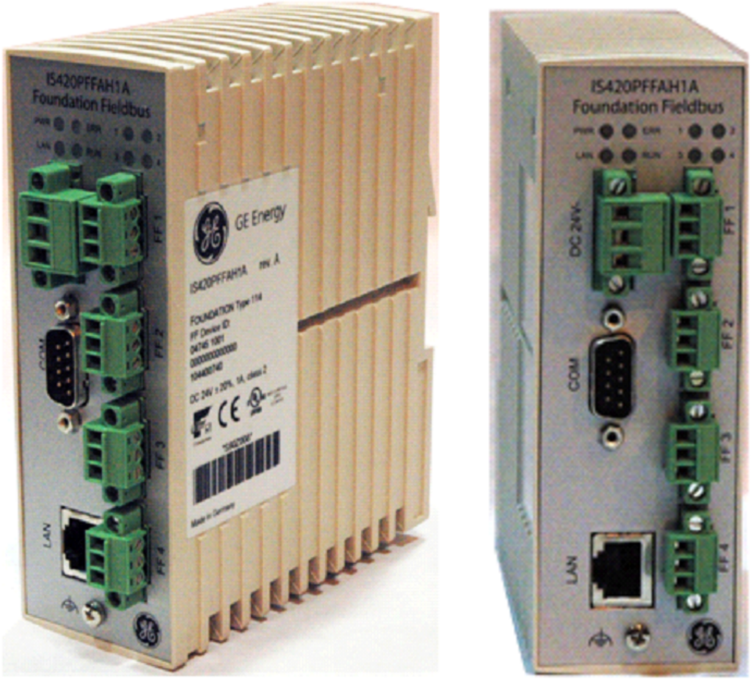
9.2 PFFAH1A Linking Device

The PFFAH1A linking device operates on 24 V dc and provides the following:

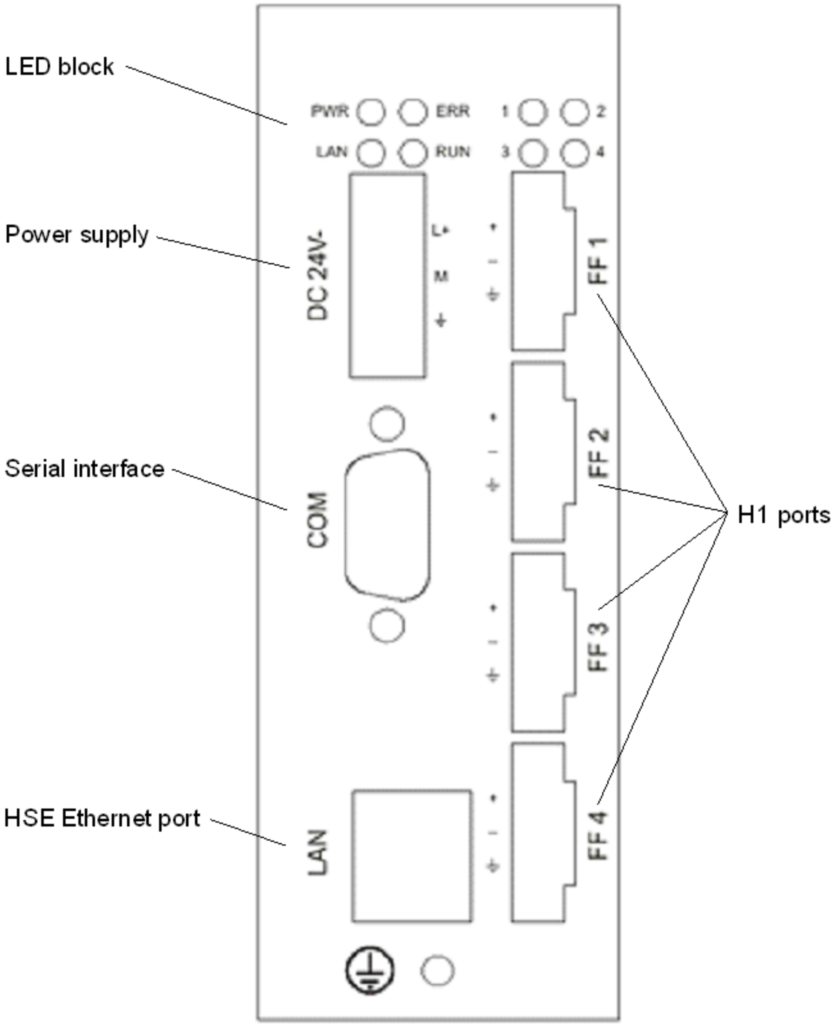
- One serial COM port for redundant operation
- One LAN port for HSE subnet connection
- Four fieldbus H1 ports

A separate screw connection is provided for grounding in addition to the ground wire that is required as part of the power supply connection. The linking device serves as a gateway between the HSE and four onboard ports. For each of the ports, the linking device operates as the Link Master (LM) and as the system management (SM) time publisher. The linking device supports dual redundant operation, it is fanless, and its compact size allows it to be used in a DIN-rail assembly.

The linking device sends processed data from one H1 link to another H1 link, and sends and receives data from the H1 link to the HSE. It also provides access to the components attached to the H1 links for configuration and identification, including access to the component function blocks.



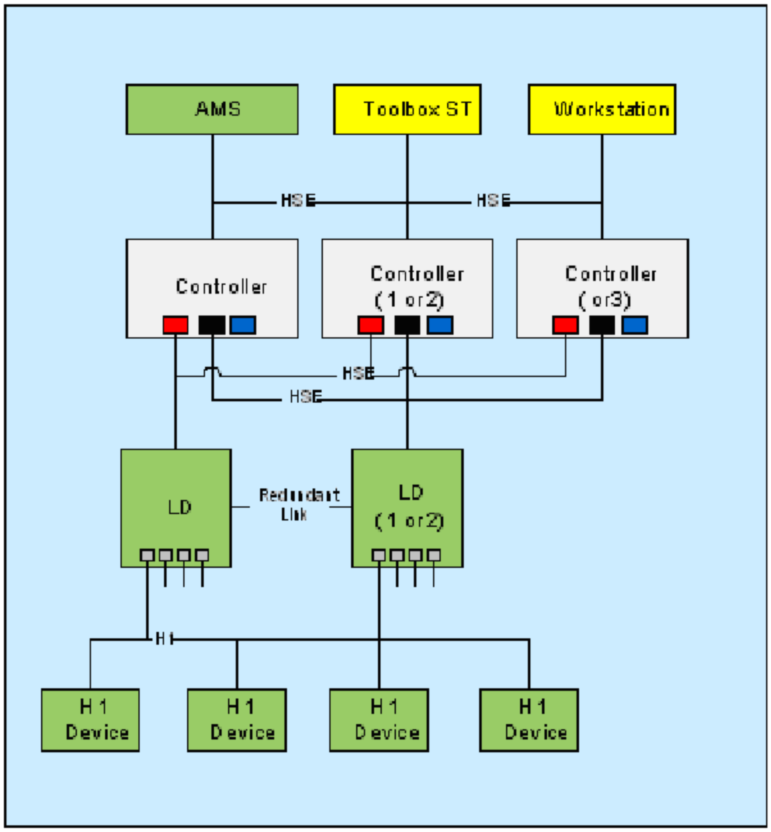
PFFAH1A Linking Device



PFFAH1A Linking Device Faceplate

9.2.1 PFFAH1A Functionality

A PFFAH1A Linking Device is used to interconnect 31.25 kilobits/sec fieldbuses and make them accessible to an HSE backbone running at 100 megabits/sec or 1 gigabit/sec. It acts as the gateway between FOUNDATION fieldbus HSE subnet and the FOUNDATION fieldbus H1 links. It supports device redundancy.



Basic FOUNDATION Fieldbus Layout

PFFAH1A linking device functionality includes the following:

- Gateway between an Ethernet (HSE) port and 4 fieldbus (H1) ports
- Supports up to 16 field devices per segment
- Supports up to four separate H1 links. In each of these links, the Linking Device operates as the Link Master as well as the System Management (SM) Time Publisher.
- Identification of the devices connected to the H1 links
- Configuration of the connected H1 devices by System Management and Network Management through HSE
- Access to the function blocks of the connected H1 devices through HSE
- Republishing of process data from one H1 link to another
- Republishing of process data from H1 to HSE and vice versa

Note For a detailed description of terms and additional details, refer to the *Mark VIe Control FOUNDATION Fieldbus Interface Application Guide* (GEH-6761) or the Fieldbus FOUNDATION's documentation.

HSE subnet functions:

- System Management Agent
- Network Management Agent
- Server providing object access to H1 devices
- Publishing/subscribing of process data from/to H1 components

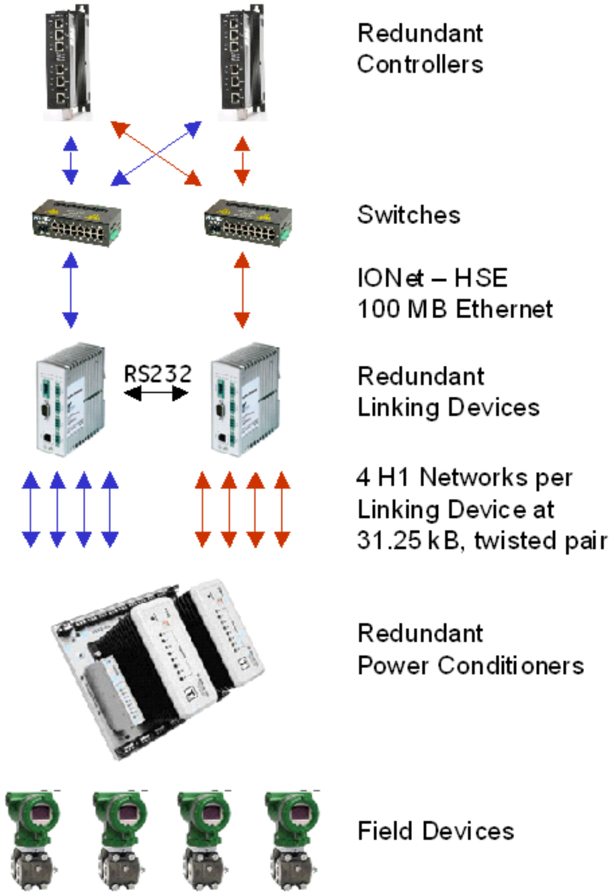
H1 link functions:

- System Management Manager
- Network Management Manager
- Client for object access to H1 components
- Publisher and subscriber of process data
- Link Master, SM Time Publisher

9.2.2 Compatibility

The PFFAH1A linking device supports Simplex and Hot Backup redundant operations. In Hot Backup mode, two physical linking devices are connected by a serial RS-232 null modem cable to form one logical linking device (redundant set). Redundancy control information is shared over the RS-232 cable. One linking device operates as the Primary device while the other operates as the Secondary device. In the redundant set, both linking devices are connected to the same H1 components and HSE subnet. The linking device is compatible with Mark* VIe I/O packs and controllers available in the ToolboxST* application V04.03 or later.

To ensure continuity and continuous operation, the Secondary device automatically takes over if the Primary device fails. When the failed linking device is replaced, it is automatically configured to match the now Primary device and to take over as the Secondary device in the redundant set. If an H1 segment connector gets disconnected from the Primary linking device it switches roles to the Secondary linking device only if there are two or more H1 devices on the segment. If there is not a device, or there is only one, the linking device does not switch roles.



PFFAH1A Redundant Linking Devices and Power Conditioners

9.2.3 PFFAH1A Specifications

Item	PPFAH1A Specification
Power Supply	24 V dc ±20%
Power Consumption	Typical: 200 mA
Dimensions	47 x 131 x 111 mm (1.9 x 5.2 x 4.4 in)
Ambient Rating for Enclosure Design†	0 to 55°C (32 to 131 °F)
Ethernet Interface	1 – Ethernet 10Base-T/100Base-TX, RJ-45 port
Ethernet Transfer Rate	10 mbps or 100 mbps (autosensing)
H1 Fieldbus Interface	4 – FF H1 3-pole screw terminals (pluggable), transformer coupling ports
H1 Fieldbus Transfer Rate	31.25 kbps
Serial Interface	1 – 9-pole SubD RS-232 port
Serial Transfer Rate	115.2 kbps

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

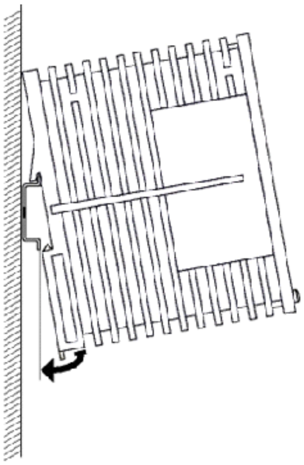
9.2.4 Installation and Troubleshooting

9.2.4.1 PFFAH1A Mounting and Installation

Warning **This equipment contains a potential hazard of electric shock, burn, or death. Ensure that all Lockout/Tag Out (LOTO) procedures are followed prior to replacing terminal boards. Only personnel who are adequately trained and thoroughly familiar with the equipment and the instructions should install, operate, or maintain this equipment.**

➢ **To mount and install the PFFAH1A linking device**

1. Securely mount the linking device. On a DIN-rail, attach the two upper notches to the rail. Press the linking device down towards the rail until it locks into place.



PFFAH1A DIN-rail Mounting

2. Connect the H1 links to the H1 ports.

Note The linking device does not provide power to the H1 links, so a power supply, power conditioner, and a bus termination must be provided for each link.

3. Connect the LAN port to an Ethernet switch or hub.
4. Connect a 24 V dc power supply to the linking device.
5. Turn on the power supply. The startup process takes ~50 seconds. Refer to the section *PFFAH1A LEDs* for an indication of proper operation.
6. Configure the PFFAH1A using the ToolboxST application. Refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703), the chapter *Mark VIe FOUNDATION Fieldbus Interface*, the section *Configuration*.

9.2.4.2 Adding a Second Linking Device for Hot Backup

One linking device operates as a Primary with no backup. Add a second linking device to form a redundant set and provide failure protection to the H1 links connected to the linking device.

➢ **To add a second linking device to form a redundant set**

1. From the ToolboxST Component Editor, add the new linking device's device ID to the Mark VIe controller, then download to the controller to assign the IP address and subnet mask to the linking device.
2. Securely *mount* the PFFAH1A linking device.
3. Connect the H1 links, ensuring they are installed on the same port (FF 1, FF 2, FF 3, or FF 4) on both linking devices.
4. Connect the second linking device to an Ethernet switch or hub different than the one to which the Primary linking device is connected.
5. Connect the serial ports of both linking devices with a RS-232 null modem cable.
6. Connect a 24 V dc power supply to the second linking device. Use a separate or redundant power supply.
7. Turn on the power supply to the second linking device. The boot process takes ~50 seconds. The configuration of the Primary device is copied to the new device and it takes the role of Secondary device in the redundant set. Refer to the table *Device Status Indications* in the section *PFFAH1A LEDs* for indication of proper operation.
8. Configure PFFAH1A linking device redundancy using the ToolboxST application.

9.2.4.3 Troubleshooting

For a redundant set in a Simplex configuration, the linking device that is powered on first operates as the Primary device. If both linking devices are powered on at the same time, the one with the lower IP address operates as the Primary device. If both linking devices in the redundant set are powered on without the serial link installed, they both act as independent, non-redundant Primary devices. If they previously operated as a redundant set, their configuration is identical and they use the same H1 node addresses. This will cause problems on the H1 links. To correct this issue, turn off the power to both linking devices, install the serial link, and turn the power on to both devices.

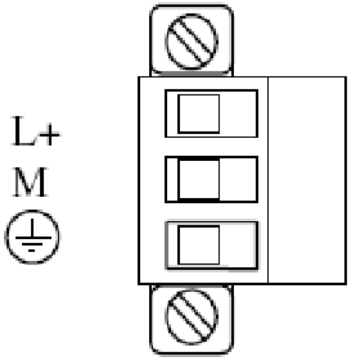
The Primary linking device follows the designated controller, regardless of order of startup. This means that if the R controller is the designated controller, the linking device on the R IONet will attempt to be the Primary device. If for some reason it cannot be the Primary, then the other linking device on the S IONet becomes the Primary and a diagnostic is generated. A diagnostic is generated in this case because there is an issue with the linking device under the dual controller that does not allow it to switch, which means there is no redundancy.

For a redundant set, wait at least one minute between checks of redundant operations such as removing the power supply, the Ethernet cable, or the RS-232 cable from the Primary device. These operations cause a redundancy change-over and the Secondary device must be operational before the next check is done. If the Secondary device is still starting up from the prior change-over, the system breaks down or the configuration information can be lost.

9.2.5 PFFAH1A Operation

9.2.5.1 Power

Power is supplied by a 3-pole terminal block with 0.2 – 2.5 mm², AWG 24-12 wire.



PFFAH1A Power Supply Terminal Block

9.2.5.2 Serial Port

A serial port is provided for use in redundant operation.

PFFAH1A Serial Interface Pin Assignment

Pin	Signal
1	CD
2	RXD
3	TXD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

9.2.5.3 Ethernet Port

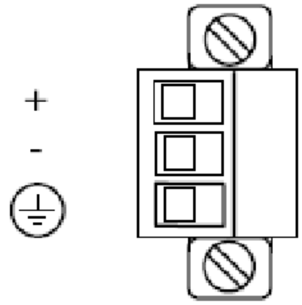
The Ethernet port supports auto negotiation and corresponds to IEEE® 802.3 10Base-T/100Base-TX standards.

PFFAH1A HSE Ethernet Port Pin Assignment

Pin	MDI Signal
1	TD+
2	TD-
3	RD+
4	Not used
5	Not used
6	RD-
7	Not used
8	Not used

9.2.5.4 H1 Connections

The four H1 connections are 3-pole terminal blocks that perform as FOUNDATION fieldbus interfaces to the H1 network and comply with type 114 of the FOUNDATION fieldbus physical layer profile. The H1 connections have no intrinsic safety, operate in standard power signaling and voltage mode, and are separately powered (galvanically isolated). FOUNDATION fieldbus cables can be interchanged and use 0.14 – 1.5 mm^2, AWG 28-16 wire.



PFFAH1A H1 3-pole Terminal Block

9.2.6 Startup Self-tests

Several hardware components are tested during the startup. The test is divided into several sections for runtime reasons. The first part of the test is performed with every start of the PFFAH1A linking device and the following items are checked:

- Access to Random Access Memory (RAM)
- Checksum test flash content (firmware)
- H1 channel (transmission and reception using an internal loopback)
- Interrupt triggering of the H1 controllers

Note System and H1 device diagnostics can be viewed from the ToolboxST application Hardware tab for the linking device.

The RAM test checks whether the entire RAM memory space can be accessed and whether the data are consistent. The checksum test checks the consistency of the flash memory content. If an error is found during this process, startup is stopped. This may require the linking device to be replaced.

9.2.7 PFFAH1A LEDs

The LED block contains LEDs listed in the following table.

LEDs

LED	Color	Indication
PWR	Red/Green	Power supply
LAN	Red/Green	HSE Ethernet Port
ERR	Red/Green	Error status
RUN	Red/Green	Ready
1	Green	Link status FF 1
2	Green	Link status FF 2
3	Green	Link status FF 3
4	Green	Link status FF 4

During the startup process, all LEDs are switched on briefly for an optical performance test. The following tables provide diagnostic information indicated by the LED indications.

Device Status Indications

LED	Display	Description
PWR	Power Supply	
	Off	No supply voltage
	Green	Supply voltage present
LAN	HSE port	
	Off	Ethernet link not established
	Green	Ethernet link has been established
ERR/RUN	Error/Ready combination	
	ERR – Off RUN – Flashing green	Initial boot phase (~7 seconds) During this phase the boot process can be stopped through the serial interface
	ERR – Off RUN – Off	Startup phase (~25 seconds) During this phase the power on self tests are run and the redundancy role is determined.
	ERR – Red RUN – Off	Permanent hardware fault detected during startup A fatal error has been detected during power on self tests.
	ERR – Off RUN – Green	Non-redundant device ready The linking device is operational and it is not a part of a redundant set.
	ERR – Green RUN – Green	Primary device is redundant switch The device is operational and is acting as the Primary device in a redundant set. The Secondary device is ready.
	ERR – Red RUN – Green	Primary device is non-redundant device, failure The device is acting as a primary device in a redundant set or as a non-redundant device, but a failure has been detected. If it is the Primary device of a redundant set, the Secondary device is not ready.
	ERR – Flashing red RUN – Green	Primary device or non-redundant device, hardware failure The device is acting as the Primary device in a redundant set or as a non-redundant device, but a minor hardware failure has been detected during startup.
	ERR – Green RUN – Flashing green	Secondary device operational The device is the Secondary device in a redundant set and is operational. The configuration information has been successfully transferred from the Primary device and the redundancy link is operational.
	ERR – Red RUN – Flashing green	Secondary device not ready The device is acting as the secondary device in a redundant set, but is not ready to take over the primary role due to configuration information not being synchronized or a non-operational redundancy link.
	ERR – Flashing red RUN – Off	Secondary device hardware failure The device is acting as the secondary device in a redundant set, but a hardware failure has been detected.

H1 Channel Status Indications

LED	Display	Description
FF 1 Status of H1 Channel 1	Fast flashing green	Device acts as the Link Active Scheduler (LAS) on channel H1-1 (FF1).
	Slow flashing green	Device is in logical token ring but does not act as the LAS on channel H1-1 (FF1).
	Off	Channel H1-1 (FF1) is not configured or not in the token ring.
FF 2 Status of H1 Channel 2	Fast flashing green	Device acts as the LAS on channel H1-2 (FF2).
	Slow flashing green	Device is in logical token ring but does not act as the LAS on channel H1-2 (FF2).
	Off	Channel H1-2 (FF2) is not configured or not in the token ring.
FF 3 Status of H1 Channel 3	Fast flashing green	Device acts as the LAS on channel H1-3 (FF3).
	Slow flashing green	Device is in logical token ring but does not act as the LAS on channel H1-3 (FF3).
	Off	Channel H1-3 (FF3) is not configured or not in the token ring.
FF 4 Status of H1 Channel 4	Fast flashing green	Device acts as the LAS on channel H1-4 (FF4).
	Slow flashing green	Device is in logical token ring but does not act as the LAS on channel H1-4 (FF4).
	Off	Channel H1-4 (FF4) is not configured or not in the token ring.

9.2.8 Configuration

Configuration of PFFAH1A linking devices and attached segments, fieldbus devices, fieldbus blocks, and related parameters and properties is performed in the ToolboxST application. For further information, refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703), the chapter *Mark VIe FOUNDATION Fieldbus Interface*, the section *Configuration*.

9.3 PFFA Linking Device Specific Alarms

The following diagnostic alarms are specific to the linking device:

1

Description Warning: Communication failure with [ ] FOUNDATION fieldbus device

Possible Cause

- Field device responded to Mark VIe controller with an error
- Request to field device timed out
- Getting initial alert state from device failed
- Receiving an alert failed
- Getting device revision information failed
- Reading block data for EGD failed

Solution During system startup, this diagnostic may become active for a short period. This is normal since it takes some time for the fieldbus devices to initialize. If the warning remains active and/or turns into an error diagnostic, perform the following:

- Check the Ethernet connection between the controller and the PFFA the field device is connected to.
- Check the H1 connection to the PFFA and the field device.
- Cycle power to the field device.
- Cycle power to the PFFA.
- Cycle power to the controller.
- Verify that the correct DD/device revisions are being used.
- From the ToolboxST application, re-build and download the configuration.
- Replace the field device.

2

Description Error: Communication failure with [ ] FOUNDATION fieldbus device

Possible Cause

- The error diagnostic comes when the cause of the warning diagnostic continues to happen and is not resolved.
- Field device responded to the Mark VIe controller with an error
- Request to field device timed out
- Getting initial alert state from device failed
- Receiving an alert failed
- Getting device revision information failed
- Reading block data for EGD failed

Solution The warning diagnostic turns into an error diagnostic when the condition causing the warning continues to occur. Perform the following steps to attempt to clear the diagnostic:

- Check the Ethernet connection between the controller and the PFFA of the problem field device.
- Check the H1 connection to the PFFA and the field device.
- Cycle power to the field device.
- Cycle power to the PFFA.
- Cycle power to the controller.
- Verify that the correct DD/device revisions are being used.
- From the ToolboxST application, re-build and download the configuration.
- Replace the field device.

3

Description I/O Communication failure with [ ] FOUNDATION fieldbus device

Possible Cause

- PFFA switchover occurred
- Field device not detected but is configured in the ToolboxST application
- Misconfigured field device

Solution If a PFFA switchover occurred, field devices are removed and then re-added. When this occurs, the diagnostic will be active for a short period, then become inactive.

- Check the field device connection to the PFFA.
- Check the connection of the controller to the PFFA.
- Cycle power to the field device.
- Cycle power to the controller.
- Verify that the correct DD/device revisions are being used.
- From the TooboxST Commissioning Wizard, verify the correct configuration.
- From the ToolboxST application, re-build and download the configuration.
- Replace the field device.

4

Description Control/Status communication error with the controller

Possible Cause

- PFFA responded to Mark VIe controller with an error
- Request to the PFFA timed out

Solution

- Check the Ethernet connection between the controller and the PFFA.
- Cycle power to the PFFA and the controller.
- From the ToolboxST application, re-build and download the configuration.
- Replace the PFFA.

5

Description Could not take over the primary linking device role

Possible Cause The secondary PFFA is on the designated controller's IONet. Control was not compromised because one of the non-designated controllers is controlling the outputs. This could be due to the following causes:

- Segment connection was disconnected on the primary PFFA
- Field devices not detected on the secondary PFFA but are present on the primary PFFA
- Broken Ethernet connection to the PFFA
- Power disconnected to the PFFA
- Internal hardware fault in the PFFA

Solution

- Check the segment connections on the PFFA.
- Check the field device connections to the PFFA.
- Check the Ethernet connection from the PFFA to the controller.
- Check the power connection to the PFFA.
- Replace the PFFA.

6

Description Mismatch between configuration and actual device [ ]

Possible Cause There is a PD Tag and/or Device ID mismatch between the ToolboxST application and real the device.

Solution

- From the ToolboxST Commissioning Wizard, check the PD Tag and/or Device ID.
- From the ToolboxST application, re-build and download the configuration.

250

Description ToolboxST application detects I/O communication failure between PFFA [ ] and controller

Possible Cause

- PFFA did not complete startup
- PFFA configuration files are missing
- PFFA restarted
- PFFA configured for Hot Backup, but only one network is connected
- Serial connection between PFFA modules is broken
- Network issue

Solution

- If the control/status communication is working correctly, any additional diagnostics should indicate the cause of the problem.
- Perform a build and download parameters to the PFFA and controller.
- Verify that the serial cable is attached correctly.
- Verify that the Ethernet cables and network switches are operating correctly.
- Manually restart the PFFA.

Note This alarm is not reported to the WorkstationST Alarm Viewer. This alarm is generated by the ToolboxST application, not by the I/O pack or module.

251

Description ToolboxST application cannot retrieve PFFA diagnostics information [ ]

Possible Cause

- Communication program failure
- PFFA is unable to retrieve IP address
- Wrong device ID and/or PD Tag in the ToolboxST configuration
- Wrong PFFA configuration in the ToolboxST application
- Wrong PFFA network connection in the ToolboxST configuration
- PFFA is configured in the ToolboxST application, but the configuration was not downloaded to controller

Solution

- Verify that the PFFA configuration (such as Version, Device ID, PD Tag) matches the actual hardware.
- Perform a build and download the configuration to the controller, wait for the PFFA communication status to change, then scan and download to the PFFA.
- Check the network cables for proper connection.
- Verify that the switch is functioning correctly.
- Manually restart the PFFA.

Note This alarm is not reported to the WorkstationST Alarm Viewer. This alarm is generated by the ToolboxST application, not by the I/O pack or module.

252

Note This alarm is obsolete.

Description There is a decommissioned device(s) on segment [ ]

Possible Cause

- Decommissioned devices exist on the segment
- ToolboxST configuration is not matching the target system
- Communication program failure

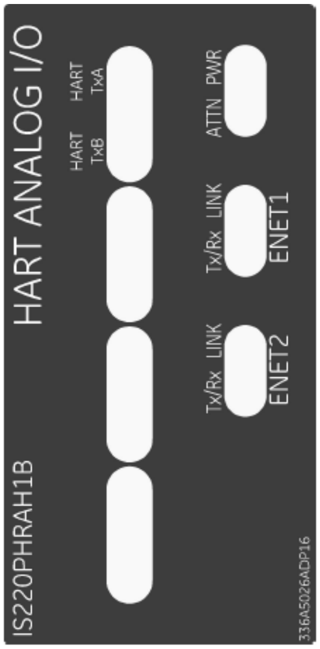
Solution

- Examine the segment and commission all devices.
- Match the configuration with the target system, then perform a build and download the configuration to the controller.
- Manually restart the PFFA or module.

Notes

10 PHRA, YHRA HART® Analog I/O Modules

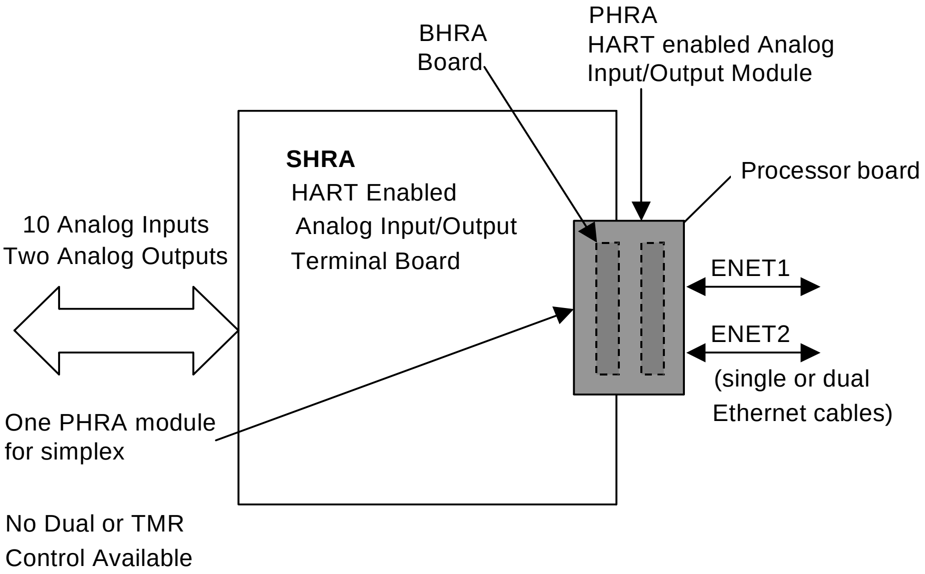
10.1 Mark VIe PHRA HART Analog I/O Pack



The Highway Addressable Remote Transducer (HART®) Enabled Analog I/O pack (PHRA) provides the electrical interface between one or two I/O Ethernet networks and an analog input/output terminal board. The PHRA contains a BPPx processor board common to the distributed I/O packs and an acquisition board specific to the analog input function.

The I/O pack is capable of handling up to 10 analog inputs, the first eight of which can be configured as ±5 V inputs, or 4-20 mA current loop inputs. The last two inputs can be configured as ±1 mA or 4-20 mA current inputs. The load termination resistors for current loop inputs are located on the terminal board and voltage is sensed across these resistors by the PHRA. The PHRA also includes support for two 4-20 mA current loop outputs. In addition, in 4-20 mA mode the PHRA can relay HART messages between HART enabled field devices and an Asset Management System (AMS). These HART enabled field devices can be connected through any of the inputs or outputs.

Input to the I/O pack is through dual RJ-45 Ethernet connectors and a 3-pin power input. Output is through a DC-62 pin connector that connects directly with the associated terminal board connector. Visual diagnostics are provided through indicator LEDs.



10.1.1 Compatibility

The PHRA I/O pack includes one of the following compatible BPPx processor boards:

- The PHRAH1A contains a BPPB processor board.
- The PHRAH1B contains a functionally compatible BPPC processor board that is supported in the ControlST* software suite V04.07 and later.

The PHRA I/O pack is compatible with the SHRA HART enabled analog I/O simplex terminal board.

Terminal Board	Terminal Type	Available Redundancy
SHRAH1A, S1A	Fixed	Simplex
SHRAH2A, S2A	Pluggable	

10.1.2 Installation

➢ **To install the PHRA I/O pack**

1. Securely mount the SHRA terminal board.
2. Directly plug one PHRA I/O pack into the SHRA DC-62 pin connector.
3. Mechanically secure the I/O pack using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right angle force applied to the DC-62 pin connector between the I/O pack and the terminal board. The adjustment should only be required once in the service life of the product.
4. Plug in one or two Ethernet cables depending on the system configuration. The pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
5. Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to remove power from the cable before plugging it in because the I/O pack has inherent soft-start capability that controls current inrush on power application.
6. Use the ToolboxST* application to configure the I/O pack as necessary.

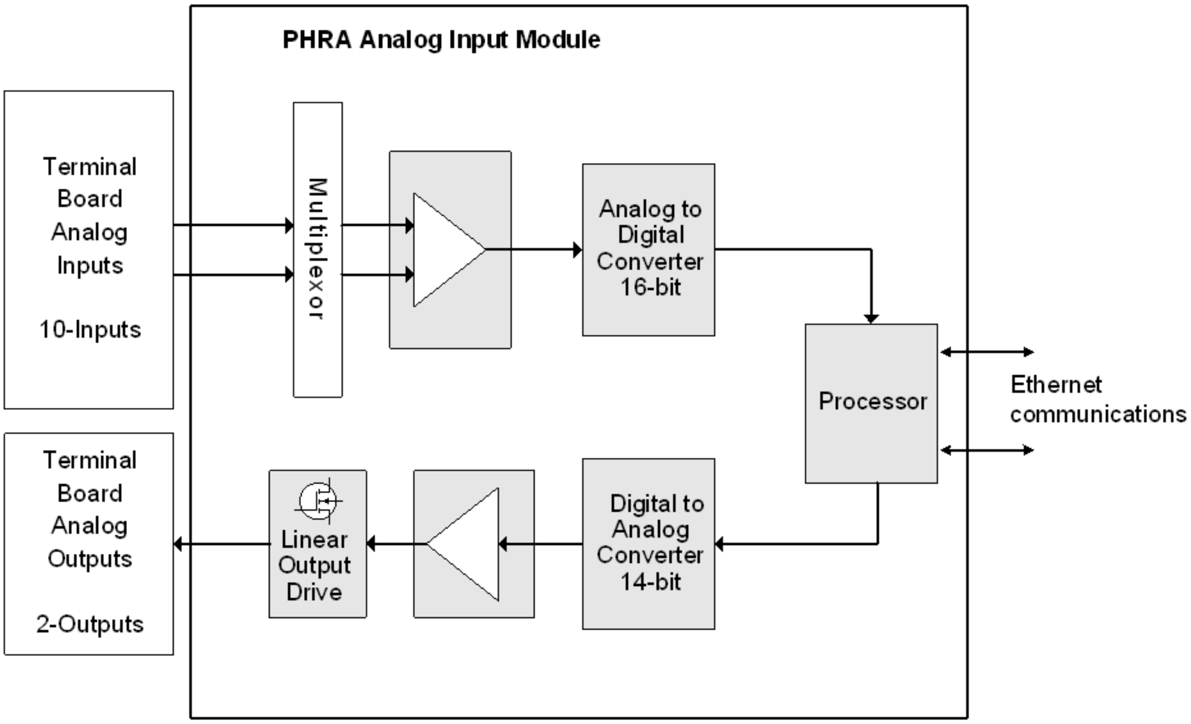
10.1.3 Operation

The following features are common to the distributed I/O modules:

- *BPPx Processor*
- *Processor LEDs*
- *Power Management*
- *ID Line*
- *I/O Module Common Diagnostic Alarms*

10.1.3.1 Analog Input Hardware

The PHRA accepts input voltage signals from the terminal board for all 10 input channels. The analog input section consists of an analog multiplexer block, several gain and scaling selections, and a 16-bit analog-to-digital converter (DAC).

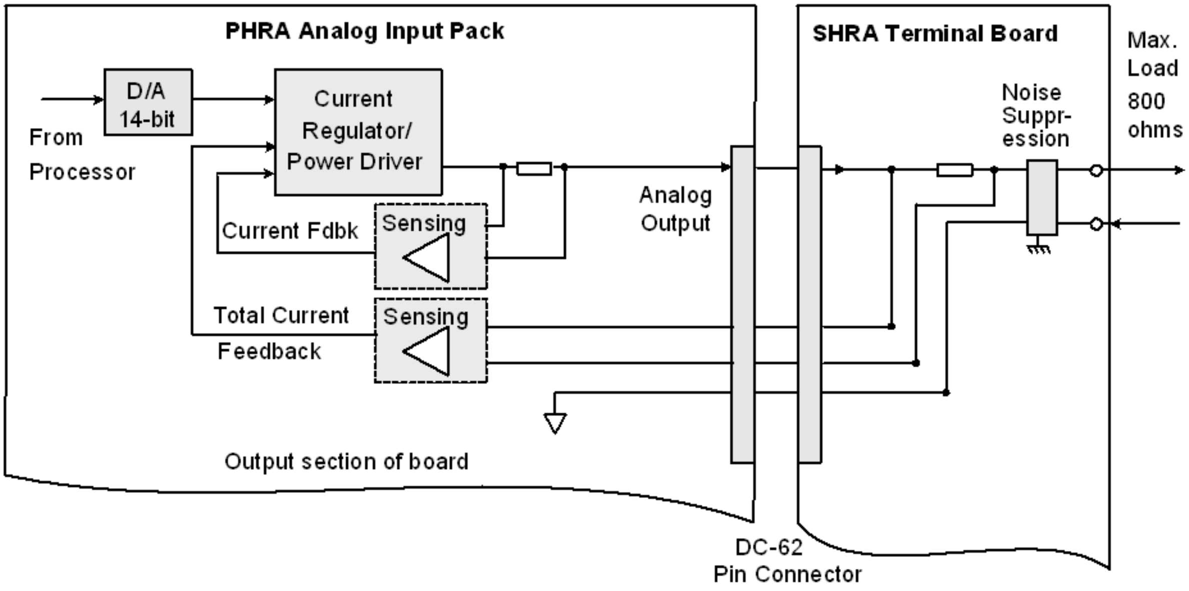

PHRA Analog Input Module
Terminal Board Analog Inputs
10-Inputs
Multiplexor
Analog to Digital Converter 16-bit
Processor
Ethernet communications
Terminal Board Analog Outputs
2-Outputs
Linear Output Drive
Digital to Analog Converter 14-bit

The inputs can be individually configured as ±5 V scale signals, depending on the input configuration. The terminal board provides a 250 Ω burden resistor when configured for current inputs yielding a 5 V signal at 20 mA. These analog input signals are first passed through a second order, passive, low pass filter network with poles at 12.5 Hz and 48.3 Hz. Voltage signal feedbacks from the analog output circuits and calibration voltages are also sensed by the PHRA analog input section.

10.1.3.2 Analog Output

The PHRA includes two 4-20 mA analog outputs capable of 18 V compliance. A 14-bit DAC commands a current reference to the current regulator loop in the PHRA that senses current both in the PHRA pack and on the terminal board. Analog output status feedbacks for each output include:

- Current reference voltage
- Individual current (output current sourced from within the PHRA)
- Total current (as sensed from the terminal board)



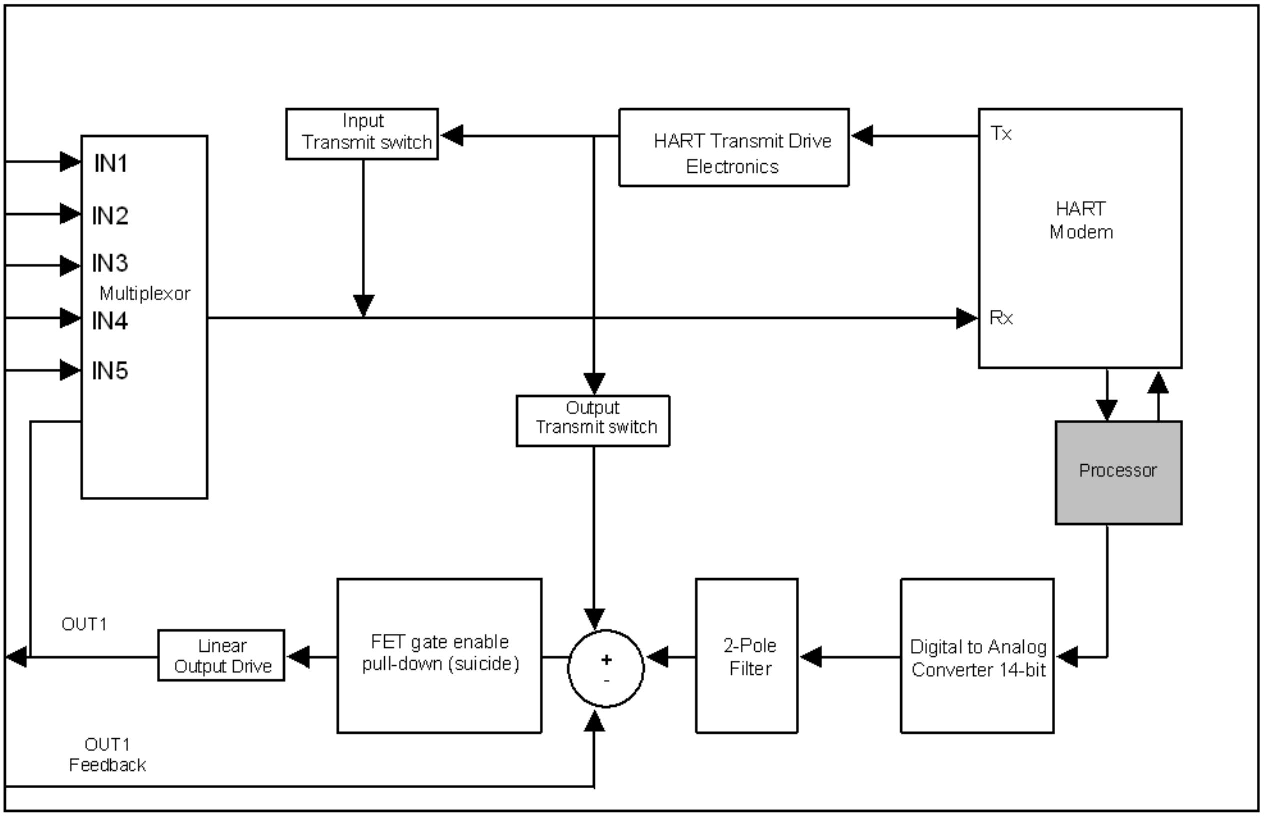
10.1.3.3 HART Hardware

All inputs and outputs on the PHRA are HART enabled. This means there are 12 individual HART channels, with 10 channels for the analog inputs and two channels for the outputs. These 12 channels are served by a pair of HART modems so that each modem is associated with six HART channels. Inputs 1 through 5 and output 1 are multiplexed down to HART modem A. Inputs 6 through 10 and output 2 are multiplexed down to HART modem B.

HART Modem Associations

HART channel	PHRA I/O Analog	Served by Modem
1	Input #1	A
2	Input #2	A
3	Input #3	A
4	Input #4	A
5	Input #5	A
6	Output #1	A
7	Input #6	B
8	Input #7	B
9	Input #8	B
10	Input #9	B
11	Input #10	B
12	Output #2	B

The number of active channels a modem is serving greatly impacts the HART data update time. If one of the six channels served by a HART modem is active, the modem is dedicated to a single field device and, under normal operating conditions, ToolboxST data associated with this device is updated roughly once per second. If all six channels are in use, roughly eight seconds will pass between updates.



Analog IO HART Interface — Quantity 2

10.1.4 Specifications

Item	PHRA Specification
Number of Channels	12 channels per terminal board (10 AI, 2 AO)
Input Span	4-20 mA dc, ±5 V dc, (Inputs 1-8) 4-20 mA or ±1 mA (Inputs 9-10)
Input Converter Resolution	16-bit analog-to-digital converter
Scan Time	Normal scan 5 ms (200 Hz). *Controller frame rate is 100 Hz.*
Measurement Accuracy	Better than 0.1% full scale over the temperature range -30 to 65°C. Typical accuracy at 25°C is 0.007% full scale.
Noise Suppression on Inputs	The ten circuits have a hardware filter with two poles at 12.5 Hz and 48.3 Hz. A software filter, using a two-pole, low-pass filter, is configurable for: 0, .75, 1.5 Hz, 3 Hz, 6 Hz, 12 Hz
Common Mode Rejection	Ac common mode rejection 60 dB at 60 Hz, with up to ±5 V common mode voltage. Dc common mode rejection 80 dB with -5 to +7 peak V common mode voltage
Common Mode Voltage Range	±5 V
Output Converter	14-bit D/A converter with 0.5% accuracy
Output Load	800 Ω for 0-20 mA output
Size	8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in x 1.65 in x 4.78 in)
Technology	Surface-mount
Ambient Rating for Enclosure Design†	PHRAH1B is rated from -40 to 70°C (-40 to 158 °F) PHRAH1A is rated from -30 to 65°C (-22 to 149 °F)

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

10.1.5 Diagnostics

The I/O pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set
- Each analog input has hardware limit checking based on configurable high and low levels for 4-20 mA inputs and preset (non-configurable) levels for ± 5 V, and ± 1 mA inputs. If the limit is exceeded, a logic signal (L3DIAG_xxxx) is set and the input is marked as unhealthy. The logic signal (L3DIAG_xxxx) refers to the entire board.
- Each input has system limit checking based on configurable high and low levels. These limits can be used to generate alarms, to enable and disable, and as latching and non-latching. RSTSYS resets the out of limits.
- The analog input hardware includes precision reference voltages in each scan. Measured values are compared against expected values and are used to confirm health of the analog to digital converter circuits.
- Analog output current is sensed on the terminal board using a small burden resistor. The I/O pack conditions this signal and compares it to the commanded current to confirm health of the digital to analog converter circuits.
- The analog output suicide relay is continuously monitored for agreement between commanded state and feedback indication.

Details of the individual diagnostics are available from the ToolboxST application. The diagnostic signals can be individually latched, and then reset with the RSTDIAG signal if they go healthy.

10.1.6 Configuration

10.1.6.1 Parameters

Parameter	Description	Choices
SystemLimits	Allows user to temporarily disable all system limit checks for testing purposes. Setting this parameter to Disable will cause a diagnostic alarm to occur.	Enable, Disable (default is Enable)
Min_ MA_Input	Select minimum current for healthy 4-20 mA input	0 to 22.5 mA
Max_ MA_Input	Select maximum current for healthy 4-20 mA input	0 to 22.5 mA
AMS_Msg_Priority	AMS messages have priority over controlled messages, if enabled	Enable, Disable
AMS_Msgs_Only	AMS messages only, do not send any control messages. Generates alarm 160 when enabled.	Enable, Disable
AMS_Mux_Scans_Permited	Allow AMS scan commands for HART message 1 and 2 (HART message 3 is always allowed)	Enable, Disable
Max_MA_Hart_Output	Minimum current sent to a HART enabled port. HART COMM will not be possible during offline modes if value is set less than 4 mA	0 to 22.5 mA

10.1.6.2 Inputs

Input Name	Input Description	Choices
AnalogIn1-10	First of 10 Analog Inputs – board point	(Input FLOAT)
Input Type	Current or voltage input type	Unused, 4-20 mA, ±5 V
Low_Input	Value of input current (mA) or voltage (V) at low end of input scale	-10 to +20
Low_Value	Value of input in engineering units at Low_Input	-3.4082 e + 038 to 3.4028 e + 038
High_Input	Value of input current (mA) or voltage (V) at high end of input scale	-10 to +20
High_Value	Value of input in engineering units at High_Input	-3.4082 e + 038 to 3.4028 e + 038
Input _Filter	Bandwidth of input signal filter	Unused, 0.75, 1.5 Hz, 3 Hz, 6 Hz, 12 Hz
Hart_Enable	Allow the HART Protocol on this IO point. This must be set to true if HART messages are needed from this field device	Enable, Disable
Hart_CtrlVars	Number of variables to read from the device. Set to zero if not used.	0-5
Hart_ExStatus	Number of extended status bytes to read from the device. Set to zero if not needed for control.	0-26
Hart_MfgID	HART field device's manufacturers code. A diagnostic alarm is sent if the field device ID differs from this value and the value is non-zero. This value can be uploaded from the PHRA if the field device is connected. (Right-click on device name and select Update HART IDS)	0-255
Hart_DevType	HART Field Device – Type of device (refer to Hart_ MfgID)	0-255
Hart_DevID	HART Field Device – Device ID (refer to Hart_MfgID)	0-116777215
SysLim1Enabl	Enable System Limit 1 fault check	Enable, Disable

Input Name	Input Description	Choices
SysLim1Latch	System Limit 1 fault latch - if set, requires a Reset System Limits (RSTSYS) on SYS_OUTPUTS block to clear	Latch, NotLatch
SysLim1Type	System Limit 1 Check Type	>= or <=
SysLim1	System Limit 1 in engineering units	-3.4082 e + 038 to 3.4028 e + 038
SysLim2Enabl	Enable System Limit 2 fault check	Enable, Disable
SysLim2Latch	System Limit 2 fault latch - if set, requires a Reset System Limits (RSTSYS) on SYS_OUTPUTS block to clear	Latch, NotLatch
SysLim2Type	System Limit 2 Check Type	>= or <=
SysLimit2	System Limit 2 in Engineering Units	-3.4082 e + 038 to 3.4028 e + 038
DiagHighEnab	Enables the generation of a high limit diagnostic alarm when the value of the 4-20 mA input is greater than the value of parameter Max_MA_Input	Enable, Disable
DiagLowEnab	Enables the generation of a low limit diagnostic alarm when the value of the 4-20 mA input is less than the value of parameter Min_MA_Input	Enable, Disable

10.1.6.3 Outputs

Output Name	Output Description	Choices
AnalogOut1-2	First of two analog outputs - board point	Point edit (Output FLOAT)
Output_MA	Type of output current, mA selection	Unused, 0-20 mA
Output_State	State of the outputs when offline. When the PAIC loses communication with the controller, this parameter determines how it drives the outputs: • PwrDownMode - Open the output relay and drive outputs to zero current. • HoldLastVal - Hold the last value received from the controller. • Output_Value - Go to the configured output value set by the parameter Output_Value.	PwrDownMode HoldLastVal Output_Value
Output_Value	Pre-determined value for the outputs	
Low_MA	Output mA at low value	0 to 20 mA
Low_Value	Output in Engineering Units at Low_MA	-3.4082 e + 038 to 3.4028 e + 038
High_MA	Output mA at high value	0 to 20 mA
High_Value	Output value in Engineering Units at High_MA	-3.4082 e + 038 to 3.4028 e + 038
D/A Err Limit	Difference between D/A reference and output, in %	0 to 100 %
Hart_Enable	Allow the HART Protocol on this IO point. This must be set to true if HART messages are needed from this field device	Enable, Disable
Hart_CtrlVars	Number of control variables to read from the device. Set to zero if not needed for control.	0-5
Hart_ExStatus	Number of extended status bytes to read from the device. Set to zero if not needed for control.	0-26

Output Name	Output Description	Choices
Hart_MfgID	HART field device's manufacturers code. A diagnostic alarm is sent if the field device ID differs from this value and the value is non-zero. This value can be uploaded from the PHRA if the field device is connected. (Right-click on device name and select Update HART IDS.)	0-255
Hart_DevType	HART Field Device – Type of device (refer to Hart_MfgID)	0-255
Hart_DevID	HART Field Device – Device ID (refer to Hart_MfgID)	0-116777215

10.1.6.4 Variables

Variable Name	Variable Description	Direction	Type
L3DIAG_PHRA	Board diagnostic	Input	BIT
LINK_OK_PHRA	Link diagnostic input	Input	BIT
ATTN_PHRA	Module diagnostic	Input	BIT
PS18V_PHRA_R	I/O 18 V power supply indication	Input	BIT
PS28V_PHRA_R	I/O 28 V power supply indication	Input	BIT
IOPackTmpr	I/O pack temperature	Input	FLOAT
MuxHealth1	Health bit for PHRA HART multiplexer	Input	BIT
SysLimit1_1	System Limit 1	Input	BIT
↓	↓	Input	BIT
SysLimit1_10	System Limit 1	Input	BIT
SysLimit2_1	System Limit 2	Input	BIT
↓	↓	Input	BIT
SysLimit2_10	System Limit 2	Input	BIT
Out1MA	Feedback, Total output current, mA	Input	FLOAT
Out2MA	Feedback, Total output current, mA	Input	FLOAT

10.1.6.5 HART Signal Definitions

Each HART field device has a set of HART signals that are read from the field device. These signals are prefixed with either HIx_ or HOx_ where x is 1-10 for input channels and 1-2 for output channels.

Signal	Type	Description
Hxx_CommCnt	Integer	Number of times the CommStat signal was not zero after a HART message
Hxx_CommStat	Bit encoded integer	HART Communication status Bit 1 – RX buffer overflow Bit 3 – Checksum error Bit 4 – Framing error Bit 5 – Overrun error Bit 6 – Parity error
Hxx_DevCnt	Integer	Number of times the DevStat signal was not zero after a HART message.
Hxx_DevStat	Bit encoded integer	Field Device Status: bits 0-7 Bit 0 – Primary variable out of limits Bit 1 – Non primary var out of limits Bit 2 – Analog output saturated Bit 3 – Analog output current fixed Bit 4 – More status available (ExStat) Bit 5 – Cold start Bit 6 – Configuration changed Bit 7 – Field device malfunction Command response byte: bits 8-15 2: Invalid selection requested 3: Passed parameter too large 4: Passed parameter too small 5: Too few bytes received 6: Device specific device error 7: In write protect mode 8-15: Device specific 16: Access restricted 32: Device is busy 64: Command not implemented
Hxx_DevRev	Integer	Field Device - Device revision code as read from the device.
Hxx_HwSwRev	Integer	Byte 0 - Field device software revision Byte 1 - Field device hardware revision
Hxx_mA	Float	Field Parm 1 – current reading of the primary signal
Hxx_PV †	Float	Field Device Specific Control Parm 2 - Primary field device value
Hxx_SV †	Float	Field Device Specific Control Parm 3 - Secondary value
Hxx_TV †	Float	Field Device Specific Control Parm 4 -Third value
Hxx_FV †	Float	Field Device Specific Control Parm 5 -Fourth value
† To view these variables, the Hart_CtrlVars parameter must have a value greater than zero.		

10.1.6.6 Extended Status Bits

The extended status bits are device-specific, and can be interrogated by using an AMS system. In general, the status bits are grouped as follows:

Bytes 0-5: Device specific status

Bytes 6-7: Operational modes

Bytes 8-10: Analog output saturation

Bytes 11-13: Analog output current fixed

Bytes 14-26: Device-specific

Each field device supports a specific number of control parameters and extended status bits. Refer to the *Field Device* documentation to determine the correct number and configure the ToolboxST application accordingly. A diagnostic alarm message will be generated if the Field Device and ToolboxST configuration do not match.

Hxx_ExStat_1	Bit Encoded	Extended Status Bytes 1-4
Hxx_ExStat_2	Bit Encoded	Extended Status Bytes 5-8
Hxx_ExStat_3	Bit Encoded	Extended Status Bytes 9-12
Hxx_ExStat_4	Bit Encoded	Extended Status Bytes 13-16
Hxx_ExStat_5	Bit Encoded	Extended Status Bytes 17-20
Hxx_ExStat_6	Bit Encoded	Extended Status Bytes 21-24
Hxx_ExStat_7	Bit Encoded	Extended Status Bytes 25-26

10.2 PHRA Specific Alarms

The following alarms are specific to the PHRA I/O pack.

32-41

Description Analog Input [ ] unhealthy

Possible Cause

- Excitation to the transducer is wrong or missing.
- The transducer may be faulty.
- The analog input current/voltage input is beyond the specified range.
- The terminal board jumper settings do not match the ToolboxST configuration.
- There may be an open or short-circuit on the input.

Solution

- Check the field wiring and connections to the indicated analog input channel.
- Check the field device for failure.
- Verify that the configuration matches the terminal board jumper settings for the indicated analog input channel.

46-47

Description Output [ ] total current feedback unhealthy

Possible Cause

- The commanded output is beyond the range of the output.
- There may be a field wiring problem.
- There may be a field device problem.
- There may be an open loop or too much resistance in the loop.

Solution

- Verify that the commanded output is within the range of the output.
- Confirm that the I/O pack 28 V input power is correct.
- Check the field wiring and the device.
- Replace the I/O pack.

48-49

Description Output [ ] Internal reference current unhealthy

Possible Cause

- There may be an I/O pack failure.

Solution

- Confirm that the I/O pack 28 V input power is correct.
- Replace the I/O pack.

66-67

Description Output [ ] Individual current too high relative to total current

Possible Cause A disagreement has been detected between the output current sensing inside the I/O pack and the current sensing on SHRA.

- A hardware failure is causing the I/O pack to drive too much output current.

Solution

- Check the I/O pack mounting on the SHRA.
- Confirm that the field wiring and load are correct.
- Check the output configuration.
- Replace the SHRA and the I/O pack.

70-71

Description Output [ ] Total current varies from reference current

Possible Cause

- There may be a field wiring problem.
- There may be an open-circuit on the output, or the total loop resistance is too high.
- The command is beyond the range of the output.

Solution

- Check the field wiring and the device.
- Check the output configuration.
- Verify that the commanded output is within output range.
- Check the I/O pack mounting on the SHRA.
- Replace the I/O pack.

74-75

Description Output [ ] Reference current error

Possible Cause The difference between the commanded output current and current feedback on the terminal board is greater than **D/A_ErrLimit** (%).

- There may be an open-circuit on the output.
- The command is beyond the range of the output.

Solution

- Check the field wiring and the device.
- Verify that the value of **D/A_ErrLimit** is set correctly.
- Verify that the commanded output is within the output range.
- Replace the I/O pack.

78-79

Description Output [ ] individual current feedback unhealthy

Possible Cause

- The commanded output is beyond the range of the output.
- There may be a field wiring problem.
- There may be a field device problem.
- There is an open loop or too much resistance in the loop.
- There may be an I/O pack failure.
- There may be a terminal board failure.

Solution

- Verify that the commanded output is within the range of the output.
- Confirm the correct I/O pack 28 V input power.
- Check the field wiring and the device.
- Replace the I/O pack.

86-87

Description Output [ ] 20/200 mA selection non-functional

Possible Cause N/A

Solution N/A

92-93

Description Output [ ] Suicide on overcurrent

Possible Cause

- Hardware failure in I/O pack.

Solution

- Replace I/O pack.

99

Description Hart Input 1 Channel 1 not initialized

Possible Cause An enabled Hart input channel does not respond.

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

100

Description Hart Input 2 Channel 2 not initialized

Possible Cause An enabled Hart input channel does not respond.

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

101

Description Hart Input 3 Channel 3 not initialized

Possible Cause An enabled Hart input channel does not respond.

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

102

Description Hart Input 4 Channel 4 not initialized

Possible Cause An enabled Hart input channel does not respond.

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

103

Description Hart Input 5 Channel 5 not initialized

Possible Cause An enabled Hart input channel does not respond.

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

104

Description Hart Output 1 Channel 6 not initialized

Possible Cause An enabled Hart output channel does not respond.

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

105

Description Hart Input 6 Channel 7 not initialized

Possible Cause An enabled Hart input channel does not respond.

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

106

Description Hart Input 7 Channel 8 not initialized

Possible Cause An enabled Hart input channel does not respond.

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

107

Description Hart Input 8 Channel 9 not initialized

Possible Cause An enabled Hart input channel does not respond.

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

108

Description Hart Input 9 Channel 10 not initialized

Possible Cause An enabled Hart input channel does not respond.

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

109

Description Hart Input 10 Channel 11 not initialized

Possible Cause An enabled Hart input channel does not respond.

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

110

Description Hart Output 2 Channel 12 not initialized

Possible Cause An enabled Hart output channel does not respond.

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

111

Description Hart Input 1 Channel 1 address mismatch

Possible Cause The device ID in the ToolboxST configuration does not match the field device.

Solution

- Verify that the correct field device is connected to the I/O point.
- If so, either set the three ID fields to zero, or upload the device ID from the field device.

112

Description Hart Input 2 Channel 2 address mismatch

Possible Cause The device ID in the ToolboxST configuration does not match the field device.

Solution

- Verify that the correct field device is connected to the I/O point.
- If so, either set the three ID fields to zero, or upload the device ID from the field device.

113

Description Hart Input 3 Channel 3 address mismatch

Possible Cause The device ID in the ToolboxST configuration does not match the field device.

Solution

- Verify that the correct field device is connected to the I/O point.
- If so, either set the three ID fields to zero, or upload the device ID from the field device.

114

Description Hart Input 4 Channel 4 address mismatch

Possible Cause The device ID in the ToolboxST configuration does not match the field device.

Solution

- Verify that the correct field device is connected to the I/O point.
- If so, either set the three ID fields to zero, or upload the device ID from the field device.

115

Description Hart Input 5 Channel 5 address mismatch

Possible Cause The device ID in the ToolboxST configuration does not match the field device.

Solution

- Verify that the correct field device is connected to the I/O point.
- If so, either set the three ID fields to zero, or upload the device ID from the field device.

116

Description Hart Output 1 Channel 6 address mismatch

Possible Cause The device ID in the ToolboxST configuration does not match the field device.

Solution

- Verify that the correct field device is connected to the I/O point.
- If so, either set the three ID fields to zero, or upload the device ID from the field device.

117

Description Hart Input 6 Channel 7 address mismatch

Possible Cause The device ID in the ToolboxST configuration does not match the field device.

Solution

- Verify that the correct field device is connected to the I/O point.
- If so, either set the three ID fields to zero, or upload the device ID from the field device.

118

Description Hart Input 7 Channel 8 address mismatch

Possible Cause The device ID in the ToolboxST configuration does not match the field device.

Solution

- Verify that the correct field device is connected to the I/O point.
- If so, either set the three ID fields to zero, or upload the device ID from the field device.

119

Description Hart Input 8 Channel 9 address mismatch

Possible Cause The device ID in the ToolboxST configuration does not match the field device.

Solution

- Verify that the correct field device is connected to the I/O point.
- If so, either set the three ID fields to zero, or upload the device ID from the field device.

120

Description Hart Input 9 Channel 10 address mismatch

Possible Cause The device ID in the ToolboxST configuration does not match the field device.

Solution

- Verify that the correct field device is connected to the I/O point.
- If so, either set the three ID fields to zero, or upload the device ID from the field device.

121

Description Hart Input 10 Channel 11 address mismatch

Possible Cause The device ID in the ToolboxST configuration does not match the field device.

Solution

- Verify that the correct field device is connected to the I/O point.
- If so, either set the three ID fields to zero, or upload the device ID from the field device.

122

Description Hart Output 2 Channel 12 address mismatch

Possible Cause The device ID in the ToolboxST configuration does not match the field device.

Solution

- Verify that the correct field device is connected to the I/O point.
- If so, either set the three ID fields to zero, or upload the device ID from the field device.

123

Description PHRA Hart Module Modified

Possible Cause The configuration of the HART multiplexer on the PHRA card was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault. This requires that the diagnostic first be unlatched and then reset.

➢ To unlatch this diagnostic

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

124

Description Hart Input 1 Channel 1 Field Device Modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ **To unlatch this diagnostic**

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

125

Description Hart Input 2 Channel 2 Field Device Modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ **To unlatch this diagnostic**

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

126

Description Hart Input 3 Channel 3 Field Device Modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ **To unlatch this diagnostic**

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

127

Description Hart Input 4 Channel 4 Field Device Modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ To unlatch this diagnostic

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

128

Description Hart Input 5 Channel 5 Field Device Modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ To unlatch this diagnostic

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

129

Description Hart Output 1 Channel 6 Field Device Modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ To unlatch this diagnostic

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

130

Description Hart Input 6 Channel 7 Field Device Modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ **To unlatch this diagnostic**

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

131

Description Hart Input 7 Channel 8 Field Device Modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ **To unlatch this diagnostic**

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

132

Description Hart Input 8 Channel 9 Field Device Modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ **To unlatch this diagnostic**

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

133

Description Hart Input 9 Channel 10 Field Device Modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ To unlatch this diagnostic

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

134

Description Hart Input 10 Channel 11 Field Device Modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ To unlatch this diagnostic

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

135

Description Hart Output 2 Channel 12 Field Device Modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ To unlatch this diagnostic

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

136

Description Hart Input 1 Chan 1 Control Parm Mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in Hart Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

137

Description Hart Input 2 Chan 2 Control Parm Mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in Hart Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

138

Description Hart Input 3 Chan 3 Control Parm Mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in Hart Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

139

Description Hart Input 4 Chan 4 Control Parm Mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in Hart Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

140

Description Hart Input 5 Chan 5 Control Parm Mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in Hart Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

141

Description Hart Output 1 Chan 6 Control Parm Mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in Hart Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

142

Description Hart Input 6 Chan 7 Control Parm Mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in Hart Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

143

Description Hart Input 7 Chan 8 Control Parm Mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in Hart Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

144

Description Hart Input 8 Chan 9 Control Parm Mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in Hart Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

145

Description Hart Input 9 Chan 10 Control Parm Mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in Hart Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

146

Description Hart Input 10 Chan 11 Control Parm Mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in Hart Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

147

Description Hart Output 2 Chan 12 Control Parm Mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in Hart Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

148

Description Hart Input 1 Chan 1 Extended Status Mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in Hart Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

149

Description Hart Input 2 Chan 2 Extended Status Mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in Hart Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

150

Description Hart Input 3 Chan 3 Extended Status Mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in Hart Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

151

Description Hart Input 4 Chan 4 Extended Status Mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in Hart Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

152

Description Hart Input 5 Chan 5 Extended Status Mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in Hart Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

153

Description Hart Output 1 Chan 6 Extended Status Mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in Hart Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

154

Description Hart Input 6 Chan 7 Extended Status Mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in Hart Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

155

Description Hart Input 7 Chan 8 Extended Status Mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in Hart Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

156

Description Hart Input 8 Chan 9 Extended Status Mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in Hart Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

157

Description Hart Input 9 Chan 10 Extended Status Mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in Hart Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

158

Description Hart Input 10 Chan 11 Extended Status Mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in Hart Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

159

Description Hart Output 2 Chan 12 Extended Status Mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in Hart Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

160

Description Hart Control Messages disabled. AMS Hart messages only

Possible Cause The **AMS_Msgs_Only** parameter is **Enabled**. No control messages are sent. This parameter overrides the values in the **Hart_CtrlVars** and **Hart_ExStatus** for each individual channel.

Solution

- To send AMS messages only, but clear this alarm: Set the **AMS_Msgs_Only** parameter to **Disabled** and set each channel's **Hart_CtrlVars** and **Hart_ExStatus** to zero.
- To allow control messages *and* AMS messages, set **AMS_Msgs_Only** to **Disabled**.

161

Description Hart Input 1 Chan 1 - Field device not write protected in locked mode

Possible Cause The field device for this channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

162

Description Hart Input 2 Chan 2 - Field device not write protected in locked mode

Possible Cause The field device for this channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

163

Description Hart Input 3 Chan 3 - Field device not write protected in locked mode

Possible Cause The field device for this channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

164

Description Hart Input 4 Chan 4 - Field device not write protected in locked mode

Possible Cause The field device for this channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

165

Description Hart Input 5 Chan 5 - Field device not write protected in locked mode

Possible Cause The field device for this channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

166

Description Hart Output 1 Chan 6 - Field device not write protected in locked mode

Possible Cause The field device for this channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

167

Description Hart Input 6 Chan 7 - Field device not write protected in locked mode

Possible Cause The field device for this channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

168

Description Hart Input 7 Chan 8 - Field device not write protected in locked mode

Possible Cause The field device for this channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

169

Description Hart Input 8 Chan 9 - Field device not write protected in locked mode

Possible Cause The field device for this channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

170

Description Hart Input 9 Chan 10 - Field device not write protected in locked mode

Possible Cause The field device for this channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

171

Description Hart Input 10 Chan 11 - Field device not write protected in locked mode

Possible Cause The field device for this channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

172

Description Hart Output 2 Chan 12 - Field device not write protected in locked mode

Possible Cause The field device for this channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

173

Description Pack internal reference voltage out of limits

Possible Cause The calibration reference voltage for the analog inputs is more than ±5% from the expected value, which may indicate a hardware failure.

Solution

- Check the I/O pack ground quality through the mounting bolts.
- Cycle power on the I/O pack.
- Replace the I/O pack.

174

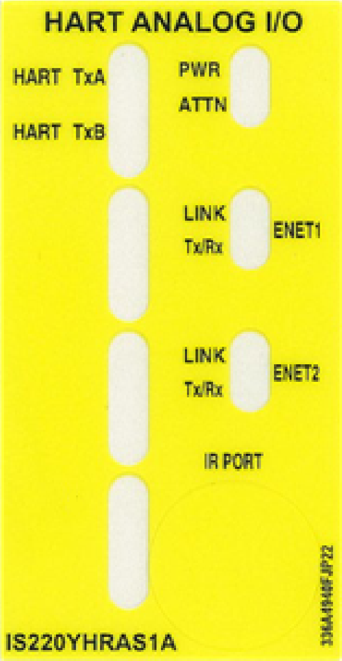
Description Pack internal null voltage out of limits

Possible Cause The calibration null voltage for the analog inputs is more than ±5% from the expected value, which may indicate a hardware failure.

Solution

- Check the I/O pack ground quality through the mounting bolts.
- Cycle power on the I/O pack.
- Replace I/O pack.

10.3 Mark VIeS YHRA HART Analog I/O Pack

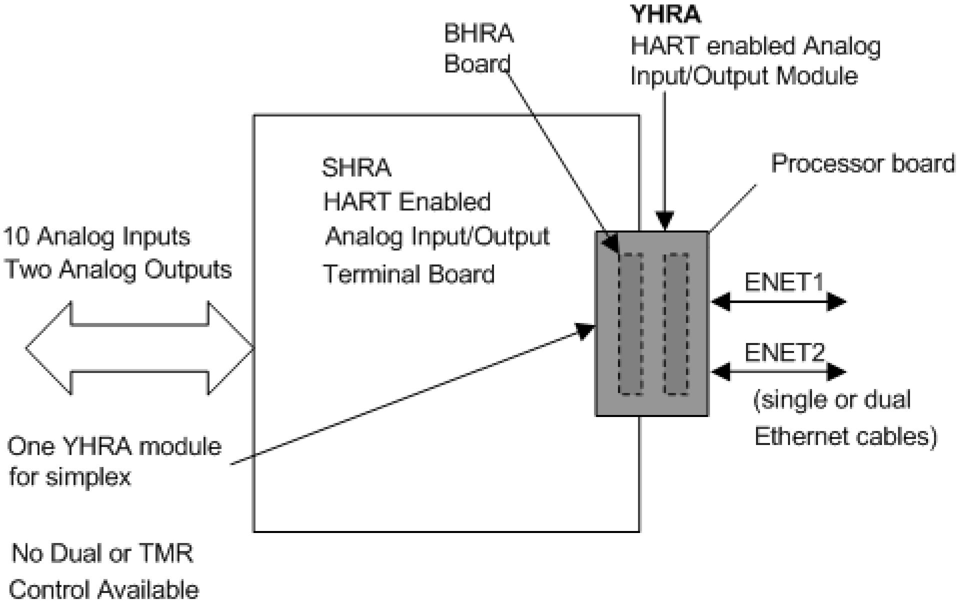


Infrared Port Not Used

The Highway Addressable Remote Transducer (HART) Enabled Analog (YHRA) I/O pack provides the electrical interface between one or two I/O Ethernet networks and an analog input/output terminal board. The YHRA contains a common processor board and an acquisition board specific to the analog input function. The YHRA is capable of handling up to 10 analog inputs, the first eight of which can be configured as ±5 V inputs, or 4-20 mA current loop inputs. The last two inputs can be configured as ±1 mA or 4-20 mA current inputs.

The load termination resistors for current loop inputs are located on the terminal board and voltage is sensed across these resistors by the YHRA. The YHRA also includes support for two 4-20 mA current loop outputs. In addition, in 4-20 mA mode the YHRA can relay HART messages between HART enabled field devices and an Asset Management System (AMS). These HART enabled field devices can be connected through any of the inputs or outputs.

Input to the YHRA is through dual RJ-45 Ethernet connectors and a 3-pin power input. Output is through a DC-62 pin connector that connects directly with the associated terminal board connector. Visual diagnostics are provided through indicator LEDs.



10.3.1 Installation

➢ **To install the YHRA pack**

1. Securely mount the desired terminal board.
2. Directly plug one YHRA I/O pack into the SHRA terminal board DC-62 pin connector.
3. Mechanically secure the pack using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right angle force applied to the DC-62 pin connector between the pack and the terminal board. The adjustment should only be required once in the life of the product.
4. Plug in one or two Ethernet cables depending on the system configuration. The pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
5. Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to insert this connector with the power removed from the cable as the I/O pack has inherent soft-start capability that controls current inrush on power application.
6. Use the ToolboxST application to configure the I/O pack as necessary.

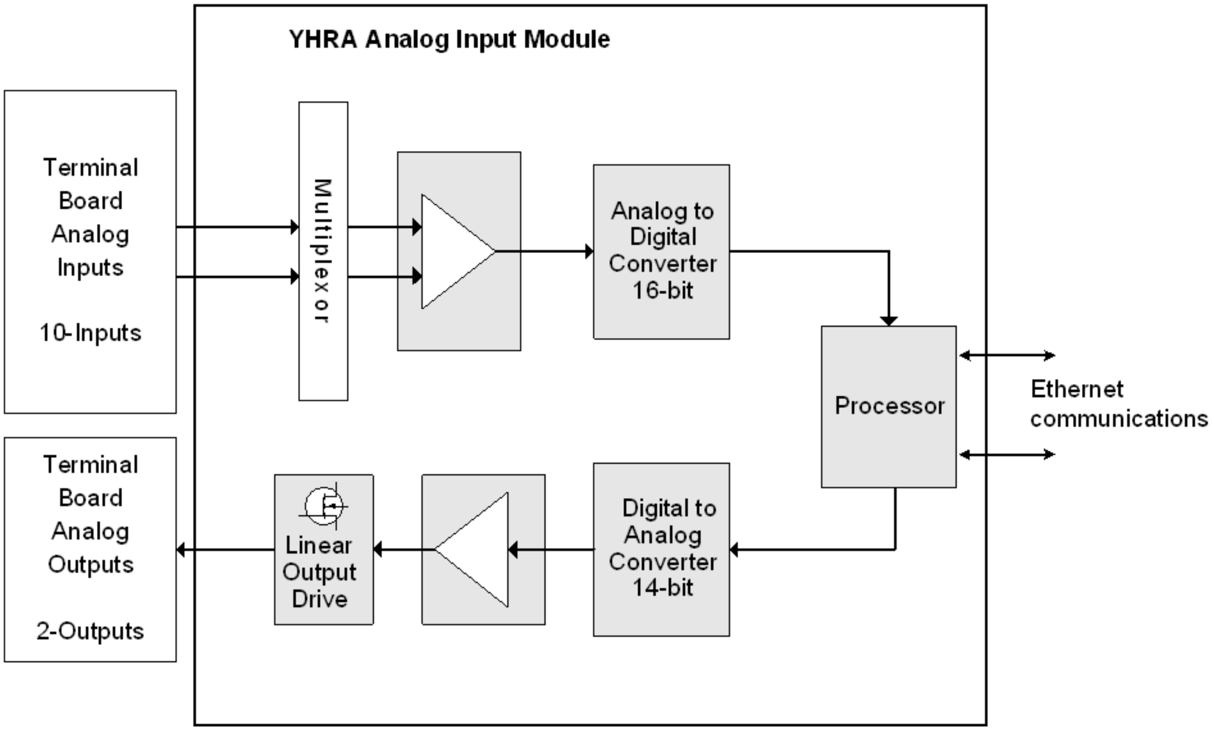
10.3.2 Operation

The following features are common to the safety I/O modules:

- BPPx Processor Board
- Processor LEDs
- I/O Module Common Diagnostic Alarms

10.3.2.1 Analog Input Hardware

The YHRA accepts input voltage signals from the terminal board for all 10 input channels. The analog input section consists of an analog multiplexer block, several gain and scaling selections, and a 16-bit ADC.

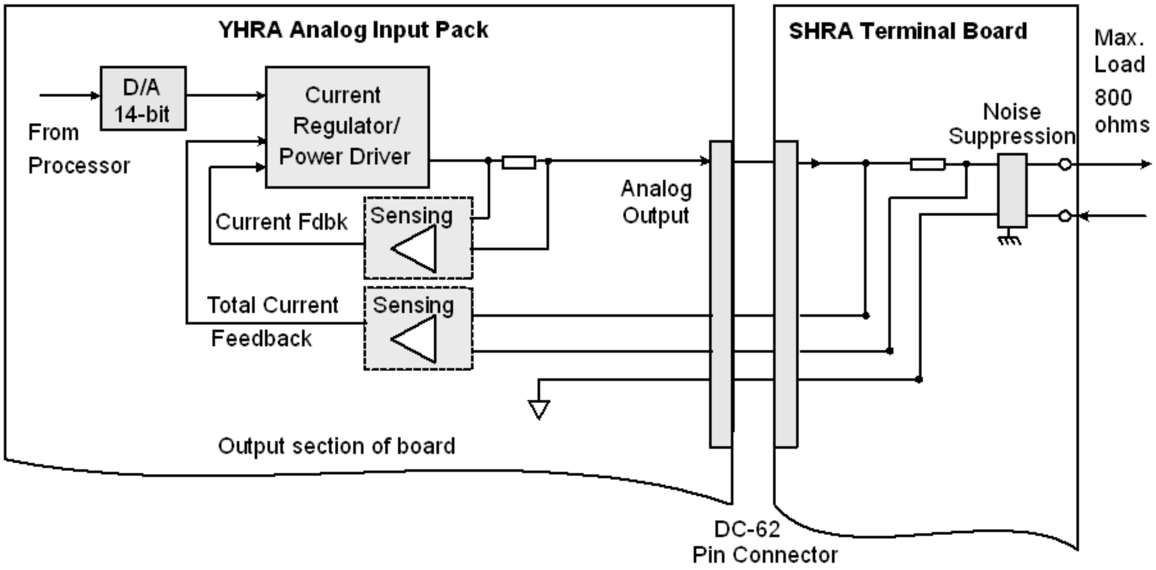

YHRA Analog Input Module
Terminal Board Analog Inputs
10-Inputs
Multiplexor
Analog to Digital Converter 16-bit
Processor
Ethernet communications
Terminal Board Analog Outputs
2-Outputs
Linear Output Drive
Digital to Analog Converter 14-bit

The inputs can be individually configured as ±5 V scale signals, depending on the input configuration. The terminal board provides a 250 Ω burden resistor when configured for current inputs yielding a 5 V signal at 20 mA. These analog input signals are first passed through a second order, passive, low pass filter network with poles at 12.5 Hz and 48.3 Hz. Voltage signal feedbacks from the analog output circuits and calibration voltages are also sensed by the YHRA analog input section.

10.3.2.2 Analog Output

The YHRA includes two 4-20 mA analog outputs capable of 18 V compliance. A 14-bit DAC commands a current reference to the current regulator loop in the YHRA that senses current both in the YHRA pack and on the terminal board. Analog output status feedbacks for each output include:

- Current reference voltage
- Individual current (output current sourced from within the YHRA)
- Total current (as sensed from the terminal board)



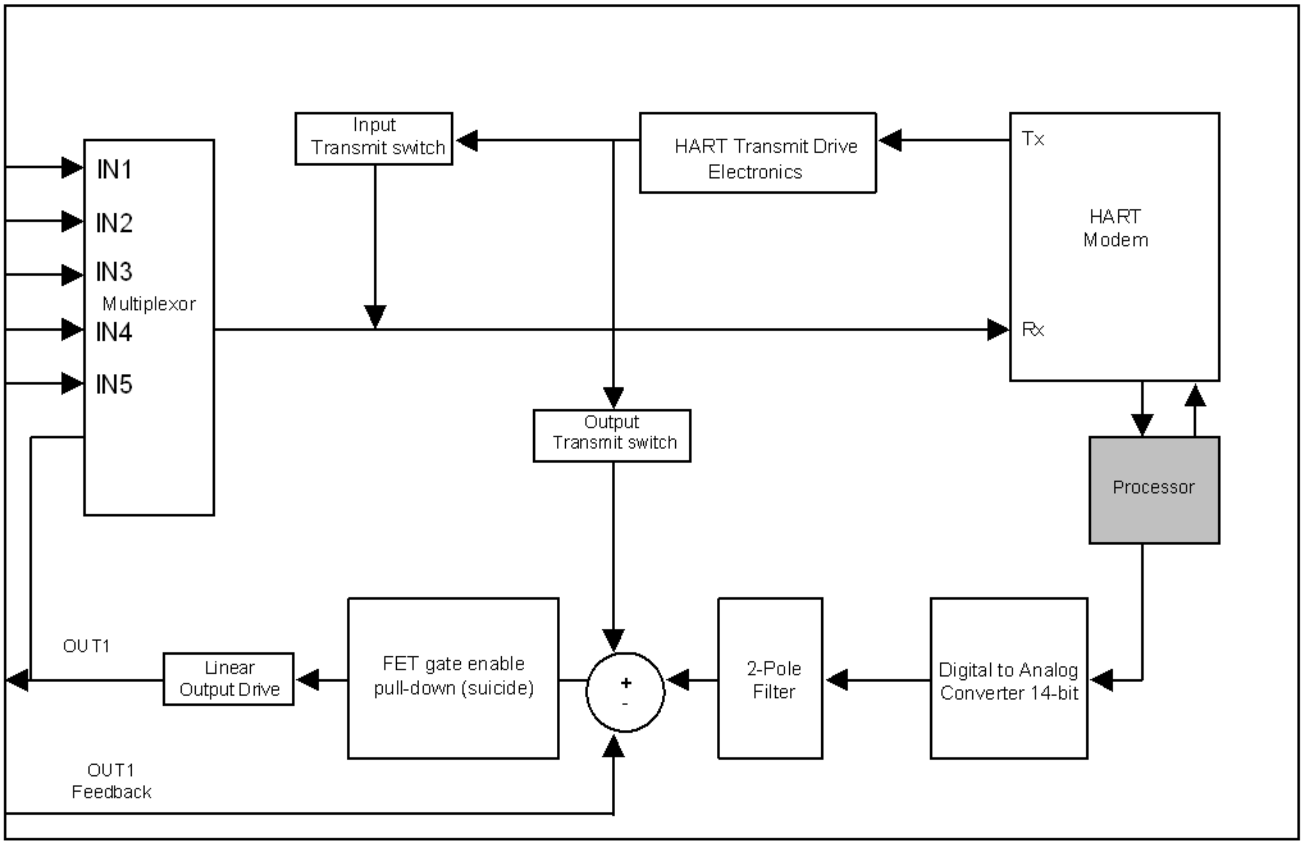
10.3.2.3 HART Hardware

All inputs and outputs on the BHRA are HART enabled. This means there are 12 individual HART channels, with 10 channels for the analog inputs and two channels for the outputs. These 12 channels are served by a pair of HART modems so that each modem is associated with six HART channels. Inputs 1 through 5 and output 1 are multiplexed down to HART modem A. Inputs 6 through 10 and output 2 are multiplexed down to HART modem B.

HART Modem Associations

HART channel	YHRA I/O analog	Served by modem
1	Input #1	A
2	Input #2	A
3	Input #3	A
4	Input #4	A
5	Input #5	A
6	Output #1	A
7	Input #6	B
8	Input #7	B
9	Input #8	B
10	Input #9	B
11	Input #10	B
12	Output #2	B

The number of active channels a modem is serving greatly impacts the HART data update time. If one of the six channels served by a HART modem is active, the modem is dedicated to a single field device and, under normal operating conditions, ToolboxST data associated with this device is updated roughly once per second. If all six channels are in use, roughly eight seconds will pass between updates.



Analog I/O HART Interface — Quantity 2

10.3.3 Specifications

Item	YHRA Specification
Number of Channels	12 channels per terminal board (10 AI, 2 AO)
Input Span	4-20 mA dc, ±5 V dc, (Inputs 1-8) 4-20 mA or ±1 mA (Inputs 9-10)
Input Converter Resolution	16-bit ADC converter
Scan Time	Normal scan 5 ms (200 Hz) *The update rate in the controller is based on the frame rate.*
Measurement Accuracy	Better than 0.1% full scale over the temperature range -30 to 65°C (-22 to 149 °F). Typical accuracy at 25°C (77 °F) is 0.007% full scale.
Noise Suppression on Inputs	The ten circuits have a hardware filter with two poles at 12.5 Hz and 48.3 Hz. A software filter, using a two-pole, low-pass filter, is configurable for: 0, 0.75 Hz, 1.5 Hz, 3 Hz, 6 Hz, 12 Hz
Common Mode Rejection	AC CMR 60 dB 60 Hz, with up to ±5 V common mode voltage. DC CMR 80 dB with from -5 to +7 peak V common mode voltage
Common Mode Voltage Range	±5 V
Output Converter	14-bit D/A converter with 0.5% accuracy
Output Load	800 Ω for 4-20 mA output
Size	8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in x 1.65 in x 4.78 in)
Technology	Surface-mount
Ambient Rating for Enclosure Design†	-30 to 65°C (-22 to 149 °F)

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

10.3.4 Diagnostics

The I/O pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set
- Each analog input has hardware limit checking based on preset (non-configurable) high and low levels near the end of the operating range. If this limit is exceeded a logic signal is set and the input is no longer scanned. The logic signal, L3DIAG_YHRA, refers to the entire board.
- Each input has system limit checking based on configurable high and low levels. These limits can be used to generate alarms, to enable/disable, and as latching/non-latching. RESET_SYS resets the out of limits.
- The analog input hardware includes precision reference voltages in each scan. Measured values are compared against expected values and are used to confirm health of the ADC circuits.
- Analog output current is sensed on the terminal board using a small burden resistor. The pack conditions this signal and compares it to the commanded current to confirm health of the DAC converter circuits.
- The analog output suicide relay is continuously monitored for agreement between commanded state and feedback indication.

Details of the individual diagnostics are available from the ToolboxST application. The diagnostic signals can be individually latched, and then reset with the RSTDIAG signal if they go healthy.

10.3.4.1 Status LEDs

Application LEDs

Color	YHRA Label	Description
Yellow	ENA1	HART data transmit, lit on activity
Yellow	ENA2	HART data receive, lit on activity

Note Refer to the Common Safety Module, *Processor LEDs* section.

10.3.5 Configuration

10.3.5.1 Parameters

Parameter	Description	Choices
System Limits	Enable or disable system limits	Enable, disable
Min_MA_Input	Select minimum current for healthy 4-20 mA input	0 to 21 mA
Max_MA_Input	Select maximum current for healthy 4-20 mA input	0 to 21 mA
AMS_Msg_Priority	AMS messages have priority over controlled messages,	Enable, Disabled
AMS_Msgs_Only	AMS messages only, do not send any control messages. Generates alarm 160 when enabled.	Enable, Disabled
AMS_Mux_Scans_Permitted	Allow AMS scan commands for HART message 1 and 2. HART message 3 is always allowed	Enable, Disable
Min_MA_Hart_Output	Minimum current sent to a HART enabled port. HART COMM will not be possible during offline modes if value is set less than 4 mA	0-22.5

10.3.5.2 Analog Inputs 1–10

Point Parameter	Description	Choices
Input Type	Current or voltage input type	Unused, 4-20 mA, ±5 V
Low_Input	Value of current at the low end of scale	-10 to 20
Low_Value	Value of input in engineering units at low end of scale	-3.4082 e + 038 to 3.4028 e + 038
High_Input	Value of current at the high end of scale	-10 to 20
High_Value	Value of input in engineering units at high end of scale	-3.4082 e + 038 to 3.4028 e + 038
InputFilter	Bandwidth of input signal filter	Unused, 0.75, 1.5 Hz, 3 Hz, 6 Hz, 12 Hz
DiagHighEnab	Enable high input limit	Enable, disable
DiagLowEnab	Enable low input limit	Enable, disable
Hart_Enable	Allow the HART Protocol on this IO point. This must be set to true if HART messages are needed from this field device	Enable, Disable
Hart_CtrlVars	Number of variables to read from the device. Set to zero if not used.	0-5
Hart_ExStatus	Number of extended status bytes to read from the device. Set to zero if not needed for control.	0-26
Hart_MfgID	HART field device's manufacturers code. A diagnostic alarm is sent if the field device ID differs from this value and the value is non-zero. This value can be uploaded from YHRA if the field device is connected. (Right-click on device name and select Upload HART IDs)	0-255

Point Parameter	Description	Choices
Hart_DevType	HART Field Device – Type of device. (See Hart_MfgID)	0-255
Hart_DevID	HART Field Device – Device ID. (See Hart_MfgID)	0-116777215
SysLim1Enabl	Input fault check	Enable, disable
SysLim1Latch	Input fault latch	Latch, unlatch
SysLim1Type	Input fault type	Greater than or equal, Less than or equal
SysLim1	Input limit in engineering units	-3.4082 e + 038 to 3.4028 e + 038
SysLim2Enabl	Input fault check	Enable, disable
SysLim2Latch	Input fault latch	Latch, unlatch
SysLim2Type	Input fault type	Greater than or equal. Less than or equal
SysLim2	Input limit in engineering units	-3.4082 e + 038 to 3.4028 e + 038

10.3.5.3 Analog Outputs 1–2

Point Parameter	Description	Choices
Output_MA	Type of output current, mA selection	Unused, 0-20 mA
Standby_State	State of the outputs when offline	PwrDownMode Hold Last Value Output_Value
Output_Value	Pre-determined value for the outputs, when Standby_State = Output_Value	
Low_MA	Output mA at low value	0 to 20 mA
Low_Value	Output in engineering units at low mA	-3.4082 e + 038 to 3.4028 e + 038
High_MA	Output mA at high value	0 to 20 mA
High_Value	Output value in engineering units at high mA	-3.4082 e + 038 to 3.4028 e + 038
D/A_ErrLimit	Difference between D/A reference and output, in %	0 to 100 %
Hart_Enable	Allow the HART Protocol on this IO point. This must be set to true if HART messages are needed from this field device	Enable, Disable
Hart_CtrlVars	Number of variables to read from the device. Set to zero if not used.	0-5
Hart_ExStatus	Number of extended status bytes to read from the device. Set to zero if not needed for control.	0-26
Hart_MfgID	HART field device's manufacturers code. A diagnostic alarm is sent if the field device ID differs from this value and the value is non-zero. This value can be uploaded from YHRA if the field device is connected. (Right-click on device name and select Upload HART IDs)	0-255
Hart_DevType	HART Field Device – Type of device. (See Hart_MfgID)	0-255
Hart_DevID	HART Field Device – Device ID. (See Hart_MfgID)	0-116777215

10.3.5.4 Variables

Board Points (Signals)	Description - Point Edit (Enter Signal Connection)	Direction	Type
L3DIAG_YHRA	Board diagnostic	Input	BIT
LINK_OK_YHRA	Link diagnostic input	Input	BIT
ATTN_YHRA	Module diagnostic	Input	BIT
IOPackTmpr	I/O pack temperature	Input	FLOAT
PS18V_YHRA_R	I/O 18 V power supply indication	Input	BIT

Board Points (Signals)	Description - Point Edit (Enter Signal Connection)	Direction	Type
PS28V_YHRA_R	I/O 28 V power supply indication	Input	BIT
MuxHealth1	Health bit for YHRA HART multiplexer	Input	BIT
SysLimit1_1	System Limit 1	Input	BIT
:	:	Input	BIT
SysLimit1_10	System Limit 1	Input	BIT
SysLimit2_1	System Limit 2	Input	BIT
:	:	Input	BIT
SysLimit2_10	System Limit 2	Input	BIT
Out1MA	Feedback, Total output current, mA	Input	FLOAT
Out2MA	Feedback, Total output current, mA	Input	FLOAT

10.3.5.5 HART Signal Definitions

Each HART field device has a set of HART signals that are read from the field device. These signals are prefixed with either HIx_ or HOx_ where x is 1-10 for input channels and 1-2 for output channels.

Signal	Type	Description
Hxx_CommCnt	Integer	Number of times the CommStat signal was not zero after a HART message
Hxx_CommStat	Bit encoded integer	HART Communication status Bit 1 – RX buffer overflow Bit 3 – Checksum error Bit 4 – Framing error Bit 5 – Overrun error Bit 6 – Parity error
Hxx_DevCnt	Integer	Number of times the DevStat signal was not zero after a HART message.
Hxx_DevStat	Bit encoded integer	Field Device Status: bits 0-7 Bit 0 – Primary variable out of limits Bit 1 – Non primary variable out of limits Bit 2 – Analog output saturated Bit 3 – Analog output current fixed Bit 4 – More status available (ExStat) Bit 5 – Cold start Bit 6 – Configuration changed Bit 7 – Field device malfunction Command response byte: bits 8-15 2: Invalid selection requested 3: Passed parameter too large 4: Passed parameter too small 5: Too few bytes received 6: Device specific device error 7: In write protect mode 8-15: Device specific 16: Access restricted 32: Device is busy 64: Command not implemented
Hxx_DevRev	Integer	Field Device - Device revision code as read from the device.
Hxx_HwSwRev	Integer	Byte 0 - Field device software revision Byte 1 - Field device hardware revision
Hxx_mA	Float	Field Parm 1 – current reading of the primary signal

Signal	Type	Description
Hxx_PV †	Float	Field Device Specific Control Parm 2 - Primary field device value
Hxx_SV †	Float	Field Device Specific Control Parm 3 - Secondary value
Hxx_TV †	Float	Field Device Specific Control Parm 4 -Third value
Hxx_FV †	Float	Field Device Specific Control Parm 5 -Fourth value
† To view these variables, the HART_CtrlVars parameter must have a value greater than zero.		
Hxx_ExStat_1	Bit Encoded	Extended Status Bytes 1-4
Hxx_ExStat_2	Bit Encoded	Extended Status Bytes 5-8
Hxx_ExStat_3	Bit Encoded	Extended Status Bytes 9-12
Hxx_ExStat_4	Bit Encoded	Extended Status Bytes 13-16
Hxx_ExStat_5	Bit Encoded	Extended Status Bytes 17-20
Hxx_ExStat_6	Bit Encoded	Extended Status Bytes 21-24
Hxx_ExStat_7	Bit Encoded	Extended Status Bytes 25-26

The extended status bits are device-specific, and can be interrogated by using an AMS system. In general, the status bits are grouped as follows:

- Bytes 0-5: Device specific status
- Bytes 6-7: Operational modes
- Bytes 8-10: Analog output saturation
- Bytes 11-13: Analog output current fixed
- Bytes 14-26: Device-specific

Each field device supports a specific number of control parameters and extended status bits. Refer to the *Field Device* documentation to determine the correct number and configure it with the ToolboxST application accordingly. A diagnostic alarm message will be generated if the Field Device and ToolboxST configuration do not match.

10.4 YHRA Specific Alarms

32-41

Description Analog Input [ ] unhealthy

Possible Cause

- Excitation to the transducer is wrong or missing.
- The transducer may be faulty.
- The analog input current/voltage input is beyond the specified range.
- The terminal board jumper settings do not match the ToolboxST configuration.
- There may be an open or short-circuit on the input.

Solution

- Check the field wiring and connections to the indicated analog input channel.
- Check the field device for failure.
- Verify that the configuration matches the terminal board jumper settings for the indicated analog input channel.

46-47

Description Analog Output [ ] total unhealthy

Possible Cause

- The commanded output is beyond the range of the output.
- There may be a field wiring problem.
- There may be a field device problem.
- There may be an open loop or too much resistance in the loop.

Solution

- Verify that the commanded output is within the range of the output.
- Confirm that the I/O pack 28 V input power is correct.
- Check the field wiring and the device.
- Replace the I/O pack.

48-49

Description Analog output [ ] reference unhealthy

Possible Cause There may be an I/O pack failure.

Solution

- Confirm that the I/O pack 28 V input power is correct.
- Replace the I/O pack.

66-67

Description Output [ ] Individual current too high relative to total current

Possible Cause

- A disagreement has been detected between the output current sensing inside the I/O pack and the current sensing on SHRA.
- A hardware failure is causing the I/O pack to drive too much output current.

Solution

- Check the I/O pack mounting on the SHRA.
- Confirm that the field wiring and load are correct.
- Check the output configuration.
- Replace the SHRA and the I/O pack.

70-71

Description Output [ ] Total current varies from reference current

Possible Cause

- There may be a field wiring problem.
- There may be an open-circuit on the output, or the total loop resistance is too high.
- The command is beyond the range of the output.

Solution

- Check the field wiring and the device.
- Check the output configuration.
- Verify that the commanded output is within output range.
- Check the I/O pack mounting on the SHRA.
- Replace the I/O pack.

74–75

Description Output [ ] Reference current error

Possible Cause

- The difference between the commanded output current and current feedback on the terminal board is greater than the *D/A_ErrLimit* parameter (%).
- There may be an open-circuit on the output.
- The command is beyond the range of the output.

Solution

- Check the field wiring and the device.
- Verify that the value of the *D/A_ErrLimit* parameter is set correctly.
- Verify that the commanded output is within the output range.
- Replace the I/O pack.

78–79

Description Output [ ] individual current unhealthy

Possible Cause

- The commanded output is beyond the range of the output.
- There may be a field wiring problem.
- There may be a field device problem.
- There is an open loop or too much resistance in the loop.
- There may be an I/O pack failure.
- There may be a terminal board failure.

Solution

- Verify that the commanded output is within the range of the output.
- Confirm the correct I/O pack 28 V input power.
- Check the field wiring and the device.
- Replace the I/O pack.

99

Description HART Input 1 Channel 1 not initialized

Possible Cause An enabled HART input channel does not respond.

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

100

Description HART Input 2 Channel 2 not initialized

Possible Cause An enabled HART input channel does not respond.

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

101

Description HART Input 3 Channel 3 not initialized

Possible Cause An enabled HART input channel does not respond.

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

102

Description HART Input 4 Channel 4 not initialized

Possible Cause An enabled HART input channel does not respond.

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

103

Description HART Input 5 Channel 5 not initialized

Cause An enabled HART input channel does not respond.

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

104

Description HART Output 1 Channel 6 not initialized

Possible Cause An enabled HART output channel does not respond.

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

105

Description HART Input 6 Channel 7 not initialized

Possible Cause An enabled HART input channel does not respond.

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

106

Description HART Input 7 Channel 8 not initialized

Possible Cause An enabled HART input channel does not respond.

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

107

Description HART Input 8 Channel 9 not initializedd

Possible Cause An enabled HART input channel does not respond.

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

108

Description HART Input 9 Channel 10 not initialized

Possible Cause An enabled HART input channel does not respond.

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

109

Description HART Input 10 Channel 11 not initializedd

Possible Cause An enabled HART input channel does not respond.

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

110

Description HART Output 2 Channel 12 not initialized

Possible Cause An enabled HART input channel does not respond.

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

111

Description HART Input 1 Channel 1 address mismatch

Possible Cause The device ID in the ToolboxST configuration does not match the field device.

Solution

- Verify that the field device is attached to the correct I/O point.
- If so, either set the three ID fields to zero, or upload the device ID from the field device.

112

Description HART Input 2 Channel 2 address mismatch

Possible Cause The device ID in the ToolboxST configuration does not match the field device.

Solution

- Verify that the correct field device is connected to the I/O point.
- If so, either set the three ID fields to zero, or upload the device ID from the field device.

113

Description HART Input 3 Channel 3 address mismatch

Possible Cause The device ID in the ToolboxST configuration does not match the field device.

Solution

- Verify that the correct field device is connected to the I/O point.
- If so, either set the three ID fields to zero, or upload the device ID from the field device.

114

Description HART Input 4 Channel 4 address mismatch

Possible Cause The device ID in the ToolboxST configuration does not match the field device.

Solution

- Verify that the correct field device is connected to the I/O point.
- If so, either set the three ID fields to zero, or upload the device ID from the field device.

115

Description HART Input 5 Channel 5 address mismatch

Possible Cause The device ID in the ToolboxST configuration does not match the field device.

Solution

- Verify that the correct field device is connected to the I/O point.
- If so, either set the three ID fields to zero, or upload the device ID from the field device.

116

Description HART Output 1 Channel 6 address mismatch

Possible Cause The device ID in the ToolboxST configuration does not match the field device.

Solution

- Verify that the correct field device is connected to the I/O point.
- If so, either set the three ID fields to zero, or upload the device ID from the field device.

117

Description HART Input 6 Channel 7 address mismatch

Possible Cause The device ID in the ToolboxST configuration does not match the field device.

Solution

- Verify that the correct field device is connected to the I/O point.
- If so, either set the three ID fields to zero, or upload the device ID from the field device.

118

Description HART Input 7 Channel 8 address mismatch

Possible Cause The device ID in the ToolboxST configuration does not match the field device.

Solution

- Verify that the correct field device is connected to the I/O point.
- If so, either set the three ID fields to zero, or upload the device ID from the field device.

119

Description HART Input 8 Channel 9 address mismatch

Possible Cause The device ID in the ToolboxST configuration does not match the field device.

Solution

- Verify that the correct field device is connected to the I/O point.
- If so, either set the three ID fields to zero, or upload the device ID from the field device.

120

Description HART Input 9 Channel 10 address mismatch

Possible Cause The device ID in the ToolboxST configuration does not match the field device.

Solution

- Verify that the correct field device is connected to the I/O point.
- If so, either set the three ID fields to zero, or upload the device ID from the field device.

121

Description HART Input 10 Channel 11 address mismatch

Possible Cause The device ID in the ToolboxST configuration does not match the field device.

Solution

- Verify that the correct field device is connected to the I/O point.
- If so, either set the three ID fields to zero, or upload the device ID from the field device.

122

Description HART Output 2 Channel 12 address mismatch

Possible Cause The device ID in the ToolboxST configuration does not match the field device.

Solution

- Verify that the correct field device is connected to the I/O point.
- If so, either set the three ID fields to zero, or upload the device ID from the field device.

123

Description YHRA HART Module Modified

Possible Cause The configuration of the HART multiplexer on the YHRA was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ To unlatch this diagnostic

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

124

Description HART Input 1 Channel 1 Field Device Modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ To unlatch this diagnostic

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

125

Description HART Input 2 Channel 2 Field Device Modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ To unlatch this diagnostic

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

126

Description HART Input 3 Channel 3 Field Device Modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ To unlatch this diagnostic

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

127

Description HART Input 4 Channel 4 Field Device Modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ To unlatch this diagnostic

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

128

Description HART Input 5 Channel 5 Field Device Modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ To unlatch this diagnostic

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

129

Description HART Output 1 Channel 6 Field Device Modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ To unlatch this diagnostic

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

130

Description HART Input 6 Channel 7 Field Device Modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ To unlatch this diagnostic

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

131

Description HART Input 7 Channel 8 Field Device Modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ To unlatch this diagnostic

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

132

Description HART Input 8 Channel 9 Field Device Modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ To unlatch this diagnostic

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

133

Description HART Input 9 Channel 10 Field Device Modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ To unlatch this diagnostic

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

134

Description HART Input 10 Channel 11 Field Device Modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ **To unlatch this diagnostic**

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

135

Description HART Output 2 Channel 12 Field Device Modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what change was made and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault.

➢ **To unlatch this diagnostic**

1. From the ToolboxST application, Component Editor, **Software** tab, navigate to the **SYS_OUTPUTS** block (this block is part of the Standard or SIL block library depending on controller type).
2. Set the RSTDIAG input BOOL to TRUE.
3. Wait for the I/O pack diagnostics to become inactive, and then set the RSTDIAG to FALSE.
4. From the **Diagnostics** tab, click **Reset Alarms** (as usual) to clear the alarm.

136

Description HART Input 1 Chan 1 Control Parm Mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in HART Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

137

Description HART Input 2 Chan 2 Control Parm Mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in HART Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

138

Description HART Input 3 Chan 3 Control Parm Mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in HART Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

139

Description HART Input 4 Chan 4 Control Parm Mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in HART Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

140

Description HART Input 5 Chan 5 Control Parm Mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in HART Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

141

Description HART Output 1 Chan 6 Control Parm Mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in HART Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

142

Description HART Input 6 Chan 7 Control Parm Mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in HART Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

143

Description HART Input 7 Chan 8 Control Parm Mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in HART Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

144

Description HART Input 8 Chan 9 Control Parm Mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in HART Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

145

Description HART Input 9 Chan 10 Control Parm Mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in HART Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

146

Description HART Input 10 Chan 11 Control Parm Mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in HART Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

147

Description HART Output 2 Chan 12 Control Parm Mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in HART Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

148

Description HART Input 1 Chan 1 Extended Status Mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in HART Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

149

Description HART Input 2 Chan 2 Extended Status Mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in HART Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

150

Description HART Input 3 Chan 3 Extended Status Mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in HART Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

151

Description HART Input 4 Chan 4 Extended Status Mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in HART Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

152

Description HART Input 5 Chan 5 Extended Status Mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in HART Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

153

Description HART Output 1 Chan 6 Extended Status Mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in HART Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

154

Description HART Input 6 Chan 7 Extended Status Mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in HART Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

155

Description HART Input 7 Chan 8 Extended Status Mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in HART Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

156

Description HART Input 8 Chan 9 Extended Status Mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in HART Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

157

Description HART Input 9 Chan 10 Extended Status Mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in HART Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

158

Description HART Input 10 Chan 11 Extended Status Mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in HART Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

159

Description HART Output 2 Chan 12 Extended Status Mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in HART Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

160

Description HART Control Messages disabled. AMS HART messages only

Possible Cause **The AMS_Msgs_Only** parameter is **Enabled**. No control messages are sent. This parameter overrides the values in the **HART_CtrlVars**and **HART_ExStatus** strong for each individual channel.

Solution

- To send AMS messages only, but clear this alarm: Set the **AMS_Msgs_Only** parameter to **Disabled** and set each channel's **HART_CtrlVars** and **HART_ExStatus** to zero.
- To allow control messages and AMS messages, set **AMS_Msgs_Only** to **Disabled**.

161

Description HART Input 1 Chan 1 - Field device not write protected in locked mode

Possible Cause The field device for this channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

162

Description HART Input 2 Chan 2 - Field device not write protected in locked mode

Possible Cause The field device for this channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

163

Description HART Input 3 Chan 3 - Field device not write protected in locked mode

Possible Cause The field device for this channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

164

Description HART Input 4 Chan 4 - Field device not write protected in locked mode

Possible Cause The field device for this channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

165

Description HART Input 5 Chan 5 - Field device not write protected in locked mode

Possible Cause The field device for this channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

166

Description HART Output 1 Chan 6 - Field device not write protected in locked mode

Possible Cause The field device for this channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

167

Description HART Input 6 Chan 7 - Field device not write protected in locked mode

Possible Cause The field device for this channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

168

Description HART Input 7 Chan 8 - Field device not write protected in locked mode

Possible Cause The field device for this channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

169

Description HART Input 8 Chan 9 - Field device not write protected in locked mode

Possible Cause The field device for this channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

170

Description HART Input 9 Chan 10 - Field device not write protected in locked mode

Possible Cause The field device for this channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

171

Description HART Input 10 Chan 11 - Field device not write protected in locked mode

Possible Cause The field device for this channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

172

Description HART Output 2 Chan 12 - Field device not write protected in locked mode

Possible Cause The field device for this channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

173

Description Pack internal reference voltage out of limitse

Possible Cause The calibration reference voltage for the analog inputs is more than ±5% from the expected value, which may indicate a hardware failure.

Solution

- Check the I/O pack ground quality through the mounting bolts.
- Cycle power on the I/O pack.
- Replace the I/O pack.

174

Description Null voltage out of limits

Possible Cause The calibration null voltage for the analog inputs is more than ±5% from the expected value, which may indicate a hardware failure.

Solution

- Check the I/O pack ground quality through the mounting bolts.
- Cycle power on the I/O pack.
- Replace I/O pack.

10.5 SHRAH#A, S#A Simplex HART Analog Input/Output

The Simplex HART Enabled Analog Input/Output (SHRA) terminal board is a compact analog input terminal board that accepts 10 analog inputs and two analog outputs. It allows HART messages to pass between the I/O pack and a HART enabled field device. The 10 analog inputs accommodate two-wire, three-wire, four-wire, or externally powered transmitters. The two analog outputs are 4-20 mA.

Only a simplex version of the board is available. High-density, Euro-block type terminal blocks are used. An on-board ID chip identifies the board to the I/O pack for system diagnostic purposes.

Compatibility

Board Revision	Mark VIe Control IS220PHRA	Mark VIeS Safety Control IS200YHRA	Comments
SHRAH1A	Yes, all versions	No	Fixed terminals
SHRAH2A	Yes, all versions	No	Pluggable terminals
SHRAS1A	Yes, all versions	Yes, all versions	Fixed terminals, IEC 61508 safety certified with Mark VIeS YHRA
SHRAS2A	Yes, all versions	Yes, all versions	Removable terminals, IEC 61508 safety certified with Mark VIeS YHRA

10.5.1 Installation

The I/O pack plugs into the D-type connector JA1 and communicates with the controller over Ethernet. The SHRA plus a plastic insulator mounts on a sheet metal carrier that then mounts on a DIN-rail. Optionally, the SHRA plus insulator mounts on a sheet metal assembly and then bolts directly to a cabinet. There are two types of Euro-block terminal blocks available as follows:

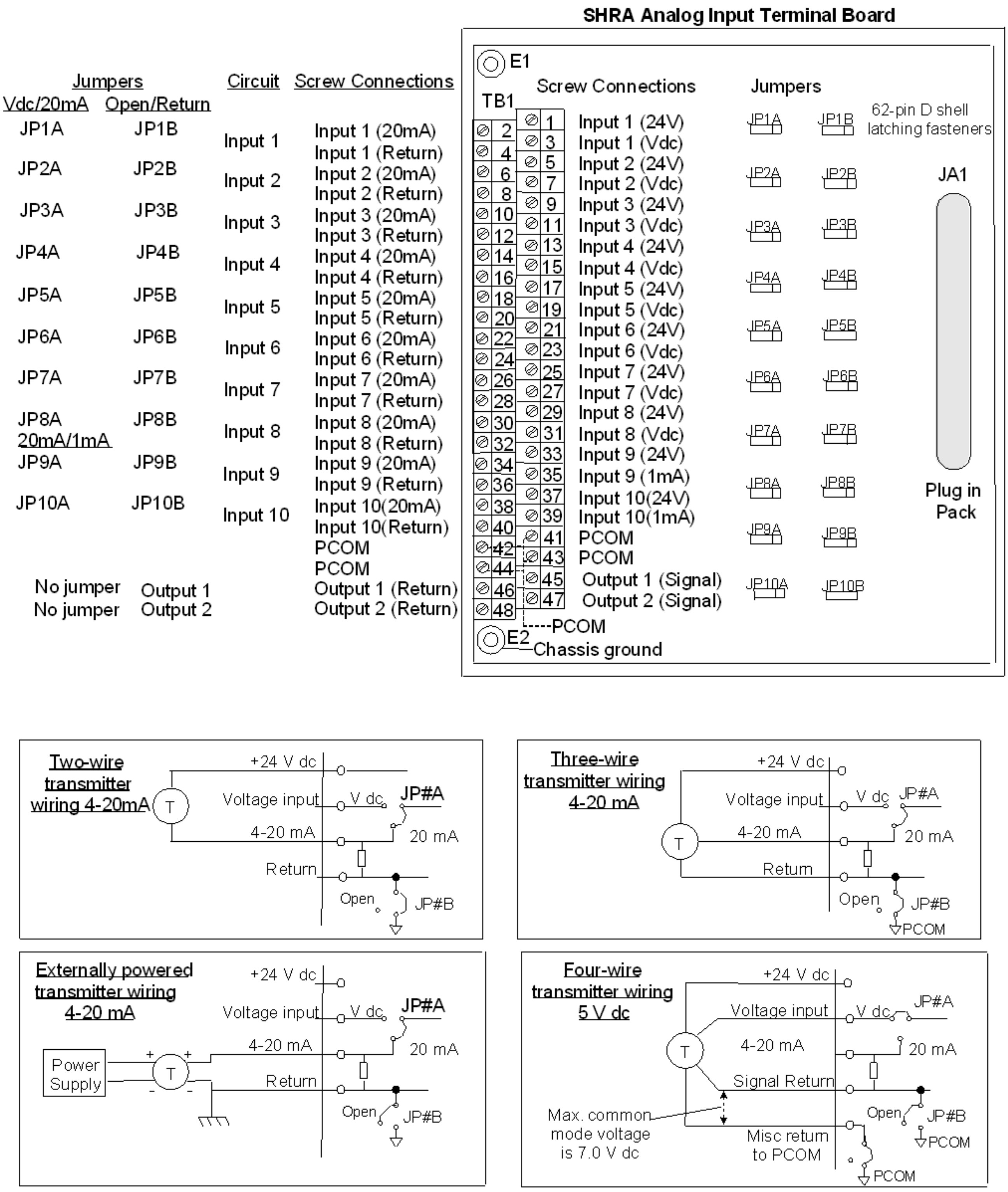
- SHRA_1A has a permanently mounted terminal block with 48 terminals.
- SHRA_2A has a right angle header, accepting a range of commercially available removable terminal blocks with 48 terminals.

Typically #18 AWG wires (shielded twisted-pair) are used. I/O cable shield termination is provided adjacent to the terminal blocks.

The following types of analog inputs/outputs can be used:

- Analog input, two-wire transmitter
- Analog input, three-wire transmitter
- Analog input, four-wire transmitter
- Analog input, externally powered transmitter
- Analog input, voltage ±5 V dc
- Analog output, 4-20 mA current

Wiring, jumper positions, and cable connections display in the following figure.


SHRA Analog Input Terminal Board
Jumpers
Vdc/20mA
Open/Return
Circuit
Screw Connections
JP1A JP1B Input 1 Input 1 (20mA) Input 1 (Return)
JP2A JP2B Input 2 Input 2 (20mA) Input 2 (Return)
JP3A JP3B Input 3 Input 3 (20mA) Input 3 (Return)
JP4A JP4B Input 4 Input 4 (20mA) Input 4 (Return)
JP5A JP5B Input 5 Input 5 (20mA) Input 5 (Return)
JP6A JP6B Input 6 Input 6 (20mA) Input 6 (Return)
JP7A JP7B Input 7 Input 7 (20mA) Input 7 (Return)
JP8A JP8B Input 8 Input 8 (20mA) Input 8 (Return)
20mA/1mA
JP9A JP9B Input 9 Input 9 (20mA) Input 9 (Return)
JP10A JP10B Input 10 Input 10(20mA) Input 10(Return)
PCOM
PCOM
No jumper Output 1 Output 1 (Return)
No jumper Output 2 Output 2 (Return)
E1
TB1
Screw Connections
Jumpers
62-pin D shell latching fasteners
2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40 42 44 46 48
1 Input 1 (24V)
3 Input 1 (Vdc)
5 Input 2 (24V)
7 Input 2 (Vdc)
9 Input 3 (24V)
11 Input 3 (Vdc)
13 Input 4 (24V)
15 Input 4 (Vdc)
17 Input 5 (24V)
19 Input 5 (Vdc)
21 Input 6 (24V)
23 Input 6 (Vdc)
25 Input 7 (24V)
27 Input 7 (Vdc)
29 Input 8 (24V)
31 Input 8 (Vdc)
33 Input 9 (24V)
35 Input 9 (1mA)
37 Input 10(24V)
39 Input 10(1mA)
41 PCOM
43 PCOM
45 Output 1 (Signal)
47 Output 2 (Signal)
JP1A JP1B JP2A JP2B JP3A JP3B JP4A JP4B JP5A JP5B JP6A JP6B JP7A JP7B JP8A JP8B JP9A JP9B JP10A JP10B
JA1
Plug in Pack
PCOM
E2
Chassis ground
Two-wire transmitter wiring 4-20mA
T
+24 V dc
Voltage input
V dc
JP#A
4-20 mA
20 mA
Return
Open
JP#B
Three-wire transmitter wiring 4-20 mA
T
+24 V dc
Voltage input
V dc
JP#A
4-20 mA
20 mA
Return
Open
JP#B
PCOM
Externally powered transmitter wiring 4-20 mA
Power Supply
+ +
T
- -
+24 V dc
Voltage input
V dc
JP#A
4-20 mA
20 mA
Return
Open
JP#B
Four-wire transmitter wiring 5 V dc
T
+24 V dc
Voltage input
V dc
JP#A
4-20 mA
20 mA
Signal Return
Open
JP#B
PCOM
Max. common mode voltage is 7.0 V dc
Misc return to PCOM
PCOM

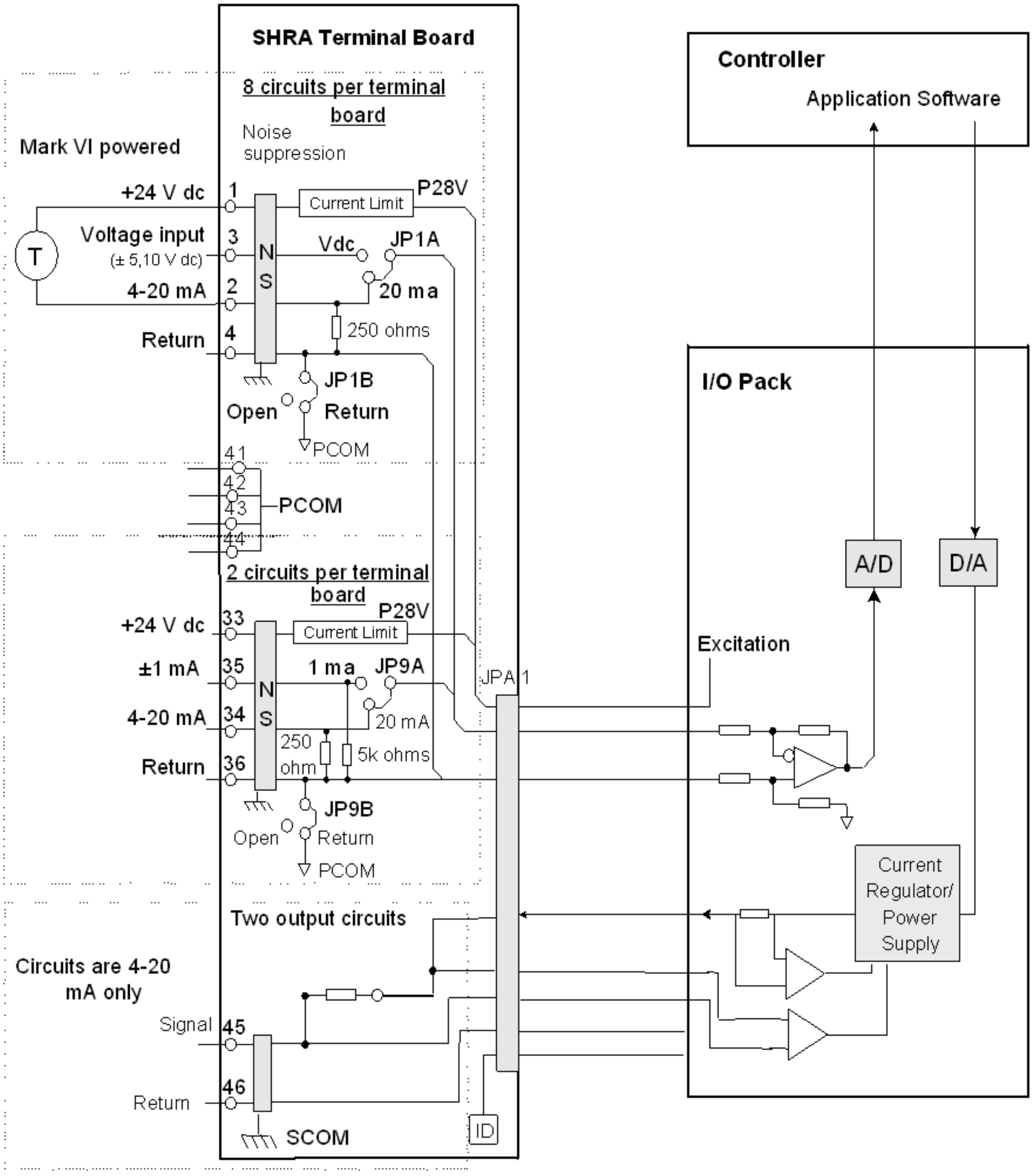
SHRA Wiring, Cabling, and Jumper Positions

10.5.2 Operation

On the terminal board, 24 V dc power is available on the terminal board for all the transmitters (transducers). There is a choice of current or voltage inputs using jumpers. HART communication is only possible with the inputs set as 4-20 mA inputs, it will not take place on an input set as ±5 V dc or ±1 mA. The two analog output circuits are 4-20 mA. There is only one cable connection, so the terminal board cannot be used for TMR applications.

Analog I/O Capacity of SHRA

Quantity	Analog Input Types	Quantity	Analog Output Types
8	±5 V dc, or 4-20 mA	2	4-20 mA
2	4-20 mA, or ±1 mA		



SHRA Terminal Board, and PHRA / YHRA I/O Packs

10.5.3 Specifications

Item	SHRA Specification
Number of Channels	12 channels (10 AI, 2 AO)
Input Span, Transmitters	1 - 5 V dc across a precision resistor (usually 250 Ω)
Max Lead Resistance to Transmitters	15 Ω maximum two-way cable resistance, cable length up to 300 m (984 ft), 24 V outputs provide 21 mA for each connection
Outputs	24 V dc outputs rated at 21 mA each
Load on Output Currents	800 Ω burden for 4-20 mA output with PHRA or YHRA pack
Size	15.9 cm high x 17.8 cm wide (6.25 in x 7.0 in)
Technology	Surface-mount

10.5.4 Diagnostics

Diagnostic tests are made on the terminal board as follows:

- The board provides the voltage drop across a series resistor to indicate the output current. The I/O pack creates a diagnostic alarm (fault) if any one of the two outputs goes unhealthy.
- Each cable connector on the terminal board has its own ID device that is interrogated by the I/O pack. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the JR, JS, JT connector location. When this chip is read by the I/O pack and a mismatch is encountered, a hardware incompatibility fault is created.

10.5.5 Configuration

Configuration of the terminal board is by means of jumpers. For location of these jumpers refer to the *installation* diagram. The jumper choices are as follows:

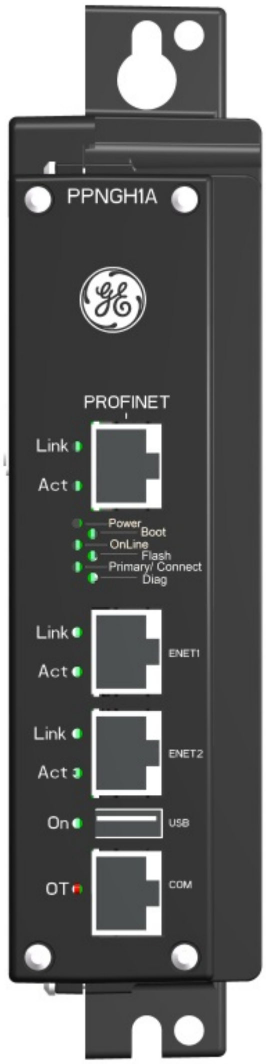
- Jumpers JP1A through JP8A select either current input or voltage input
- Jumpers JP1B through JP8B select whether the return is connected to common or is left open
- Jumpers JP9A and JP10A select either 1 mA or 20 mA input current
- Jumpers JP9B and JP10B select whether the return is connected to common or is left open

11 PPNG PROFINET® Gateway Module

11.1 Mark VIe PROFINET Gateway (PPNG) Module

Attention

The information provided section does not apply to the Embedded PROFINET Gateway (Embedded PPNG) module. For information on the Embedded PPNG module, refer to the chapter *Controllers and Unmanaged Switches*, the section *UCSC Embedded PROFINET Gateway (Embedded PPNG) Module*.



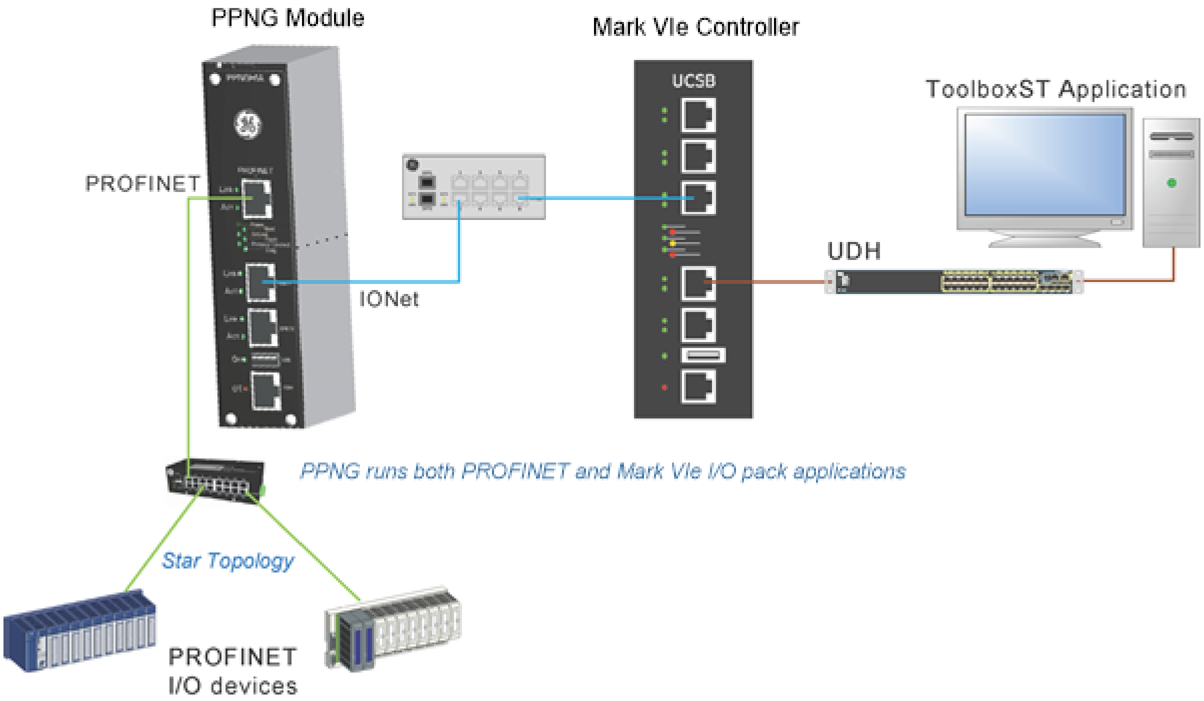
The PROFINET® Gateway (PPNG) module maps I/O from PROFINET Slave devices to the Mark* VIe controller on the IONet. The IS420PPNGH1A connects the Mark VIe controller to a high-speed PROFINET local area network (LAN), enabling communication with PROFINET I/O devices. The PPNG provides functions, services, and protocols required for certification as a PROFINET RT Version 2.2 I/O controller, running 100 Mbps Ethernet interfaces. Functioning as an I/O pack, PPNG with the ToolboxST* application provides the ability to add PROFINET I/O devices and smart sensors into a typical Mark VIe control system architecture.

PPNG features are as follows:

- One RJ-45 shielded twisted pair 10/100 Mbps port for PROFINET communication
- Two RJ-45 shielded twisted pair 10/100 Mbps ports (ENET1, ENET2) for IONet communication
- Single module
- Built-in power supply
- No jumper settings required
- No battery or fan
- Flash memory can be conveniently updated
- Status LEDs for Ethernet, power, and processor
- Internal clock synchronized with the Mark VIe controller for time-stamped diagnostics entries
- Uses the same ControlST* configuration tools across Mark controls platforms
- Multiple PPNGs can be supported for each Mark VIe controller
- PPNG supports star (connect to switch), line (connect direct to I/O device), or mixed network topologies on the PROFINET network.
- Configuration of PROFINET I/O devices
- Cyclic exchange of input and output data from PROFINET I/O devices, asynchronous with Mark VIe controller frame
- Displays values of inputs and outputs through ToolboxST application
- Displays diagnostic messages from devices to resolve issues

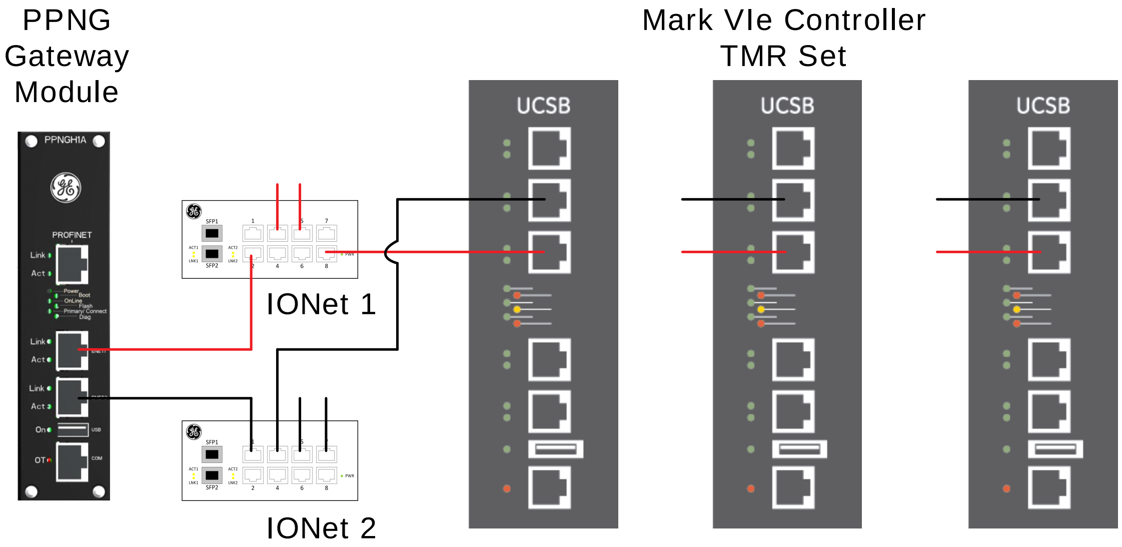
The ToolboxST application is used to configure the PROFINET I/O devices. Any change in these devices requires a new configuration to be downloaded to the PPNG, then the module restarts. A local variable can be connected to a particular I/O point from the PROFINET I/O device and used in the Mark VIe controller application logic.

The following figures display typical PPNG module topologies.



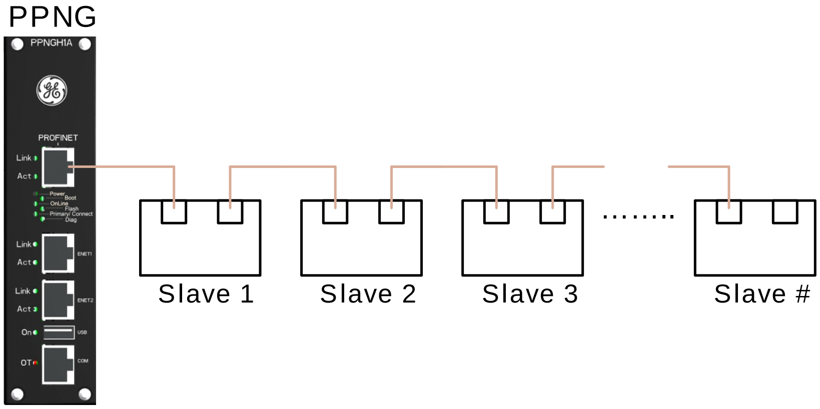
Star Topology

Dual IONets with Dual or TMR controllers are supported.



Dual IONets

Line PROFINET topology is supported, with the restrictions that the PPNG has to be at one end of the bus and other performance limitations.



Line Topology

PPNG can also support a mix of line and star topologies. In a mixed layout, the PPNG does not need to reside at the end of the bus. For example, in the above figure, a switch could be placed between Slaves 2 and 3, and the PPNG could be connected to the switch.

11.1.1 Compatibility

- PPNG functionality is supported in ControlST V05.04 and later.
- Online downloads to the PPNG are supported with ControlST V06.00 or later.
- PPNG supports *IONet network redundancy*; however, the PPNG module itself is Simplex.
- The PPNG does not support system redundancy or media redundancy on the PROFINET network.

11.1.1.1 Default Scanners

The PPNG requires PROFINET communication to modular (slice) I/O modules through an I/O device scanner (also commonly known as a bus coupler or head module, depending on the manufacturer). The following GEIP PROFINET scanner configurations are available by default from the ToolboxST application:

GEIP PROFINET Slave Device	User Manual
RX3i CEP PROFINET Scanner	GFK-2736
RX3i PROFINET Scanner	GFK-2737
PAC8000 PROFINET Scanner	GFK-2839
RSTi PROFINET Network Adapter	GFK-2745
VersaMax PROFINET Scanner	GFK-2721
VersaPoint PROFINET Scanner	GFK-2883

11.1.1.2 I/O Devices

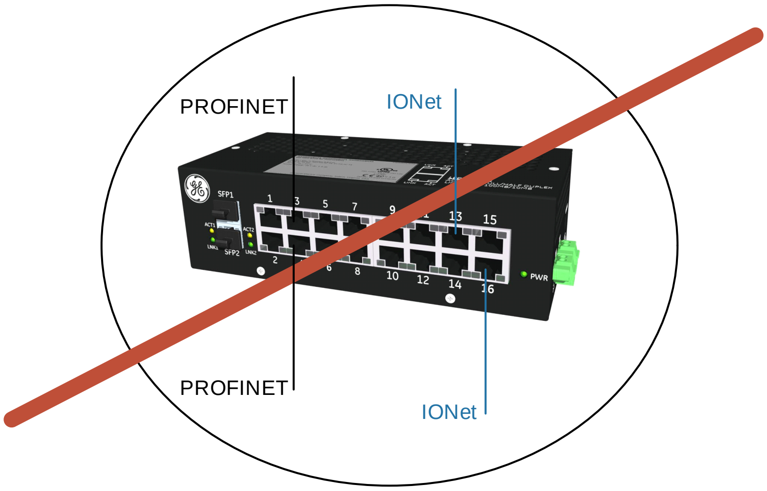
To allow the PPNG to work with smart sensors or other scanner modules, the ToolboxST application supports the import/download of other I/O device configurations by importing the vendor-supplied GSDML file. Refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6700), the section *PPNG PROFINET Module Configuration*.

11.1.1.3 Switches

PROFINET devices should be connected to a separate PROFINET network switch, and should not be mixed with the IONet network. The maximum number of switches that shall be used for PROFINET with one PPNG is five switches (which is the same limitation given for IONet).

Caution

IONet and PROFINET are not allowed through the same switch. Use independent switches for each network type.



GEIP has qualified the following unmanaged switches for use on the PROFINET communication network, between the PPNG and the slave devices:

- ESWA 8–port industrial unmanaged switch
- ESWB 16–port industrial unmanaged switch

Users should order green-colored Ethernet cables for connections between PPNG and all PROFINET devices on the PROFINET network (to help distinguish this network from the IONet).

Green-colored PROFINET Ethernet Cables

GE Part #	Length (feet)
336A4940DTP3GN	3
336A4940DTP5GN	5
336A4940DTP8GN	8
336A4940DTP10GN	10
336A4940DTP12GN	12
336A4940DTP15GN	15
336A4940DTP18GN	18

11.1.1.4 Performance Limits

To prevent overloading of the PPNG, the maximum number of I/O devices that can be configured is limited to the equivalent of eight devices with update rates of 1 ms. Devices configured with longer update periods present smaller data loads to the PPNG. For example, a device with an update rate of 2 ms is equivalent to ½ device at 1 ms.

From the ToolboxST application, different update rates are selectable for inputs and outputs separately. The drop-down box displays these different rates as per the slave's capabilities. The following table assumes that the input and output rates are the same and then lists the limits for these rates. The ToolboxST application enforces these limits with a build error.

PPNG Performance limits

PPNG PROFINET Update Rate	Maximum PROFINET Devices Attached to PPNG
1 ms	8
2 ms	16
4 ms	32
8 ms or more	64

In a line topology, the system limits previously mentioned might not hold true because this is influenced by the types of slaves used in the bus. This is because the traffic from the farthest end of the bus (away from the PPNG) passes through each of the slaves in between before reaching the PPNG. If some intermediate slave has switching hardware that is not capable enough to handle this traffic, then disconnection of devices could occur. Testing has shown issues like this with legacy GE RSTi hardware.

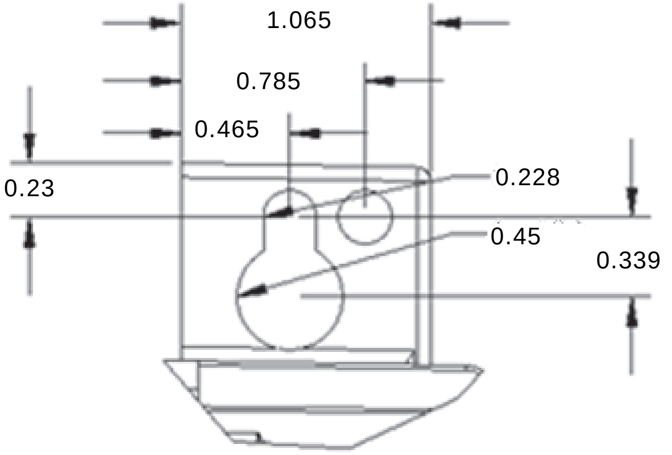
11.1.2 Specifications

Item	PPNG Specifications
Microprocessor	1066 MHz Intel EP80579
Operating System	QNX® Neutrino
Internal Memory	256 MB DDR2 SDRAM with error-correcting code (ECC) NAND flash size is 2 GB
Conformance Class Version	PROFINET IO-RT V2.2 Class A I/O controller
Min ControlST Version	V05.04
Power Requirements	28 V dc typical, 28.7 peak, 17.3 nominal
IS400UCLIH1A	Required ID assembly that connects between the dc power connector and the PPNG Length: ~3 inches
Weight	2.4 lb (1 Kg)
Ethernet Ports	Three RJ-45 10/100 Mbps ports: one for PROFINET, two for IONet (ENET1, ENET2)
Ethernet Cabling Supported	Cat 5e STP for PROFINET and IONet ports
COM Port	Used by GE for development, accepts a standard 4-pair UTP cable joined with a computer null modem connector (GE part #342A4944P1) Can also be used for initial baseload setup
I/O Device Data Update Rates	Configurable: 1ms, 2ms, 4ms, 8ms, 16ms, 32ms, 64ms, 128ms, 256ms, and 512ms
Number of MAC Addresses	Three: one for PROFINET and two for IONET
Maximum I/O Memory	8 KB of input and 8 KB of output memory
Max Number of PPNGs Attached to One Mark VIe Controller	4 (enforced by ToolboxST application) Refer to *GEH-6721_Vol_I*, the section *IONet Specifications* for other limits.
Max Nnumber of PROFINET I/O Devices Attached to One PPNG	Refer to the section, *Performance Limits*.
Network Topology Supported	Star (typical), Line (daisy-chain with PPNG at one end of the bus), or a combination
Max PROFINET Data Rate	6 KB per millisecond
PROFINET Network Speed	100 Mbps full duplex on dedicated PROFINET Network (IONet must be on a separate switch)
I/O Redundancy	Simplex
Media Redundancy Protocol (MRP)	No
Dimensions	Refer to the section, *Installation*.
Ambient Rating for Enclosure Design†	-30 to 65°C (-22 to 149 °F) Vertical mounting

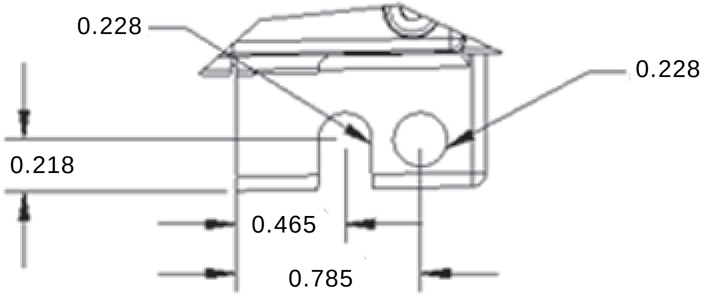
Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

11.1.3 Installation

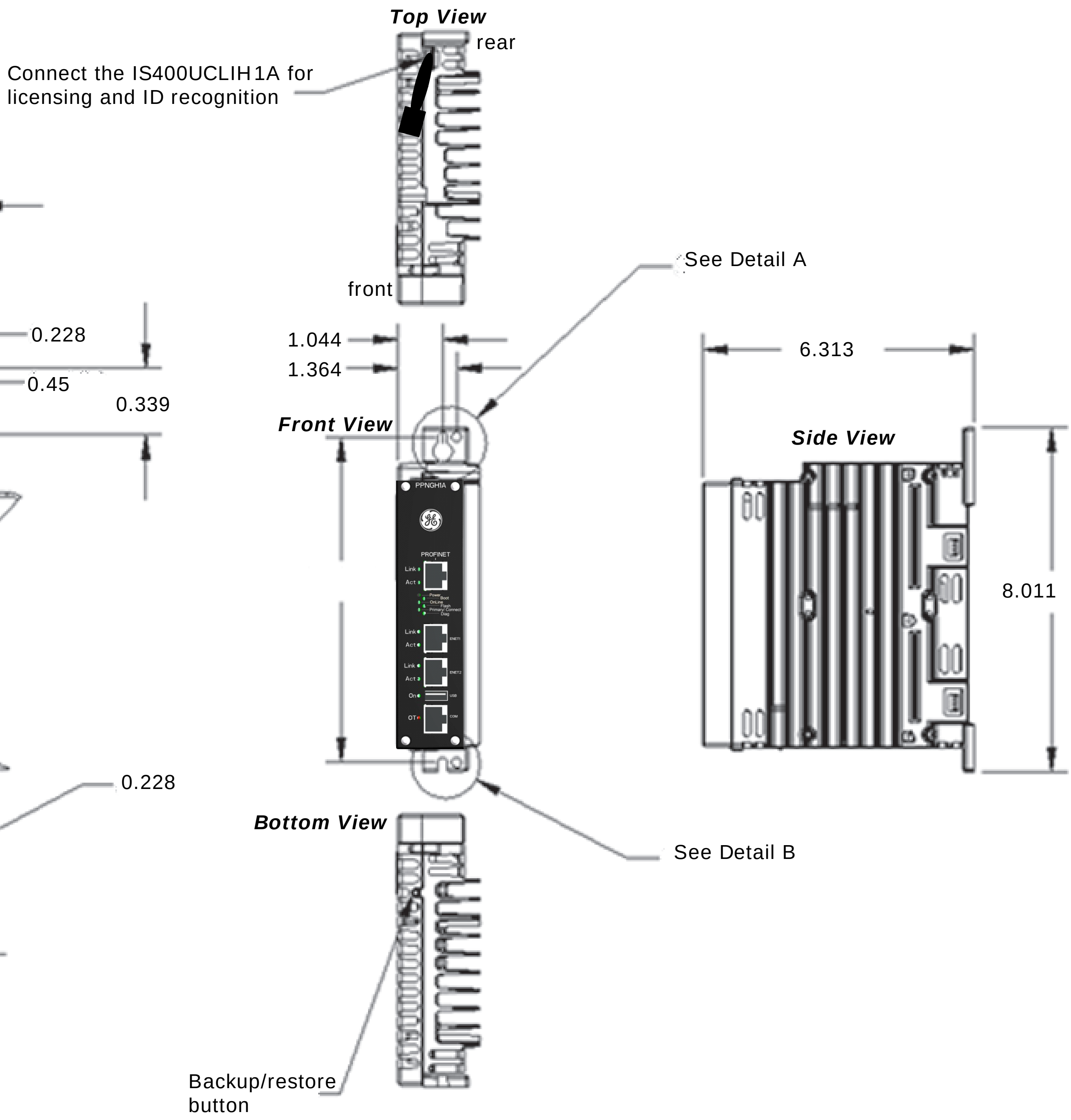
The PPNG is contained in a single module that mounts directly to the panel sheet metal. The following diagrams display the module envelope and mounting dimensions. All dimensions are in inches. The PPNG is to be mounted to the panel as shown with vertical air flow through the fins to be unobstructed.



Detail A



Detail B



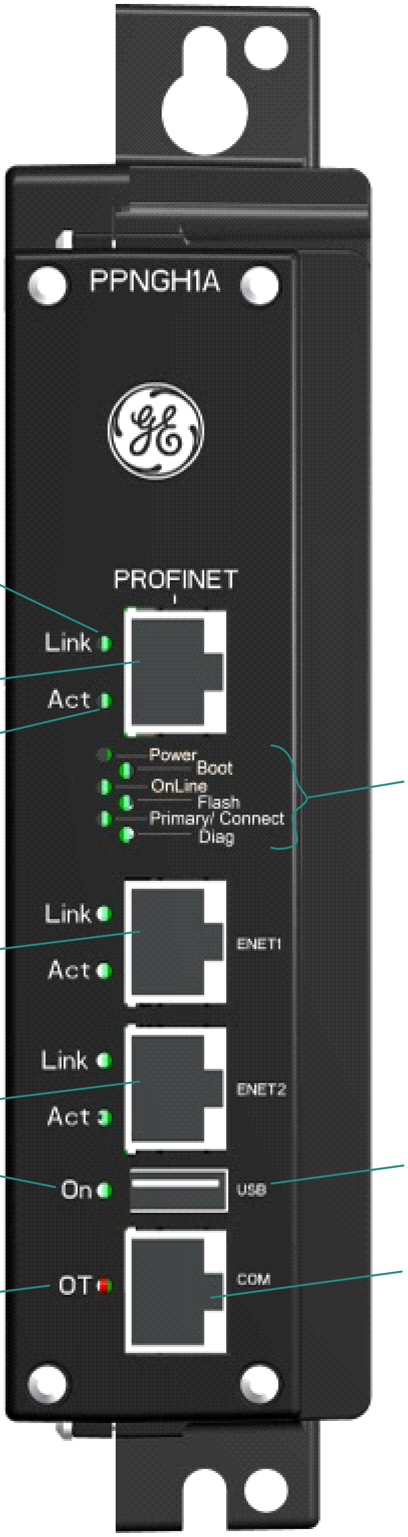
➢ To install the PPNG module

1. Securely mount the PPNG to the panel. Refer to the figure, *PPNG Envelope and Mounting Dimensions*.
2. Connect the *PROFINET Ethernet* STP cable either directly to the PROFINET I/O device (line topology with PPNG at one end of the bus) or to a GE-qualified switch (not the switch used for IONet).
3. From the PPNG ENET1 port, connect an Ethernet cable to the Ethernet switch of corresponding IONet network, which is configured in ToolboxST application for this port. If redundant IONets are used, then connect a cable from the PPNG ENET2 port to the Ethernet switch of the corresponding IONet (configured in the ToolboxST application for that port).
4. Connect the PROFINET I/O devices. Refer to the section, *PROFINET Network Connections* and refer to the device-specific technical manuals for more information.
5. Connect the ID assembly *IS400UCLIH1A* to the power input on the top-rear of the PPNG module. This assembly provides the required PROFINET licensing and terminal board ID recognition for the ToolboxST application.
6. Apply dc power by plugging in the power connector to ID assembly. PPNG has inherent soft-start capability that controls current levels upon application.
7. Use the ToolboxST application to configure the PPNG as necessary. Refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6700), the section *PPNG PROFINET Module Configuration* for more detailed procedures with software screen examples.
    a. From the Component Editor, **Hardware** tab, add the PPNG module.
    b. Run the **I/O Pack Setup Wizard** to transfer the PPNG Base Load from the Mark VIe controller to the PPNG. This requires an unencrypted minimum 4 GB USB memory stick or the alternate method uses a serial cable from the COM port. Help for this wizard is available from the ToolboxST application. After the PPNG is successfully communicating over IONet to the Mark VIe controller, the remainder of the configuration and downloads occur directly from the ToolboxST application (no further use of the USB drive is required).
    c. Configure the PROFINET network data rate. Refer to the *Compatibility* section for system limits.
    d. Attach and configure the PROFINET I/O devices.

Note The I/O device host names must match the names in the ToolboxST configuration. The ToolboxST DCP configuration feature can be used to set the I/O device host names. Right-click the PPNG module and select Identify PROFINET Devices.

8. Perform a series of Builds and Downloads (similar to a standard I/O pack).

11.1.3.1 Front Face Ports



Link LED is solid green when established an Ethernet link with the network switch

PROFINET port

Act LED is solid green when there is sufficient packet traffic or flashes if the traffic is low

Refer to the section *Status LEDs* for details

IONet 1 port

IONet 2 port

Used for the backup/restore of PPNG firmware and for the initial setup of baseload

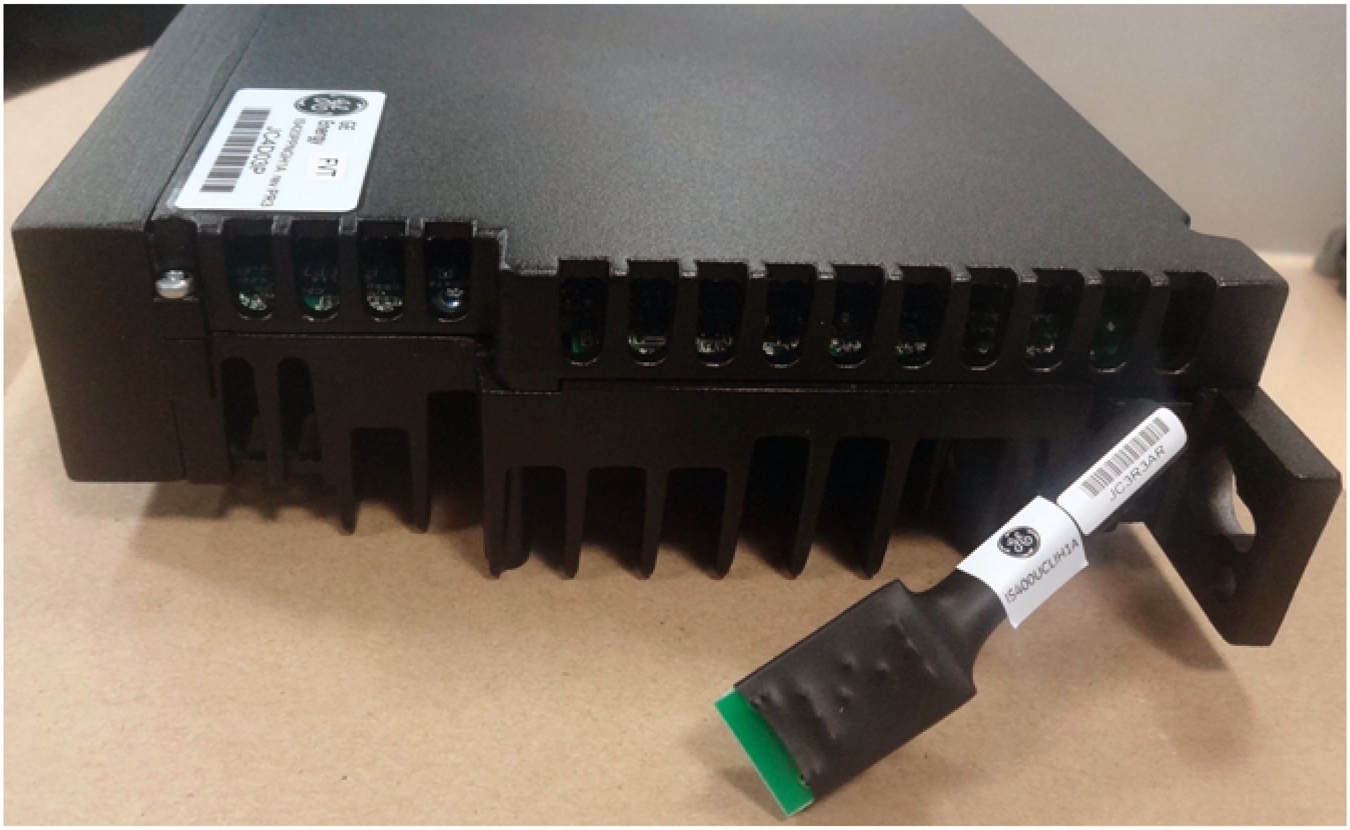
On LED is solid green when the USB port is active

OT Over Temperature LED
Yellow = alarm is present
Red = trip has occurred

Used by GE during development process and optionally instead of USB for initial setup of baseload

11.1.3.2 Required ID Assembly

The IS400UCLIH1A assembly provides the required PPNG licensing and terminal board ID recognition for the ToolboxST application. It connects to the dc power input on the top-rear of the PPNG module (the incoming dc power connects to the other end of this assembly).



PPNG with the IS400UCLIH1A Assembly Attached

11.1.3.3 PROFINET Ethernet Connections

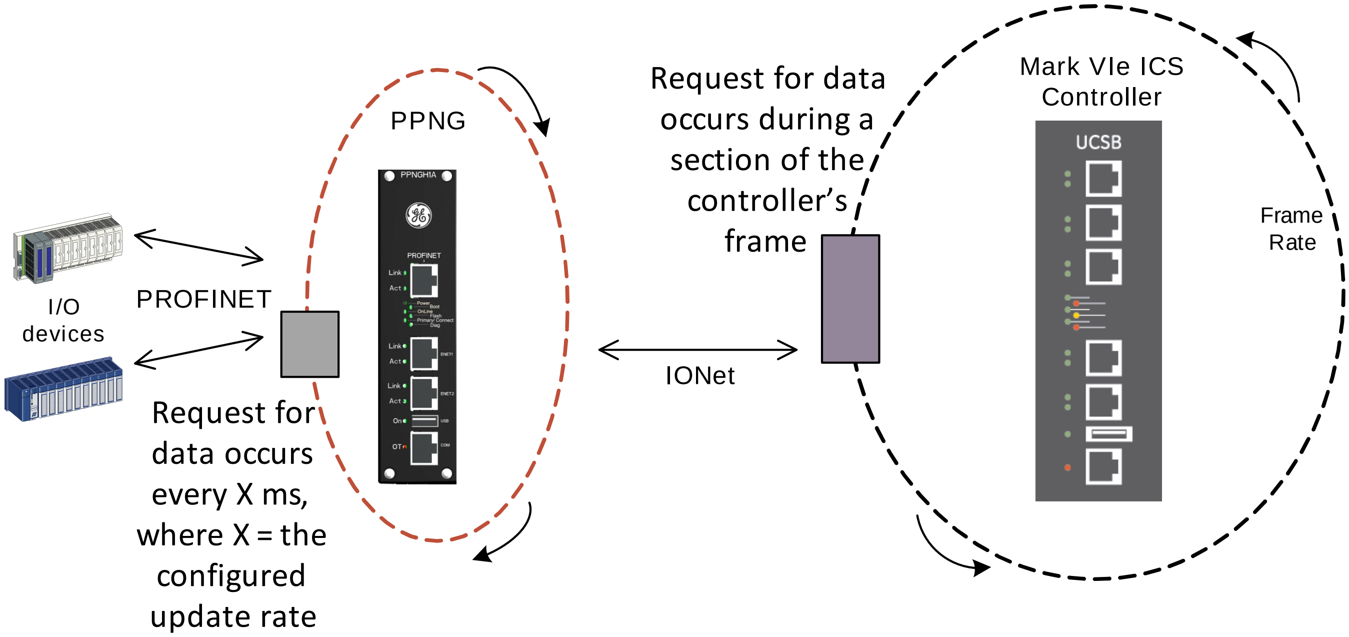
Connect to the PPNG PROFINET port using a Cat 5e shielded twisted pair Ethernet cable. Connect to only one PROFINET network either directly to the device (bus topology with PPNG at one end of the bus) or through a GE-qualified switch. This switch is used to connect more than one PROFINET slave to the PPNG in a star wiring topology. The maximum length of copper cable between any two active devices (switch or PROFINET device) should not exceed 100 meters as directed by Ethernet standards.

11.1.4 Dataflow between PPNG and Mark VIe Controller

Dataflow between the PPNG and the controller is of two types, fixed I/O and PROFINET I/O. The limited amount of fixed I/O includes the inputs common to all I/O packs, for example L3DIAG and IOPackTmpr, but no outputs. The set of fixed I/O is pre-defined in the PPNG firmware. PROFINET I/O consists of the data exchanged with PROFINET slave devices, and its definition varies according to hardware configuration specified by the application.

The PPNG exchanges data with the Mark VIe controller at standard controller frame rates, (10 ms, 20 ms, 40 ms and so forth). Actual PROFINET data size depends on the data transmitted by PROFINET I/O devices. PPNG firmware limits this to a maximum of 8 KB of data in either direction. The ToolboxST application has rules to check for maximum allowable amount of PROFINET data in terms of Ethernet packets. Refer to the section, *Compatibility* for a summary of performance limits with respect to number of data types and configured PPNG data rates.

The exchange of data between the PROFINET I/O device and PPNG is a configurable *update rate*. The frame rate of the Mark VIe controller is also a configurable scan rate. Be aware that these two transfers of data occur asynchronously, as displayed in the following figure.


PPNG
PPNGH1A
PROFINET
I/O devices
PROFINET
Request for data occurs every X ms, where X = the configured update rate
Request for data occurs during a section of the controller's frame
IONet
Mark VIe ICS Controller
UCSB
Frame Rate

Asynchronous Data Exchange

11.1.5 PROFINET Network Communication

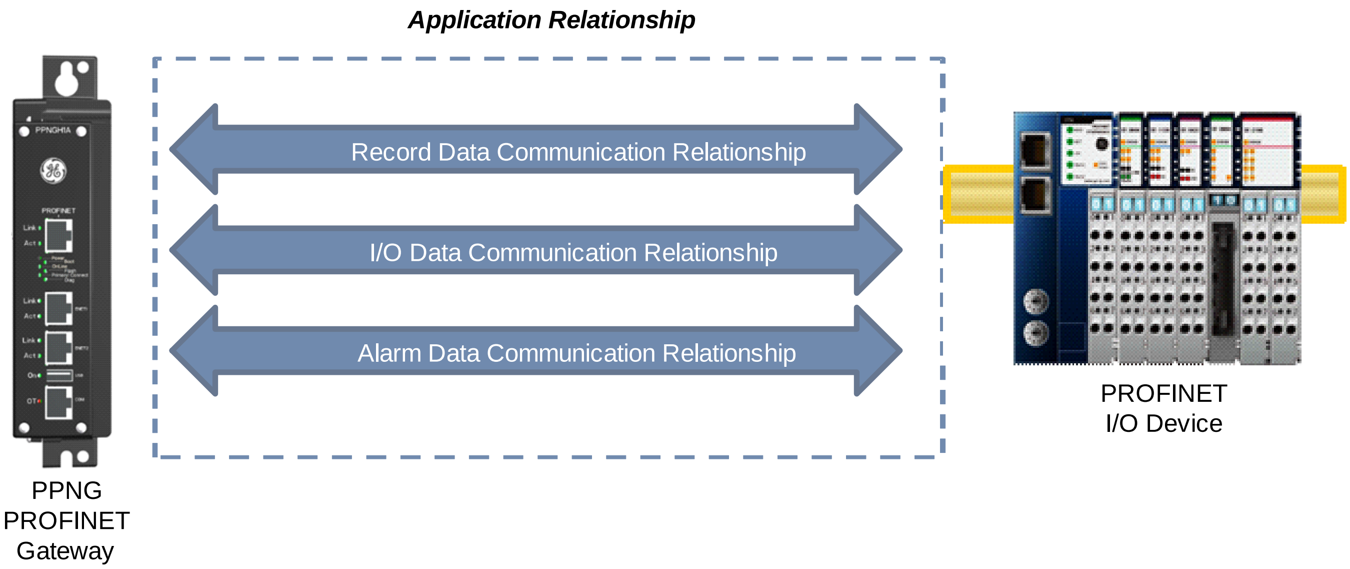
The PPNG uses PROFINET communications for exchanging data between PPNG and PROFINET I/O devices on one side, and it uses IONet communication to exchange data between the Mark VIe controller and the PPNG on the other side. A typical PROFINET network has the following components:

- **PROFINET I/O controller** – the PPNG acts as a PROFINET I/O controller. It controls one or more PROFINET I/O devices with read/write of associated data.
- **Ethernet switch** – the GE-qualified general-purpose unmanaged Ethernet switch is used to route data from multiple PROFINET I/O devices to the PROFINET I/O controller (PPNG)
- **PROFINET I/O devices** – are distributed I/O devices hosting various data types that communicate to the PPNG.

Before the PPNG can exchange data with a PROFINET I/O device, an application relationship (connection) must be established between the devices. The PPNG automatically sets up the correct number and types of Communication Relationships (CRs) based on its ControlST configuration.

The following CR types are established between the PPNG and the I/O devices:

- Record Data CRs – is always the first to be established within an application relationship. They are used for non real-time transfers of data records, such as startup parameters, diagnostics, identifications, and configurations.
- IO CRs – used for real-time, cyclic transfer of I/O data
- Alarm CR – used for real-time, acyclic transfer of alarms and events


Application Relationship
Record Data Communication Relationship
I/O Data Communication Relationship
Alarm Data Communication Relationship
PROFINET
I/O Device
PPNG
PROFINET
Gateway

11.1.6 Diagnostics

The PPNG has the following LEDs:

- **Link** displays solid green if the PPNG Ethernet port has established a link with an Ethernet switch port.
- **Act** indicates packet traffic on an Ethernet interface. This LED flashes if the traffic is low, but is solid green in most systems.
- **Power** displays solid green when the internal 5 V dc supply is on and regulating. The PPNG converts the incoming 28 V dc to 5 V dc. All other internal power planes are derived from the 5 V dc.
- **Online** displays solid green when the PPNG is online and running application code.
- **Flash** displays amber when any flash device is being accessed.
- **Primary/ Connect** is solid green if the PPNG is a primary PROFINET module and all configured devices are connected. If at least one device is not connected, then the LED flashes at a 1 Hz frequency (on for 500 ms and off for 500 ms).
- **Diag** displays solid red when the PPNG has an active diagnostic. The diagnostic can be viewed and cleared using the ToolboxST application.
- **On** displays solid green when the USB port is active.
- **OT** displays yellow when an over-temperature alarm is present or red when a temperature trip has occurred
- **Boot** displays solid red or flashing red during the boot process.

11.1.6.1 Boot LED Flashing Codes

The boot LED is lit continuously during the boot process unless an error is detected. It flashes at a 1 Hz frequency if an error is detected. The LED, when flashing, is on for 500 ms and off for 500 ms. After the flashing state, the LED turns off for three seconds. The number of flashes indicates the failed state.

Boot LED Flashing Codes

State	Description	# of Flashes
Executing BIOS	Normally booting BIOS	On
Failed SPD	SPD has bad data	1
Failed DRAM	DRAM memory test has failed in the BIOS	2
Failed BIOS SPI	BIOS was unable to validate the BIOS SPI checksum	3
Failed CPLD	BIOS was unable to communicate with the complex programmable logic device (CPLD)	4
Failed APP SPI	BIOS was unable to communicate with the APP SPI	5
Failed QNX IFS	BIOS was unable to read or verify the QNX IFS image	6
Fully Booted	Fully Booted	Off

11.1.6.2 Variables

The following PPNG input variables are available for connection to Mark VIe controller application logic in support of operator screen indications for PPNG module status.

Variable Name	Type	Description
L3DIAG_PPNG_R	Input BOOL	True indicates that the PPNG has at least one diagnostic alarm in the queue (active or normal state)
LINK_OK_PPNG_R	Input BOOL	True indicates that the IONet communication link is okay
ATTN_PPNG_R	Input BOOL	True indicates that the PPNG has at least one active diagnostic alarm
PROFI_BACKUP_PPNG_R	Input BOOL	This would always be False in case of simplex PPNG as it is always a primary PPNG. A True would indicate that the specific PPNG is acting as a Backup in the case of redundant PPNGs (not currently supported).
CPU_HOT_PPNG_R	Input BOOL	This signal is True if the PPNG processor temperature has exceeded 97 °C (207 °F)
BoardTmpr_PPNG_R	AnalogInput REAL	PPNG processor temperature in degrees F

11.1.6.3 PROFINET I/O Device Diagnostics

PROFINET I/O devices (slaves) provide alarms and events that are received by the PPNG. From the ToolboxST application, these slave device messages can be reset after viewing. PROFINET slave device alarms and events are not forwarded to the Mark VIe controller or the WorkstationST Alarm Viewer. The following table defines the slave device message types supported by the PPNG.

Alarm	Type
0x0001	Diagnosis
0x0003	Pull
0x0004	Plug
0x0005	Status
0x0006	Update
0x0008	Controlled by Supervisor (Logical Pull)
0x0009	Released (Logical Plug)
0x000A	Plug Wrong Submodule
0x000B	Return of Submodule
0x000C	Diagnosis Disappears
0x000E	Port data change notification
0x0011	Network component problem notification
0x0013	Dynamic frame packing problem indication
0x0016	Multiple Interface mismatch notification

11.2 PPNG Specific Alarms

The following diagnostic alarms are specific to the PPNG module.

32

Description Configuration Incompatible: Old - [ ]; New - [ ]

Possible Cause An online load was attempted on a configuration change that requires a PPNG to be restarted.

Solution From the ToolboxST application, build and download the firmware and configuration to the PPNG. Wait for the PPNG to restart and verify its status.

33

Description PPNG is not connected — invalid component hardware detected

Possible Cause The user has connected the wrong component hardware to a system that is expecting the PPNG module hardware.

Solution Uninstall the invalid component hardware and install the proper PPNG module hardware.

34

Description License unavailable for running PPNG

Possible Cause The user has not connected the required ID assembly (GE part # 336A4937RDG036) to the dc power input of the PPNG module.

Solution Disconnect the dc connector to power off the PPNG. Connect the ID assembly to the PPNG power input. Connect the dc power connector to the other end of the ID assembly to power up the PPNG.

165

Description Redundant PPNG Peer-to-Peer Communication Timeout

Possible Cause Embedded PPNG is unable to communicate with the Peer Embedded PPNG over one or both of the R and S IONets:

- Peer Embedded PPNG is not online or configured properly
- Peer Embedded PPNG is not communicating on the R and S IONets due to IONet failure

Solution

- Using ToolboxST, verify that both Embedded PPNGs are downloaded properly with the correct firmware and parameters.
- Verify the R and S IONets are healthy. Replace any faulty Ethernet cables or switches as necessary.

166

Description PROFINET I/O Device Diagnostic Detected

Possible Cause PPNG has detected that one of the attached PROFINET I/O devices has a diagnostic alarm.

Solution From the ToolboxST application, PPNG configuration, select the **Profinet Diagnostics** tab to display PROFINET I/O device diagnostic alarms.

2400–2527

Description Device Configuration Error: Device [ ]

Possible Cause Incorrect PROFINET I/O Device Configuration

Solution From the ToolboxST application, update the PROFINET device configuration. Build and download the firmware and configuration to the PPNG. Wait for the PPNG to restart and verify its status.

2528–2655

Description Device Communication Error: Device [ ]

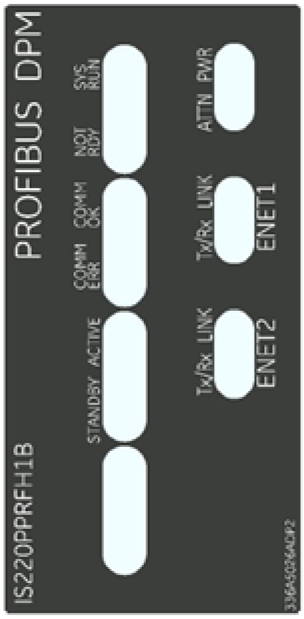
Possible Cause The PPNG cannot communicate with the PROFINET I/O Device

Solution

- Verify that the PROFINET I/O device is functioning as expected or replace if needed.
- Verify that the Ethernet cables are connected and functioning as expected or replace if needed.
- Verify that the PROFINET switch is functioning as expected or replace if needed.

12 PPRF PROFIBUS® Master Gateway

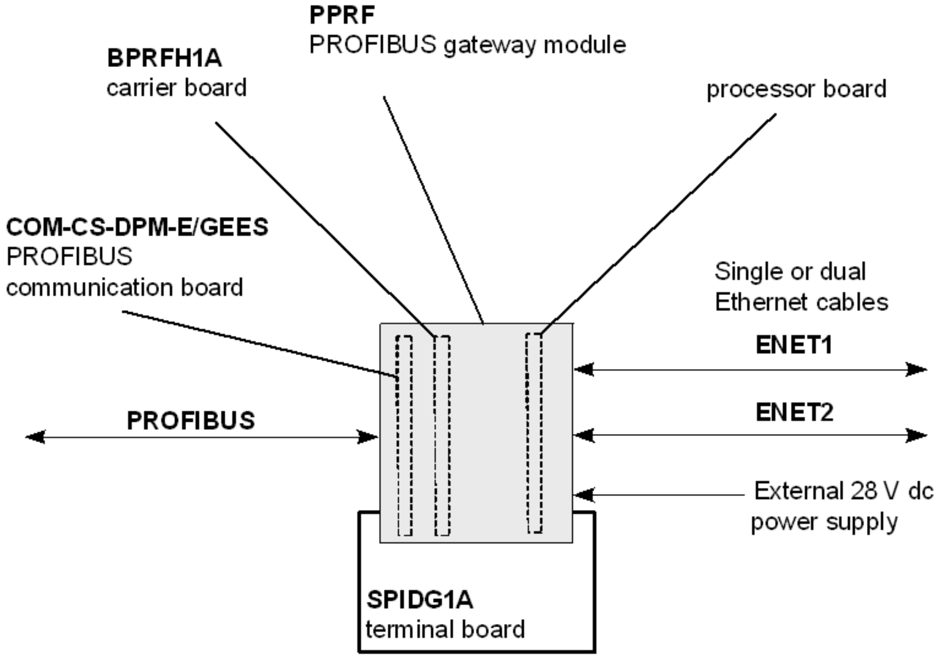
12.1 PPRF PROFIBUS Master Gateway I/O Pack

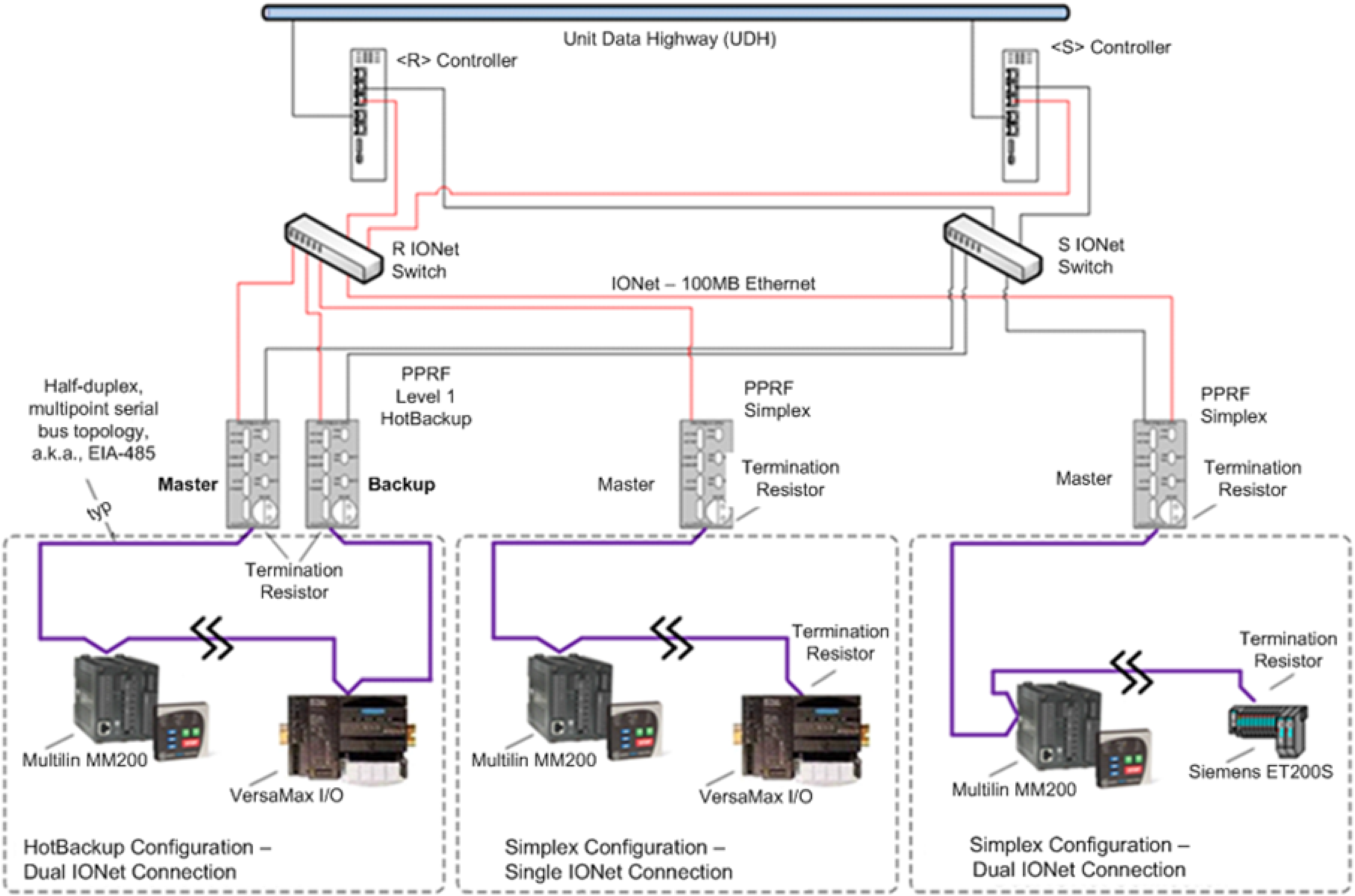


The PROFIBUS Master Gateway (PPRF) I/O pack is a PROFIBUS DP-V0 or DP-V1, Class 1 Master, that maps I/O from PROFIBUS slave devices to Mark* VIe controllers on the IONet. The I/O pack contains a BPPx processor board and an acquisition carrier board fitted with a COM-C PROFIBUS communication module supplied by Hilscher GmbH.

The COM-C module provides a PROFIBUS RS-485 interface through a DE-9 D-sub receptacle connector. It serves as a PROFIBUS DP master supporting transmission rates from 9.6 Kbps to 12 Mbps and up to 124 slaves with up to 244 bytes of inputs and outputs per slave.

The PROFIBUS Master Gateway Terminal board (SPIDG1A) is used to mount the I/O pack and to supply an electronic ID. Its only connection is the interface to the I/O pack itself, as the PROFIBUS connection is made to the DE-9 D-sub receptacle connector exposed on the side of the I/O pack. Visual diagnostics are provided through indicator LEDs on the I/O pack.





Typical PROFIBUS Setup

12.1.1 Compatibility

The PPRF I/O pack includes one of the following BPPx processor boards:

- PPRFH1A contains a BPPB processor board
- PPRFH1B contains a functionally compatible BPPC that is supported in the ControlST* software suite V04.04 and later

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Note The DP-V1 and DP-V0 are available with PPRFH1B and ControlST software suite V4.06 or later. Prior to V04.06, only DP-V0 was available.

The PPRF supports the following redundancy options:

- Single I/O pack with single I/O Ethernet connection (no redundancy)
- Single I/O pack with dual I/O Ethernet connections
- HotBackup I/O pack with dual I/O Ethernet connections

The dual I/O Ethernet connection configuration is common to other I/O packs. However, in the HotBackup, two PPRFs are employed, one operating as the active PROFIBUS master communicating with slave devices, and the other operating in a passive, stand-by mode, ready to become the active master if an active master failure occurs.

Redundancy	Hardware Form	IONet Connections	Frame Rate
Simplex	H1A	One or Two	† 20, 40, 80, 160, 320
HotBackup	H1A	Two**	† 20, 40, 80, 160, 320
Simplex	H1B	One or Two	10, 20, 40, 80, 160, 320
HotBackup	H1B	Two**	10, 20, 40, 80, 160, 320
HotBackup	H1A / H1B*	Two**	† 20, 40, 80, 160, 320
* If a PPRFH1B is used as a replacement pack on a HotBackup configuration, it can only be configured to the same frame rates supported by the PPRFH1A.			
** HotBackup uses two I/O packs with two Ethernet connections for each I/O pack.			

Caution

† The PPRFH1A can be configured for 20 ms frame period, but this is not recommended for new applications. It is the responsibility of the application engineer to qualify fitness for use at 20 ms.

12.1.2 Installation

➢ **To install the PPRF I/O pack**

1. Securely mount the SPID terminal board to the PPRF I/O pack.

2. Directly plug the PPRF into the terminal board connector. For HotBackup configurations, repeat steps 1 and 2 with a second SPID and PPRF.

3. Mechanically secure the PPRF(s) using the threaded inserts adjacent to the Ethernet ports. The inserts connect to a mounting bracket specific to the terminal board type. The bracket should be adjusted so there is no right angle force applied to the DC-37 pin connector between the I/O pack and the terminal board. This adjustment is required once during the service life of the product.

4. Plug in one or two Ethernet cables depending on the system configuration. The pack operates over either port. If dual connections are used, standard practice is to hook ENET1 to the network associated with the R controller; however, the PPRF is not sensitive to Ethernet connections and will negotiate proper operation over either port.

5. Connect and secure the PROFIBUS cable into the DE-9 D-sub receptacle connector. As per PROFIBUS requirements, the PROFIBUS Network must be terminated on each end.

6. Apply power to the connector on the side of the I/O pack(s). It is not necessary to insert the connector with power removed from the cable. The PPRF has inherent soft-start capability that controls current inrush on power application.

7. Use the ToolboxST application to add and configure the I/O pack(s), and the PROFIBUS network. From the Component Editor, press F1 for help.

12.1.2.1 Bus Installation Guidelines

The proper cable for a PROFIBUS network is a shielded, twisted-pair cable, and is sold simply as *PROFIBUS Network Cable*. This twisted pair cable consists of a green wire and a red wire.

The following table lists some of the characteristics of the PROFIBUS network and cable.

Item	Specification
Network Topology	Linear bus, terminated at both ends. Stubs possible.
Medium	Shielded twisted pair cable. Shielding may be omitted, depending on the environment.
Number of Stations	32 stations in every segment without repeaters. With repeaters, extendable up to 124.
Transmission Speed	9.6, 19.2, 31.25, 45.45, 93.75, 187.5, 500, 1500 Kbps 3, 6, 12 Mbps
Connector	9-pin D-sub connector
Cable Type	PROFIBUS DP
Surge Impedance	135 to 165 Ohms (3 to 20 MHz)
Working Capacitance	< 30 pF per meter
Loop Resistance	≤ 110 Ohms per Kilometer
Wire Diameter	> 0.64 mm
Conductor Cross-sectional Area	> 0.34 mm^2
L/R Ratio	≤ 15 μH/Ohm

The maximum bus length using shielded, twisted-pair cable for a single network segment is 1200 meters. Total network length can be increased with the use of repeaters, with up to a maximum of three repeaters per network. Other cable types are restricted to shorter bus lengths. The maximum bus length also depends on the data rate, as displayed in the following table.

Maximum Bus Length in Meters	Kbits per Second
1,200	9.6; 19.2; 31.25; 45.45; 93.75
600	187.5
400	500
200	1,500
100	3,000; 6,000; 12,000

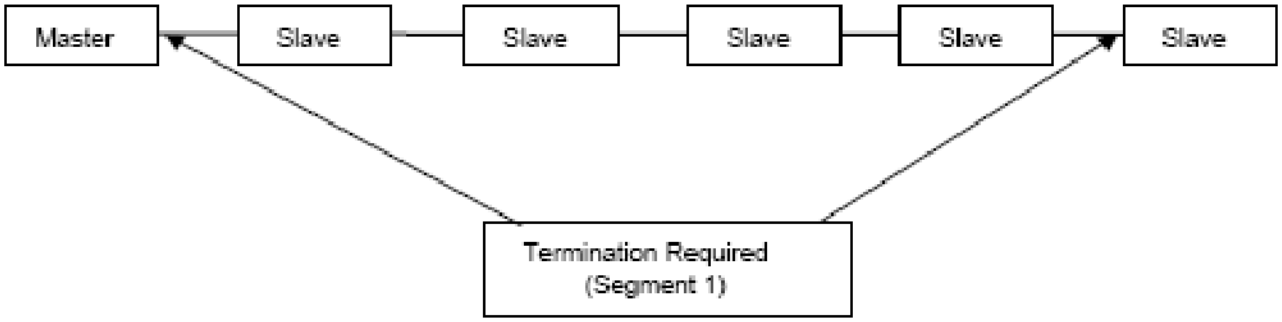
Often, it is the required bus length that determines the data rate. For data rates up to 500 Kbits/second, follow the stub recommendations of PROFIBUS Part 1. At 1500 Kbps the overall drop capacity should be less than 0.2 nF. The maximum length of the stub at 1500 Kbps is 6.6 meters. Cable shielding is recommended at higher baud rates, to maintain communications integrity in the industrial environment.

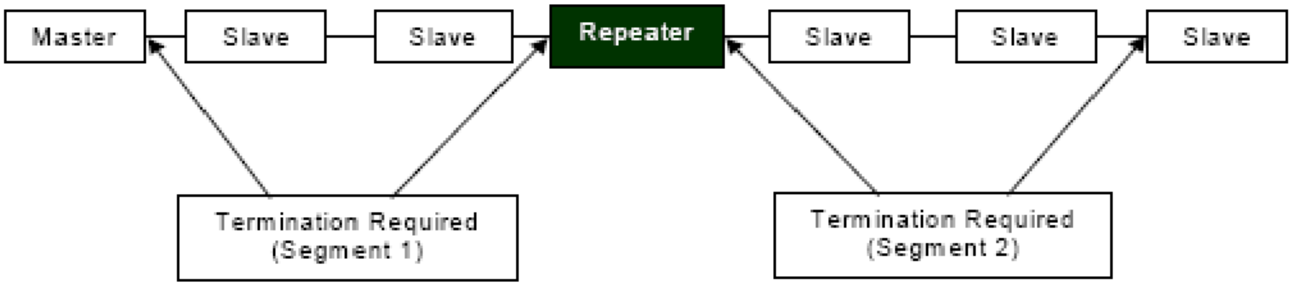
Typically the Slave device provides the PROFIBUS standard female 9-pin D subminiature connector. The mating male cable connectors are available from most fieldbus parts distributors as PROFIBUS 9-pin D connectors. These connectors often provide termination resistors and a switch on the connector to enable/disable termination. Connectors with and without termination are also available.

The connectors generally label the connections for the twisted pair as cable A and cable B. The following table illustrates the proper assignment of wire to connector to pin to signal.

Wire Color	Connector	Pin	Signal
Red	B	3	RxD / TxD-P
		5	DGND
		6	VP
Green	A	8	RxD / TxD-N

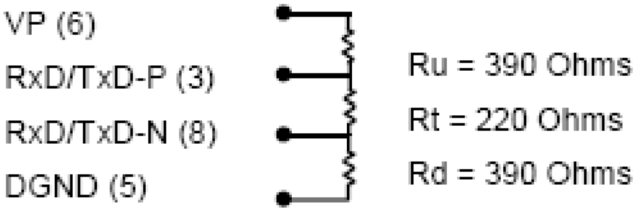
Termination resistors are needed, as displayed in the following figures. One terminator must be applied at each end of a network segment.



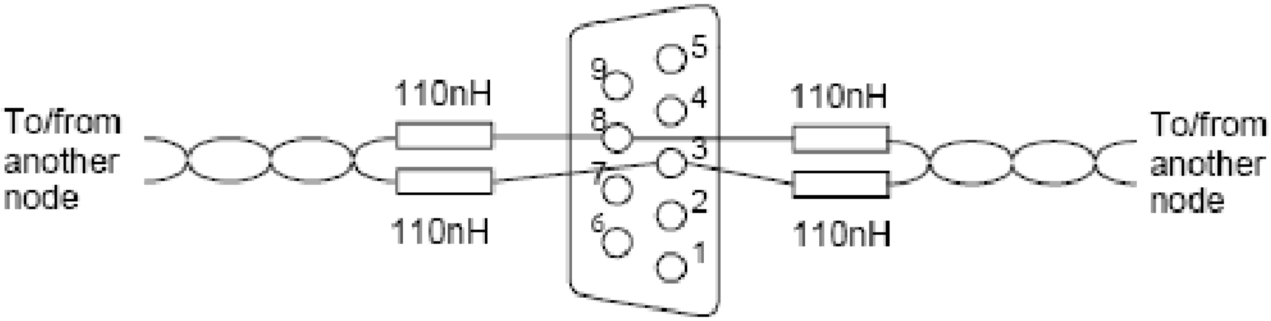


Attention

For proper network termination, the terminating devices must provide and maintain power. Power is provided by the device on Pin 6 and Ground is provided on Pin 5. If power is lost to either terminating device, the network may not operate correctly. Generally, the network Master device is one of the terminating devices. The other terminating device may be a critical Slave device or a separately powered, stand-alone terminator.

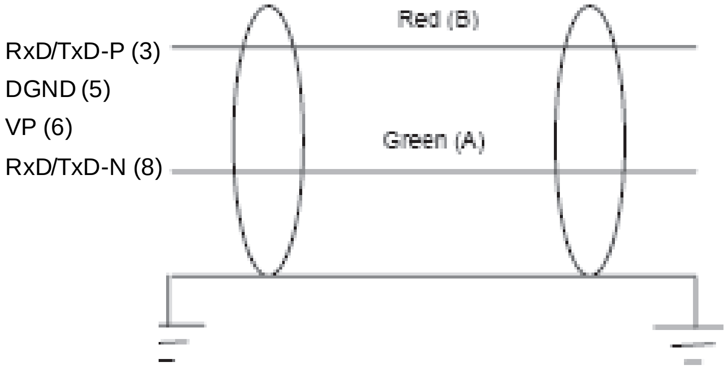


In addition to the termination displayed previously, the following compensation should be added for 12 Mbit bus technologies.



Generally, it is only necessary to ensure that the cable shields are attached to ground. In most cable connectors, the shield is attached to the metal housing of the conductor on the cable side and this is brought to ground by the metal connector on the Slave device.

In some installations with large networks or higher data rates, large ground potentials (greater than ±7 V) can occur. In these cases, it may be necessary to ensure all PROFIBUS devices are attached to the same Protective Earth ground.



Note For a more detailed discussion of the PROFIBUS DP communication networks using RS-485, including intrinsically safe applications, refer to the document, *Profibus RS 485-IS User and Installation Guideline*.

12.1.3 Operation

The following features are common to the distributed I/O modules:

- *BPPx Processor*
- *Processor LEDs*
- *Power Management*
- *ID Line*
- *I/O Module Common Diagnostic Alarms*

12.1.3.1 PROFIBUS Gateway Function

The PPRFs COM-C module, built on a PROFIBUS core based on Siemens® ASPC2 technology, contains firmware that implements the PROFIBUS DP (Decentralized Periphery) functionality. The PPRF provides PROFIBUS DP-V0 and DP-V1 functionality, which includes configuring slave devices, cyclically exchanging I/O data with them, obtaining PROFIBUS diagnostics, and online parameterization using Device DTM and DP-V1 messaging.

The COM-C's firmware, residing in a flash memory, is released as part of the PPRF firmware and downloaded to the COM-C's flash at I/O pack startup time only if necessary (for instance when the PPRF firmware is released with an updated COM-C firmware).

The COM-C module requires a PROFIBUS configuration file that is created by the ToolboxST application. This file, specifying the DP master parameter set, is loaded from the ToolboxST application along with the other standard I/O pack configuration files, and, if changed, requires a PPRF reboot following the load. As is the case with the COM-C firmware file, the PROFIBUS configuration file is stored in COM-C flash and only downloaded from PPRF flash if necessary.

To support a broader set of field devices and device management/asset management applications, GE has leveraged the benefits of FDT technology by developing a set of FDT Group certified DTMs to provide HART over Ethernet and PROFIBUS DP-V1 over Ethernet Device Manager capability in coordination with the Device Manager Gateway. The DTMs allow management of HART and PROFIBUS DP-V1 devices from any FDT frame application from virtually any computer. For further details, refer to the *Device Manager User Guide* (GEH-6821).

PPRFH1B supports DP-V1 for devices with DTMs available. DP-V1 requires the following:

- DTM support, uses GE's PROFIBUS Communication DTM
- Device must support and supply FDT certified DTM

Note DP-V1 is used for acyclic and cyclic data exchange and alarm handling.

12.1.3.2 Input Events

The PPRF optionally supports input Boolean sequence of event logging referred to as input event detection. PPRF input event time tagging has a 10 ms resolution.

12.1.3.3 HotBackup Redundancy

The PPRF supports a HotBackup redundancy configuration in which two PPRFs operate in tandem, one being the active master and the other retaining a standby status. The active master exchanges I/O with the PROFIBUS slaves and receives generated diagnostics. The backup master operates in standby mode, not communicating with the slave devices but ready to automatically assume the active role if any of the following occur:

- The active master loses communication connectivity with the PROFIBUS slaves (such as, the PROFIBUS cable is disconnected)
- The active master loses communication connectivity on both I/O Ethernets (such as, both Ethernet cables are disconnected or Ethernet switch connection, Ethernet cable disconnection combinations, and such, occur. Redundant Ethernet connections are required for each PPRF, and losing a single Ethernet does not cause a switch.)
- The active master is powered down or *fails*.

Since the switchover time is less than 200 ms, slave watchdog timeout values should not be set to less than that value so that the slaves do not timeout during the portion of the interval in which no PROFIBUS communication takes place. Given that the slave watchdog timeout is set sufficiently large, PROFIBUS I/O values should not spike or drop-out during the switchover period. They may, however, flat-line momentarily.

Unlike what is done in dual or TMR-pack cases, in the PPRF HotBackup configuration, the two PPRFs are assigned different producer IDs. Different controller application variables may be assigned to the fixed Class 1 inputs that are received from each pack (such as, L3Diag). The fixed inputs include an active/backup status Boolean from each PPRF (PROFI_BACKUP_PPRF_R and PROFI_BACKUP_PPRF_S, respectively).

Single application variables are assigned to the PROFIBUS I/O, and data exchange to and from those variables takes place regardless of which PPRF is active. When a backup-to-active switch occurs, the controller automatically switches data exchange between its variables and the newly active PPRF. The controller application takes no part in backup switching and does not have to supply PPRF-specific, separate variables for each PROFIBUS I/O point.

Note If there is a partial PROFIBUS network failure, where both packs are able to communicate with different subsets of slave devices, I/O is only transferred with the slave devices that the primary master has access to. At the same time, the backup master does not try to transfer I/O to the slave devices it is connected to, unless a backup-to-active master switch is initiated. However, if this is done, transfers take place only with the slave devices connected to the newly active I/O pack.

12.1.3.4 Dataflow between PPRF and Mark VIe Controller

Dataflow between the PPRF and the controller is of two types, fixed I/O and PROFIBUS I/O. The limited amount of fixed I/O includes the inputs that are common to all I/O packs, for example L3DIAG and IOPackTmpr, but no application-driven outputs. The set of fixed I/O is pre-defined in the PPRF firmware. PROFIBUS I/O consists of the data exchanged with PROFIBUS slave devices, and its definition varies according to hardware configuration specified by the application.

The PPRF supports varying amounts of I/O depending on the frame rate and the hardware form of the PPRF (H1A/H1B). The PPRF does not place an architectural limit on the number of I/O points, however, the following table contains recommended limits.

Note Any application that goes beyond the recommended limits should be fully validated.

Recommended Limits

PPRFH1A			
Frame Rate (ms)	**Boolean I/O 50/50 Inputs/Outputs**	**Analog I/O 50/50 Inputs/Outputs**	**Total I/O Points**
40	500	500	1000
†20	†	†	†
†Qualify per application. The PPRFH1A can be configured for 20 ms frame period, but this is not recommended for new applications. It is the responsibility of the application engineer to qualify fitness for use at 20 ms.			
PPRFH1B			
Frame Rate (ms)	**Boolean I/O 50/50 Inputs/Outputs**	**Analog I/O 50/50 Inputs/Outputs**	**Total I/O Points**
20, 40	0	1200	1200
20, 40	416	900	1316
20, 40	832	600	1432
20, 40	1248	300	1548
20, 40	1664	0	1664
10	0	600	600
10	288	450	738
10	576	300	876
10	864	150	1014
10	1152	0	1152

Note Total input data cannot exceed 3584 bytes and total output data cannot exceed 3584 bytes. Total combined input and output data cannot exceed 7168 bytes.

12.1.4 Specifications

Item	PPRF Specification
PROFIBUS Master Type	DP-V0 Class 1 Master DP-V1 Class 1 Master (PPRFH1B only)
PROFIBUS Connection	RS-485 interface through DE-9 D-sub receptacle connector
Transmit Time	PROFIBUS output data from the Mark VIe control is received once per frame, up to 25 times per second at 40 ms frame rate or 100 times per second at 10 ms frame period (PPRFH1B only). It is asynchronously transmitted by the COM-C module to PROFIBUS slaves as fast as possible, governed by the PROFIBUS network baud rate, number of slaves, size of data packets from each slave, and slave response time.
Receive Time	PROFIBUS inputs are asynchronously received by the PPRF COM-C module as fast as possible, governed by the PROFIBUS network baud rate, number of slaves, size of data packets from each slave, and slave response time, then scanned by the PPRF firmware 25 times per second at 40 ms frame rate, and transmitted to the Mark VIe control once per frame, up to 25 times per second.
PROFIBUS Transmission Speeds	9.6 Kbps to 12 Mbps
Number of Slaves	124 slaves with up to 244 bytes of inputs and outputs per slave
I/O Throughput	For recommended limits, refer to the table in the section, *Dataflow between PPRF and Mark VIe Controller*. This design criteria does not apply to all PROFIBUS network configurations. I/O throughput capability varies based on PROFIBUS network configurations.
Total I/O Data Max	Total input data cannot exceed 3584 bytes and total output data cannot exceed 3584 bytes. Total combined inputs and outputs cannot exceed 7168 bytes.
Input Event Detection	Available on input Booleans, 10 ms resolution
Size	8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in x 1.65 in x 4.78 in)
Technology	Surface mount
Ambient Rating for Enclosure Design†	-20 to 55ºC (-4 to 131 ºF)

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

12.1.5 Diagnostics

The PPRF receives and stores all PROFIBUS diagnostics generated by slave devices. In addition to any portion of the diagnostic data (including the standard and extended portions), controller applications receive an input Boolean that is set to True when PROFIBUS diagnostics have been received from one or more slave devices (diagnostics presence) and also receive input Booleans set to True to identify specific slave devices that have generated diagnostics (station diagnostics presence).

The ToolboxST application provides an Advanced Diagnostics command, as part of the Troubleshoot Module, which can be used to display the PROFIBUS diagnostics bytes that are generated by slave devices.

12.1.5.1 PPRF LEDs

A green LED labeled SYS RUN indicates three different conditions as follows:

- LED solid on – the COM-C module has established communication with at least one PROFIBUS slave device
- LED flashing fast cyclically (5 Hz) – PROFIBUS master is configured and ready to communicate with slaves but is not connected or otherwise unable to communicate
- LED flashing non-cyclically (3 times at 5 Hz then 8 times between 0.5 Hz and 1 Hz) – the COM-C module is either missing a PROFIBUS configuration or its watchdog timer maintained with the I/O pack firmware has timed out (120 ms timeout)

A yellow LED labeled NOT RDY indicates three different conditions as follows:

- LED flashing slowly cyclically (1 Hz) – COM-C module is waiting for a firmware load
- LED flashing fast cyclically (5 Hz) – COM-C firmware download in progress
- LED flashing non-cyclically (3 times at 5 Hz then 8 times between 0.5 Hz and 1 Hz) – serious COM-C hardware for firmware error

Note If both the SYS RUN and NOT RDY LEDs are off at the same time, either power is not applied or the COM-C module is being reset (which happens during an active to backup redundant PPRF transition). In all other conditions, one or the other LED will be on (though maybe flashing). The SYS RUN LED lights when the COM-C module’s SYS LED is green; the NOT RDY LED lights when the COM-C module’s SYS LED is yellow.

A green LED labeled COMM OK mimics the COM-C COM LED when it is yellow:

- LED solid on – the COM-C module is holding the PROFIBUS token and is able to transmit PROFIBUS telegrams to slave devices
- LED flashing non-cyclically (between 0.5 Hz and 100 Hz) – the COM-C module is sharing the PROFIBUS token with other master devices on the network. This takes place in HotBackup configurations
- LED out – the COM-C is not communicating on the PROFIBUS network

A red LED labeled COMM ERR mimics the COM-C COM LED when it is red:

- LED solid on – the COM-C module has encountered a communication error
- LED out – check COMM OK LED for communication status

Green LEDs labeled ACTIVE and STANDBY that are lit solidly in a mutually exclusive fashion:

- ACTIVE LED solid on – PPRF is the active master
- STANDBY LED solid on – PPRF is the backup master

12.1.5.2 Health

Each PROFIBUS input has an associated health bit allocated in the inputs EGD exchange. The PPRF sets input health to unhealthy when any of the following conditions occur:

- Loss of communication between the associated slave device and the PROFIBUS master
- Loss of COM-C module READY/RUN status
- Standard I/O Ethernet input validation error

PROFIBUS diagnostics other than the station diagnostics presence inputs, the Station_Non_Existent diagnostic, and the diagnostics presence input become unhealthy if any of the following conditions occur:

- The Station_Non_Existent diagnostic is True.
- Loss of COM-C module READY/RUN status
- The slave is not configured in the master.

The station diagnostic presence inputs and Station_Non_Existent diagnostic inputs become unhealthy if either of the following conditions occur:

- Loss of COM-C module READY/RUN status
- The slave is not configured in the master.

The diagnostics presence input becomes unhealthy when the following condition occurs:

- Loss of COM-C module READY/RUN status

12.1.5.3 PPRF Slave Device Standard Diagnostic Data

➢ **To display the diagnostic data**

1. From the **ToolboxST** application, open the **Component Editor**.
2. From the **Hardware Tree View**, select the PPRF module.
3. Expand the **Tree View** of the attached Slave devices and select an attached Slave.
4. Select the **Standard Diagnostics** tab.

The Byte and Bit information in the following table represents the first six bytes of information passed between the Master and Slave.

Byte	Bit	Name	Description	Detail
0	0	Station_Non_Existent	Station not present	Master cannot reach the Slave. If this bit is set to True, the diagnostic bits contain the state of the previous diagnostic message. The Slave sets this bit to False.
	1	Station_Not_Ready	Station not ready	The Slave sets this bit to True if it is not ready for data transfer
	2	Cfg_Fault	Configuration fault	The Slave sets this bit to True if the configuration sent by the Master does not match its own.
	3	Ext_Diag	Extended diagnostic	The Slave sets this bit to True if new diagnostic information is available. A new fault or the clearing of faults may cause this bit to be set to True.
	4	Not_Supported	Not supported	The Slave sets this bit to True if it receives a request for a function that it does not support.
	5	Invalid_Slave_Response	Invalid response	The Master sets this bit to True if it receives an inconsistent response from the Slave. The Slave sets this bit to False.
	6	Prm_Fault	Parameter fault	The Slave sets this bit to True if the last parameter frame was faulty (wrong length, ID, or parameters).
	7	Master_Lock	Master lock	The Master sets this bit to True if the address in byte 4 is not its own address, indicating the Slave has been parameterized by another Master. The Slave sets this bit to False.
1	0	Prm_Req	Parameters required	The Slave sets this bit to True if it needs to be reparameterized and reconfigured. The bit stays set until parameterization is finished.
	1	Stat_Diag	Static diagnostics	The Slave sets this bit to True if it wants the Master to request diagnostics. For example, the Slave would set this bit if it is not able to provide valid user data. The Master should continue to request diagnostic data until the Slave resets this bit to False.
	2		Reserved	
	3	WD_On	Watchdog on	If the Slave sets this bit to True, it indicates that the Watchdog Control in the Slave has been activated.
	4	Freeze_Mode	Freeze mode	The Slave sets this bit to True when it receives the Freeze command.
	5	Sync_Mode	Sync mode	The Slave sets this bit to True when it receives a Sync command.
	6		Reserved	
	7	Deactivated	Deactivated	The Master sets this bit to True if the Slave has been marked inactive by the Send Parameter command.

Byte	Bit	Name	Description	Detail
2	0-6		Reserved	
	7	Ext_Diag_Overflow	Diagnostic Overflow	The Slave sets this bit to True if it receives more module diagnostics data than it can accommodate.
3		Master_Add	Master Address	The address of the Master that parameterized the Slave. If no Master has parameterized the device, the Slave sets this byte to 255 decimal.
4–5		Ident_Number	ID Number	This is the manufacturers PROFIBUS ID Number displayed in decimal format.
		Station_Diagnostic	Device Diagnostic(s) Present	Station Diagnostic is True if there are any diagnostics on the Slave.

In addition, located on the **Standard Diagnostic** tab is the *Station_Diagnostic* variable. It is a *manufactured* Boolean that uses the Slave's configuration to determine its health. If the Slave is present in the system and has any diagnostics present, this bit is set to *TRUE*. Otherwise, it is set to *FALSE*. The Boolean uses the PROFIBUS diagnostic bytes, which are displayed from *PPRF | Troubleshoot | Advanced Diagnostics | PPRF Commands |PROFIBUS Diagnostics*.

12.1.6 Configuration

12.1.6.1 Parameters and Online Loads

I/O pack parameters can be changed online without restarting the system. PPRF parameters also consist of I/O transfer scaling values, which are configured when Boolean input event detection is enabled or not for given points. The PPRF is also used to change point data type conversion and the addition and removal of variables attached to points through online loads. A system restart is not required as long as the ToolboxST application *Compress Variables* command is not run, which would rearrange the EGD exchange.

Parameter	Description	Choices
ProfiClearMode	When set to *False*, all PROFIBUS communication is stopped when the PPRF loses IONet communication. When set to *True* , the PROFIBUS slave devices are set to CLEAR mode if they support it. This parameter allows the user to disable CLEAR mode when the PPRF module loses IONet communication. CLEAR mode is a fail-safe operating condition supported by some DP-V1 slave devices. If a PROFIBUS slave device doesn't support CLEAR mode, its behavior may be unpredictable if CLEAR mode is used. Disabling CLEAR mode is equivalent to unplugging the PPRF from the PROFIBUS network when IONet communication is lost. Consult the manual for specific PROFIBUS slave devices to determine if they support CLEAR mode. This is a new parameter for firmware V04.05; however the behavior in PPRF firmware prior to V04.05 is as though ProfiClearMode is set to *True*.	False, True Default is *False*
SetDiagOnExtDiag	When set to *True*, the PROFIBUS Diagnostic Presence variable and Alarm 44 will be generated when an Extended Diagnostic is present on any device. When set to False, it will prevent the PROFIBUS Diagnostic Presence variable and Alarm 44 from being annunciated when an Extended Diagnostic is available. This parameter allows the user to specify which devices they will monitor by connecting variables to the Standard Diagnostics tab on the devices they want to monitor. This is a new parameter for firmware V05.00; however the behavior in PPRF firmware prior to V05.00 is as though SetDiagOnExtDiag is set to *True*.	False, True Default is *True*

12.1.6.2 PROFIBUS Network Configuration

Before a PROFIBUS device can communicate to the PPRF, it must be added to the PROFIBUS network and configured. These configuration activities are performed using the ToolboxST application and are based on using the standardized General Station Description or *.GSD files (these files can take the form of **.gse*, **.gsf*, **.gsg*, **.gsi*, and/or **.gss*) provided by the PROFIBUS equipment suppliers. These GSD files are read by the ToolboxST application to provide detailed information on the active PROFIBUS devices. From the ToolboxST application, the GSD Manager is used to associate the *.GSD files with Mark VIe control devices.

The watchdog timer is used to enable a Slave to detect bus inactivity. The watchdog timer is reset every time an error free message is received. If no valid message is received within the specified time then the Slave assumes a communication error and sets its outputs to the failed state. Vendor's Slave device GSD file is available for download from the GSD Library located on the website of the PROFIBUS Trade Organization at *www.profibus.com*.

12.2 PPRF Specific Alarms

The following alarms are specific to the PPRF I/O pack.

32

Description Configuration Incompatible: Old - [ ]; New - [ ]

Possible Cause An online load was attempted on a configuration change that requires a reboot.

Solution Rebuild and download the firmware and configuration to the I/O pack.

35

Description PROFIBUS module upgrade failure

Possible Cause A malfunction occurred when a new PROFIBUS module firmware file was being loaded to the PROFIBUS module.

Solution

- Rebuild and download the firmware to the PPRF.
- If the problem persists, replace the I/O pack.

36

Description PROFIBUS module access failure - Unable to download configuration.

Possible Cause A malfunction occurred when a new PROFIBUS configuration was being loaded to the PROFIBUS module.

Solution

- Rebuild and download the firmware to the PPRF.
- If the problem persists, replace the I/O pack.

37

Description Bad configuration loaded to PROFIBUS module

Possible Cause Invalid PROFIBUS configuration files were downloaded to the PROFIBUS module. This causes the PROFIBUS module to not reach the RUN status, which is generally reached when a valid configuration has been processed.

Solution

- Rebuild and download the firmware to the PPRF.
- If the problem persists, replace the I/O pack.

38

Description Unable to communicate with PROFIBUS module

Possible Cause The PROFIBUS host watchdog (a heartbeat between the pack processor and PROFIBUS module) could not be activated.

Solution

- Rebuild and download the firmware to the PPRF.
- If the problem persists, replace the I/O pack.

39

Description PROFIBUS module failure

Possible Cause From the PPRF firmware perspective, the PROFIBUS watchdog timed out (indicating failure of the PROFIBUS firmware).

Solution

- Rebuild and download the firmware to the PPRF.
- If the problem persists, replace the I/O pack.

40

Description PROFIBUS module failure - Module shutdown

Possible Cause The PROFIBUS module has shut down, indicated by a loss of READY/RUN. PROFIBUS READY indicates that the firmware is running, and RUN indicates that a valid configuration has been processed. Loss of READY/ RUN implies that the PROFIBUS module has shut down.

Solution

- Cycle power on the pack.
- If the problem persists, replace the I/O pack.

41

Description PROFIBUS module unable to become active master

Possible Cause This is applicable to redundant configurations only. On startup, a malfunction occurred in making the PPRF the active PROFIBUS master.

Solution

- Rebuild and download the firmware to the PPRF.
- If the problem persists, replace the I/O pack.

42

Description PROFIBUS module unable to become backup master

Possible Cause This is applicable to redundant configurations only. On startup, a malfunction occurred in making the PPRF the backup PROFIBUS master.

Solution

- Rebuild and download the firmware to the PPRF.
- If the problem persists, replace the I/O pack.

43

Description Unable to obtain diagnostic indication from PROFIBUS module

Possible Cause The PROFIBUS module may have failed.

Solution

- Rebuild and download the firmware to the PPRF.
- If the problem persists, replace the I/O pack.

44

Description PROFIBUS diagnostic present

Possible Cause A PROFIBUS diagnostic has been received from a slave device.

Solution

- Refer to the Advanced Diagnostics tool within the ToolboxST application to determine the cause of the diagnostic.
- Identify which slave device is generating the diagnostic.
- Determine and resolve the issue with the slave device. Refer to the slave device documentation.

45

Description Error obtaining PROFIBUS diagnostic

Possible Cause A malfunction occurred while obtaining a PROFIBUS diagnostic message from the PROFIBUS module.

Solution

- Rebuild and download firmware to the PPRF.
- If the problem persists, replace the I/O pack.

46

Description Error interpreting PROFIBUS diagnostic message

Possible Cause

- A malformed PROFIBUS diagnostic was received from the PROFIBUS module.
- Extended diagnostic lengths in the device are incorrectly configured to be longer than 100 bytes.
- The PROFIBUS network has been incorrectly configured.

Solution

- Configure the extended diagnostic length in the device to be shorter than 100 bytes.
- Verify that the PROFIBUS network is configured correctly.
- Rebuild and download the firmware to the PPRF.
- If the problem persists, replace the I/O pack.

47

Description Firmware mismatch in redundant PPRF packs

Possible Cause This is applicable to redundant configurations only. The firmware version of one of the redundant PPRF I/O packs does not match that of the other I/O pack.

Solution

- Verify that both packs are powered and sending data to the controller.
- Download the firmware and configuration to the I/O packs.
- Replace the faulty Ethernet cable from the pack to the IONet network switch.
- Replace the I/O pack.
- If the network switch is faulty, place the pack's Ethernet cable into an empty switch port. If the problem persists, replace the network switch.

48

Description Redundant PPRF pack initialization error

Possible Cause A redundant PPRF I/O pack is not receiving peer-to-peer communications from the other redundant I/O pack. The redundant PPRF I/O packs will not go online unless peer-to-peer communication is healthy.

Solution

- Verify that both packs are powered.
- Download the firmware and configuration to the I/O packs.
- Replace the faulty Ethernet cable from the pack to the IONet network switch.
- Replace the I/O pack.
- If the network switch is faulty, place the pack's Ethernet cable into an empty switch port. If the problem persists, replace the network switch.

49

Description Redundant PPRF pack peer-to-peer communication timeout

Possible Cause A redundant PPRF I/O pack is not receiving peer-to-peer communications from the other redundant I/O pack.

Solution

- Verify that both packs are powered and sending data to the controller.
- Download the firmware and configuration to the I/O packs.
- Replace the faulty Ethernet cable from the pack to the IONet network switch.
- Replace the I/O pack.
- If the network switch is faulty, place the pack's Ethernet cable into an empty switch port. If the problem persists, replace the network switch.

50

Description Active master PPRF PROFIBUS communication failure

Possible Cause This is applicable in redundant configurations only. The master PPRF lost communications with the PROFIBUS network.

- The PROFIBUS cable(s) may be faulty.
- The terminating resistors on the PROFIBUS cable(s) may be configured incorrectly.
- There may be a hardware failure.

Solution

- Verify that the PROFIBUS cables are connected securely.
- Verify that the terminator resistor is configured correctly for the PROFIBUS network. The terminating resistors must be set at the PPRF pack and at the END of the PROFIBUS network only.
- Replace the PROFIBUS network cable.
- Replace the I/O pack.

51

Description Backup master PPRF PROFIBUS communication failure

Possible Cause This is applicable in redundant configurations only. The master PPRF lost communications with the PROFIBUS network.

- The PROFIBUS cable(s) may be faulty.
- The terminating resistors on the PROFIBUS cable(s) may be configured incorrectly.
- There may be a hardware failure.

Solution

- Verify that the PROFIBUS cables are connected securely.
- Verify that the terminator resistor is configured correctly for the PROFIBUS network. The terminating resistors must be set at the PPRF pack and at the END of the PROFIBUS network only.
- Replace the PROFIBUS network cable.
- Replace the I/O pack.

52

Description Invalid PROFIBUS module firmware detected

Possible Cause The PROFIBUS module firmware does not match the hardware.

Solution

- Rebuild and download the firmware to the PPRF.
- If the problem persists, replace the I/O pack.

53

Description 10 millisecond frame periods are not supported

Possible Cause 10 millisecond frame periods are unsupported with PPRFH1A.

Solution

- With PPRFH1A, adjust the frame period to be greater than or equal to 20† milliseconds.
- For 10 millisecond frame periods, replace PPRFH1A with PPRFH1B.

Caution

† The PPRFH1A can be configured for 20 ms frame period, but this is not recommended for new applications. It is the responsibility of the application engineer to qualify fitness for use at 20 ms.

54

Description Backup master PPRF cannot communicate with active master.

Possible Cause This is applicable in redundant configurations only. The backup PPRF cannot communicate with the active master on the PROFIBUS network.

- Incorrect software configuration
- The PROFIBUS cable(s) may be faulty.
- The terminating resistors on the PROFIBUS cable(s) may be configured incorrectly.
- There may be a hardware failure.

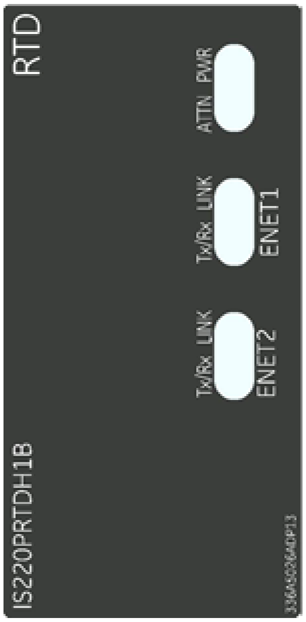
Solution

- From the ToolboxST application, modify the baud rate, then redownload the configuration.
- Verify that the PROFIBUS cables are connected securely.
- Verify that the terminator resistor is configured correctly for the PROFIBUS network. The terminating resistors must be set at the PPRF I/O pack and at the end of the PROFIBUS network only.
- Replace the PROFIBUS network cable.
- Replace the I/O pack.

Notes

13 PRTD Input Module

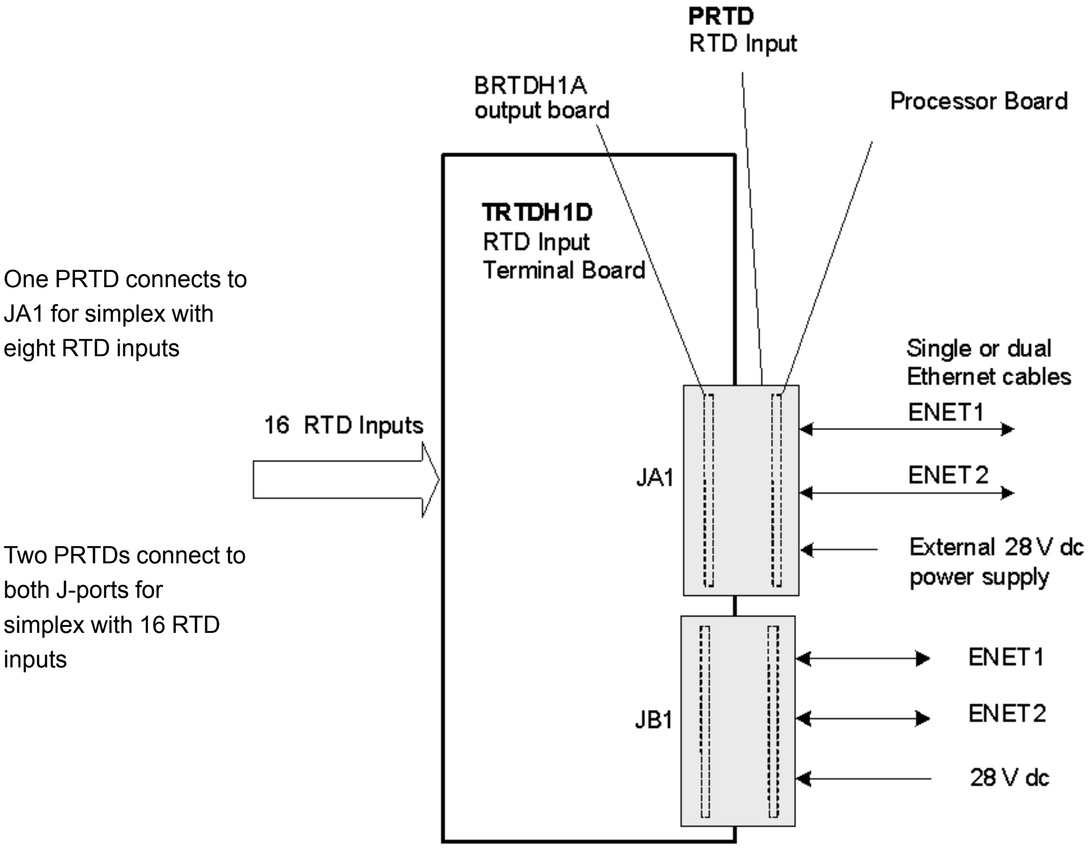
13.1 PRTD Resistance Temperature Device (RTD) Input Pack



The Resistance Temperature Device Input pack (PRTD) provides the electrical interface between one or two I/O Ethernet networks and a RTD input terminal board. The PRTD contains a processor board common to the distributed I/O packs and an acquisition board specific to the RTD input function. The PRTD I/O pack is capable of handling up to eight RTD inputs. Two PRTD packs may be plugged into a single TRTD board to handle 16 simplex inputs.

The PRTD supports only simplex operation.

Input to the I/O pack is through a DC-37 pin connector that connects directly with the associated terminal board connector, and a three-pin power input. Output is through dual RJ-45 Ethernet connectors. Visual diagnostics are provided through indicator LEDs.


PRTD
RTD Input
BRTDH1A
output board
Processor Board
TRTDH1D
RTD Input
Terminal Board
One PRTD connects to JA1 for simplex with eight RTD inputs
16 RTD Inputs
Two PRTDs connect to both J-ports for simplex with 16 RTD inputs
Single or dual Ethernet cables
ENET1
ENET2
JA1
External 28 V dc power supply
ENET1
ENET2
JB1
28 V dc

13.1.1 Compatibility

The PRTD I/O pack includes one of the following compatible BPPx processor boards:

- The PRTDH1A contain a BPPB processor board.
- The PRTDH1B contains a functionally compatible BPPC that is supported in the ControlST* software suite V04.06 and later.

The PRTD pack is compatible with the RTD input terminal boards TRTDH1D, TRTDH2D, and SRTD. Simplex redundancy is only supported.

Terminal Board	# of RTD inputs	# of I/O packs	J-port	Redundancy
† TRTDH1D/ H2D	8	one	JA1	Simplex
	16	two	JA1 and JA2	
SRTD	8	one	JA1	
† The PRTD provides galvanic isolation of the RTD input circuit. This requires changes in the terminal board transient protection, provided on the TRTDH1D and TRTDH2D boards. The TRTDH1D terminal board provides filtering compatible with the standard scan rate of PRTD. The TRTDH2D version of the terminal board provides less filtering to allow proper performance when the fast scan rate of PRTD is selected. Earlier versions of the TRTD board are not supported by the PRTD, although no physical damage will occur.				

13.1.2 Installation

➢ **To install the PRTD I/O pack**

1. Securely mount the desired terminal board.
2. Directly plug one or two PRTD (for simplex control of eight or 16 RTDs) into the terminal board connectors.
3. Mechanically secure the I/O pack using the threaded inserts adjacent to the Ethernet ports. The inserts connect with a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right angle force applied to the DC-37 pin connector between the I/O pack and the terminal board. The adjustment should only be required once in the service life of the product.

Note The PRTD mounts directly to a terminal board. TRTDH#D has two DC-37 pin connectors that receive the PRTDs, one for each set of 8 RTD inputs.

4. Plug in one or two cables (depending on system configuration) to negotiate proper operation over either port. If dual connections are used the standard practice is to hook ENET1 to the network associated with the R controller.
5. Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to remove power from the cable before plugging it in because the I/O pack has inherent soft-start capability that controls current inrush on power application.
6. Use the ToolboxST* application to configure the I/O pack as necessary. From the Component Editor, press F1 for help.

13.1.2.1 Connectors

The I/O pack contains the following connectors:

- A DC-37 pin connector on the underside of the I/O pack connects directly to the terminal board. The connector contains the signals for 8 RTD inputs and the ID signal.
- ENET1 is an RJ-45 Ethernet connector. It is located on the side of the pack and is the primary system interface.
- ENET2 is a second RJ-45 Ethernet connector also on the side of the pack. It is the redundant or secondary system interface.
- A 3-pin power connector on the side of the I/O pack is for 28 V dc power for the I/O pack and terminal board.

13.1.3 Operation

The following features are common to the distributed I/O modules:

- *BPPx Processor*
- *Processor LEDs*
- *Power Management*
- *ID Line*
- *I/O Module Common Diagnostic Alarms*

13.1.3.1 Analog Input Hardware

The PRTD input board accepts eight three-wire RTD inputs from the RTD terminal board.

The pack supplies a 10 mA dc multiplexed (not continuous) excitation current to each RTD, which can be grounded or ungrounded. The eight RTDs can be located up to 300 meters (984 feet) from the distributed I/O cabinet with a maximum two-way cable resistance of 15 Ω.

The A/D converter in the pack samples each signal and the excitation current four times per second for normal mode scanning, and 25 times per second for fast mode scanning, using a time sample interval related to the power system frequency. Linearization for the selection of RTD types is performed in software by the processor. RTD open and short circuits are detected by out of range values. An RTD, which is determined to be out of hardware limits, is removed from the scanned inputs to prevent adverse effects on other input channels. Repaired channels are reinstated automatically in 20 seconds, or can be manually reinstated.

13.1.3.2 Calibration

RTD inputs are automatically calibrated using the filtered calibration source and null voltages.

13.1.4 Specifications

Item	PRTD Specification		
Number of Channels	8 channels per pack		
RTD Types	100 and 200 Ω platinum 10 Ω copper 120 Ω nickel		
Span	0.3532 to 4.054 V		
A/D Converter Resolution	14-bit resolution		
Scan Time	Normal scan 250 ms (4 Hz) to provide 50 and 60 Hz noise rejection where each RTD is sensed for 22 ms at 4 times a second.		
	Fast scan 40 ms (25 Hz) for special airflow measurements with each RTD sensed for 4 ms at 25 times per second. This mode provides faster response sacrificing the 50 and 60 Hz rejection.		
Temperature Measurement Accuracy	**RTD Type**	**Group Gain**	**Accuracy at 204 °C (400 °F)**
	120 Ω Nickel	Normal_ 1_0	1.1°C (2 °F)
	200 Ω Platinum	Normal_ 1_0	1.1°C (2 °F)
	100 Ω Platinum	Normal_ 1_0	2.22°C (4 °F)
	100 Ω Platinum -51 to 204ºC (-60 to 400 °F)	Gain_2_0	1.11°C (2 °F)
	10 Ω Copper	10ohmCU_10_0	5.55°C (10 °F)

Item	PRTD Specification
Ohms Measurement Accuracy	For slow RTDs (4 Hz) 0.1 % of full scale including full scale ranges of: • For a Gain = Normal_ 1_0, 0.4 ohms, (where full scale is 400 Ω) • For a Gain = Gain_2_0, 0.2 ohms, (where full scale is 200 Ω) • For a Gain = 10ohmCU_10_0, 0.04 ohms, (where full scale is 40 Ω) For fast RTDs (25 Hz) 0.15 % of full scale
Common Mode Rejection	Ac common mode rejection 60 dB at 50/60 Hz, Dc common mode rejection 80 dB
Common Mode Voltage Range	±5 Volts
Normal Mode Rejection	Rejection of up to 250 mV rms is 60 dB at 50/60 Hz system frequency for normal scan
Max Lead Resistance	15 Ω maximum two-way cable resistance
Ambient Rating for Enclosure Design†	PRTDH1B is rated from -40 to 70°C (-40 to 158 °F) PRTDH1A is rated from -30 to 65°C (-22 to 149 °F)

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

13.1.4.1 RTD Types and Ranges

Note The units (°C or °F) are based on the RTD Unit settings. Refer to the section, *Configuration*.

RTD inputs ranging from 7 to 405 Ω are supported over a full-scale input range of 0.069 to 4.054 V due to the 10 mA excitation current. The following table displays the types of RTD used and the temperature ranges.

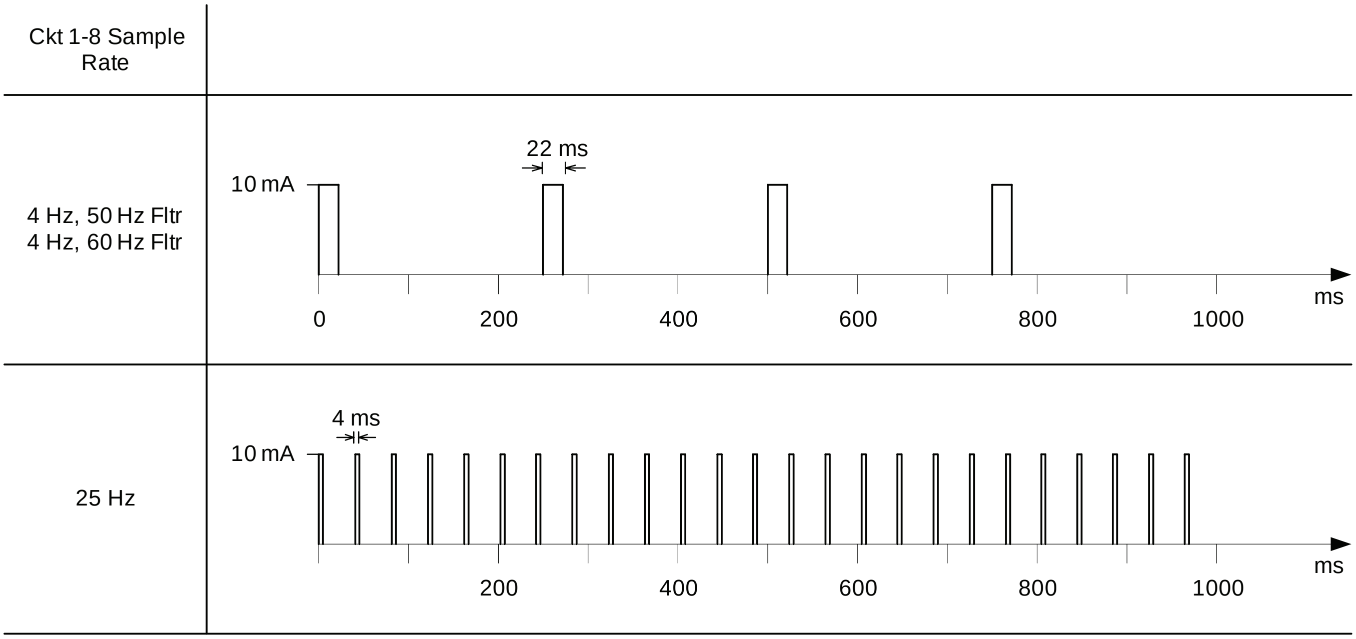
RTD Type	Name/Standard	Range °C	Range °F	Minimum Ω	Maximum Ω
10 Ω copper	MINCO_CA	-51 to 260	-60 to 500	7	19
	CU10				
100 Ω platinum	PT100_SAMA 100	-51 to 593	-60 to 1100	78	310
	MINCO_PIA	-158 to 880	-252 to 1616	35	405
	MINCO_PD	-51 to 700	-60 to 1292	80	345
	PT100_DIN				
	MINCO_PA	-51 to 630	-60 to 1166	80	327
	PT100_PURE				
	MINCO_PB				
	PT100_USIND				
120 Ω nickel	MINCO_NA	-51 to 249	-60 to 480	86	365
	N 120				
200 Ω platinum	PT 200	-51 to 204	-60 to 400	159	358
	MINCO_PK	-51 to 266	-60 to 511	159	404

13.1.4.2 RTD Excitation Signal

The excitation signal to the RTD sensors is a 10 mA pulse, driven by circuitry operating on ± 15 V isolated DC supplies. The terminals to the RTD each have a bipolar 15 V clamp diode and 0.001 ufd filter capacitor. The current and voltage levels are within the IEC60079-11 guidelines for class IIC gasses. The duration and periodicity of the pulses vary with the settings for the I/O pack as follows:

- 4 Hz settings for 50 or 60 Hz rejection uses a 22 millisecond long pulse every 250 milliseconds
- 25 Hz fast setting uses a 4 millisecond long pulse every 40 milliseconds

PRTD Current Wave Form & RMS Values



RMS Current (for rectangular pulse wave) = a * $\sqrt{(D)}$
a = amplitude of wave
D = Duty cycle of wave

4 Hz (RMS Current)= 10 mA * $\sqrt{(22/250)}$ = 2.97 mA

25 Hz (RMS Current)= 10 mA * $\sqrt{(4/40)}$ = 3.16 mA

13.1.5 Diagnostics

The I/O pack performs the following self-diagnostic tests

- A power-up self-test that includes checks of RAM, Flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set
- Each RTD type has hardware limit checking based on preset (non-configurable) high and low levels set near the ends of the operating range. If this limit is exceeded, a logic signal is set, and the input is no longer scanned. If any one of the 8 input’s hardware limits is set it creates a composite diagnostic alarm, L3DIAG_PRTD, referring to the entire board.
- Each RTD input has system limit checking based on configurable high and low levels. These limits can be used in application code to generate process alarms, and can be configured for enable/disable, and as latching/non-latching. RESET_SYS resets latched system limit signals that are no longer out of limits.

13.1.6 PRTD ToolboxST Configuration

13.1.6.1 Parameters

Parameter	Description	Choices
SystemLimits	Allows user to temporarily disable all system limit checks for testing purposes. Setting this parameter to Disable will cause a diagnostic alarm to occur.	Enable (default), disable
AutoReset	Automatic restoring of RTDs removed from scan	Enable (default), disable
GroupRate	RTD's 1-8 sample rate and n+ system frequency filter if 4 Hz sampling	4 Hz, 50 Hz filter 4 Hz, 60 Hz filter (default) 25 Hz

13.1.6.2 Inputs

Item	Description	Choices
RTDType	Select RTD type or ohms input RTDs linearizations supported by firmware, (unused inputs are removed from scanning)	Unused (default), CU10, MINCO_CA, PT100_DIN, MINCO_PD, PT100_PURE, MINCO_PA, PT100_USIND, MINCO_PB, N120, MINCO_NA, MINCO_PIA, PT100_SAMA, PT200, MINCO_PK, Ohms
SysLim1Enabl	Enable system limit 1 fault check Enables or disables a temperature limit for each RTD, can be used to create an alarm	Enable, disable (default)
SysLim1Latch	Latch system limit 1 fault Determines whether the limit condition will latch or unlatch for each RTD; reset used to unlatch.	Latch (default), unlatch
SysLim1Type	System limit 1 check type (≥ or ≤) Limit occurs when the temperature is greater than or equal (≥), or less than or equal to a preset value.	≥ (default), ≤
SysLimit1	System limit 1 - Deg °F or Deg °C. Enter the desired value of the limit temperature	-60 to 1300 (default)
SysLim2Enabl	Enable system limit 2 fault check Enables or disables a temperature limit used to create an alarm	Enable, disable (default)
SysLim2Latch	Latch system limit 2 fault Determines whether the limit condition will latch or unlatch; reset used to unlatch.	Latch (default), unlatch
SysLim2Type	System limit 2 check type (≥ or ≤). Limit occurs when the temperature is greater than or equal (≥), or less than or equal to a preset value.	≥ ≤ (default)
SysLimit2	System limit 2 - Deg °F or ohms. Enter the desired value of the limit temperature, Deg °F or ohms	-60 to 1,300 (default)
RTDGain	Select RTD sensor gain. Gain 2.0 is for higher accuracy if ohms <190.	Normal_1_0 (default) Gain_2_0 10ohmCu_10_0

Item	Description	Choices
RTDUnit	Temperature units in degree Celsius or degree Fahrenheit for any selected Rtd Type except Ohms and Unused. If RtdType is Ohms, this parameter does not apply. This parameter affects the native units of the controller application variable. It is only indirectly related to the tray icon and associated unit switching capability of the HMI. This parameter should not be used to switch the display units of the HMI.	deg_F (default) deg_C
	Caution **Do not change the RtdUnit parameter in the ToolboxST application because these changes will require corresponding changes to application code and to the Format Specification or units of the connected variable. This parameter modifies the actual value sent to the controller as seen by application code. Application code that is written to expect degrees Fahrenheit will not work correctly if this setting is changed. External devices, such as HMIs and Historians, may also be affected by changes to this parameter.**	

13.1.6.3 Variables

Variable	Description-Point Edit (Enter Signal Connection)	Direction	Type
L3DIAG_PRTD_R	I/O diagnostic indication	Input	BIT
LINK_OK_PRTD_R	I/O link okay indication	Input	BIT
ATTN_PRTD_R	I/O attention indication	Input	BIT
IOPackTmpr_R	I/O pack temperature	Input	FLOAT
SysLim1RTD1_R	System limit 1	Input	BIT
↓	↓	Input	BIT
SysLim1RTD8_R	System limit 1	Input	BIT
SysLim2RTD1_R	System limit 2	Input	BIT
↓	↓	Input	BIT
SysLim2RTD8_R	System limit 2	Input	BIT
PS18V_PRTD_R	I/O 18 V Power Supply Indication	Input	Bool
PS28V_PRTD_R	I/O 28 V Power Supply Indication	Input	Bool

13.2 PRTD Specific Alarms

The following alarms are specific to the PRTD I/O pack.

32-39

Description RTD [ ] Voltage out of range - Raw Counts [ ]

Possible Cause

- There is a break in the RTD wiring/cabling or high impedance is blocking the signal.
- There is a break in the connections to the terminal board.
- The RTD device has failed.
- Internal PRTD hardware problem.

Solution

- Check the field wiring for an open circuit or high impedance.
- Verify the proper connections to the terminal board.
- Check the RTD for proper operation.
- Replace the I/O pack.

64-71

Description RTD [ ] Current out of range - Raw Counts [ ]

Possible Cause

- RTD wiring, cabling, or sensor issues
- There is a break in the connections to the terminal board.
- The current source on the PRTD has failed.
- The measurement device has failed.

Solution

- Check the field wiring for an open circuit or high impedance.
- Check for loose and/or corroded junction points.
- Check for a damaged sensor.
- Verify the proper connections to the terminal board.
- Replace the I/O pack.

96-103

Description RTD [ ] Resistance out of range ([ ] Ohms)

Possible Cause

- The wrong type of RTD has been configured or selected by default.
- High-resistance values were created by high voltage and/or low current.

Solution

- Verify that the RTD-type configuration matches the attached device type.
- Check the field wiring for high impedance.

128

Description Internal reference out of range - Voltage circuit

Possible Cause The internal PRTD hardware checks have failed.

Solution Replace the I/O pack.

144

Description Internal reference out of range - Current circuit

Possible Cause The internal PRTD hardware checks have failed.

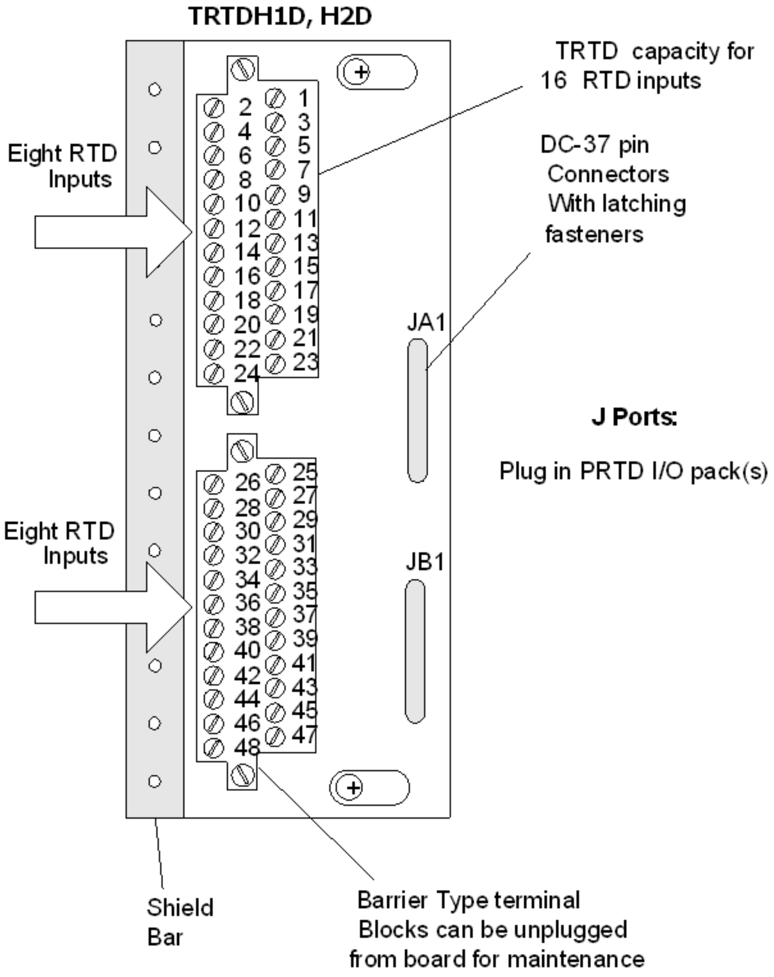
Solution Replace the I/O pack.

13.3 TRTD 16 RTD Inputs

The RTD Input (TRTD) terminal board accepts 16, three-wire RTD inputs when the I/O packs are placed on both J-ports. These inputs are wired to two barrier type terminal blocks. The inputs have noise suppression circuitry to protect against surge and high frequency noise. TRTD communicates with the PRTDs, which convert the inputs to digital temperature values and transfer them to the Mark VIe controller.

13.3.1 Compatibility

In the Mark VIe control system, TRTDH1D and TRTDH2D work with the PRTD I/O pack and support simplex applications only. Two PRTD I/O packs plug into the TRTD for a total of 16 inputs.



RTD Input Terminal Boards

The PRTD provides galvanic isolation of the RTD input circuit. This requires changes in the terminal board transient protection, provided on the TRTDH1D and TRTDH2D boards. The TRTDH1D terminal board provides filtering compatible with the standard scan rate of PRTD. The TRTDH2D version of the terminal board provides less filtering to allow proper performance when the fast scan rate of PRTD is selected. TRTD board versions previous to TRTDH#D are not supported by the PRTD, although no physical damage will occur.

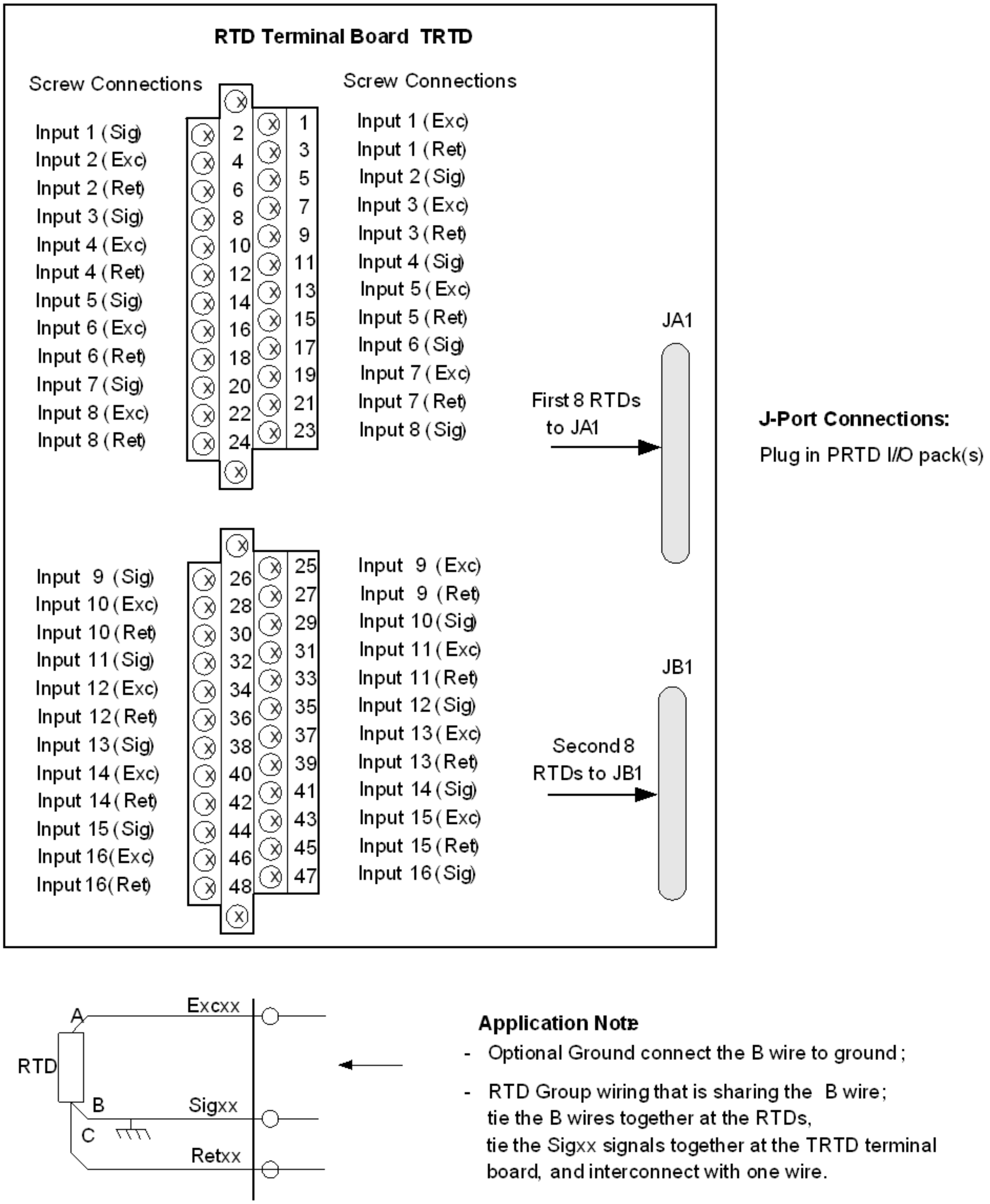
13.3.2 Installation

Note A shield terminal strip attached to chassis ground is located immediately to the left of each terminal block.

Connect the wires for the 16 RTDs directly to the two terminal blocks on the terminal board. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wires.

Caution

Double-shielded wire must be used. All shields must be terminated at the shield terminal strip. Do not terminate shields located at the end device.



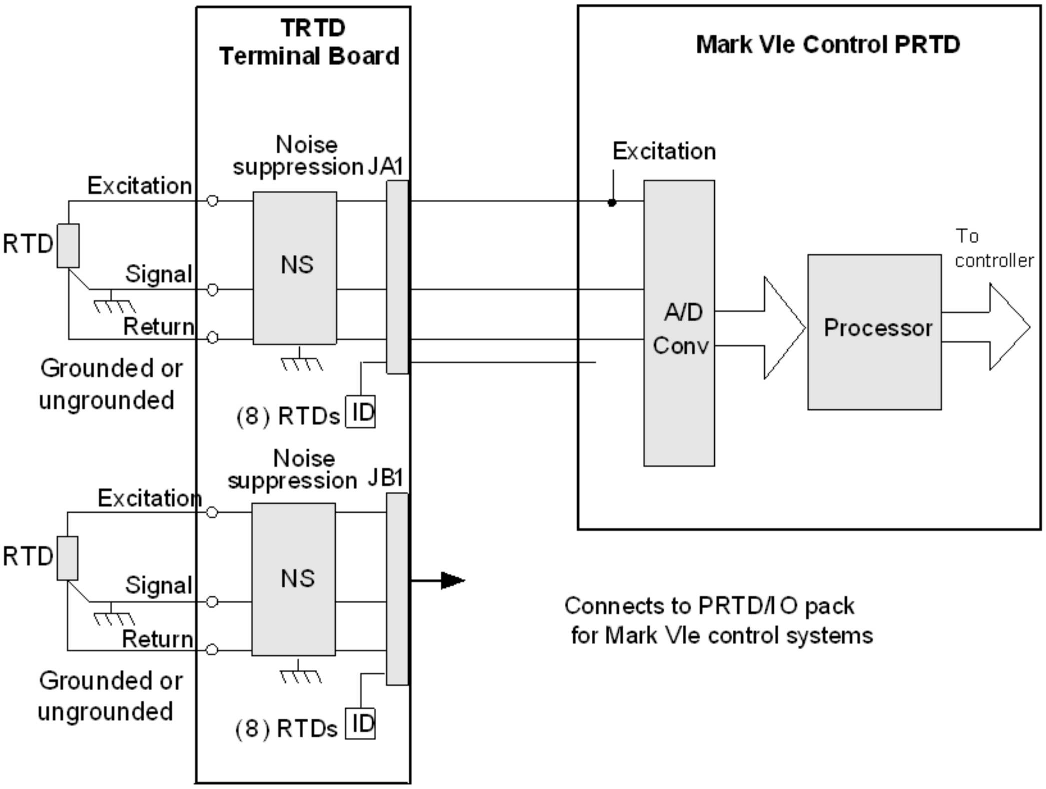
Application Note:

- Optional Ground connect the B wire to ground ;
- RTD Group wiring that is sharing the B wire;
  tie the B wires together at the RTDs,
  tie the Sigxx signals together at the TRTD terminal board, and interconnect with one wire.

TRTD RTD Terminal Board Wiring

13.3.3 Operation

TRTD supplies a 10 mA dc multiplexed (not continuous) excitation current to each RTD, which can be grounded or ungrounded. The 16 RTDs can be located up to 300 m (984 ft) from the control cabinet with a maximum two-way cable resistance of 15 Ω.



TRTD (Simplex) Inputs and Signal Processing

13.3.4 Specifications

Item	TRTD Specification
Number of Channels	Eight channels per terminal board
Size	17.78 cm wide x 33.02 cm high (7 in x 13 in)

13.4 SRTD 8 RTD Input

The Resistance Temperature Device Input (SRTD) terminal board is a compact RTD terminal board, designed for DIN-rail or flat mounting. The board has eight RTD inputs and connects to the PRTD I/O processor. High-density Euro-block type terminal blocks are mounted to the board. An on-board ID chip identifies the board to the I/O processor for system diagnostic purposes.

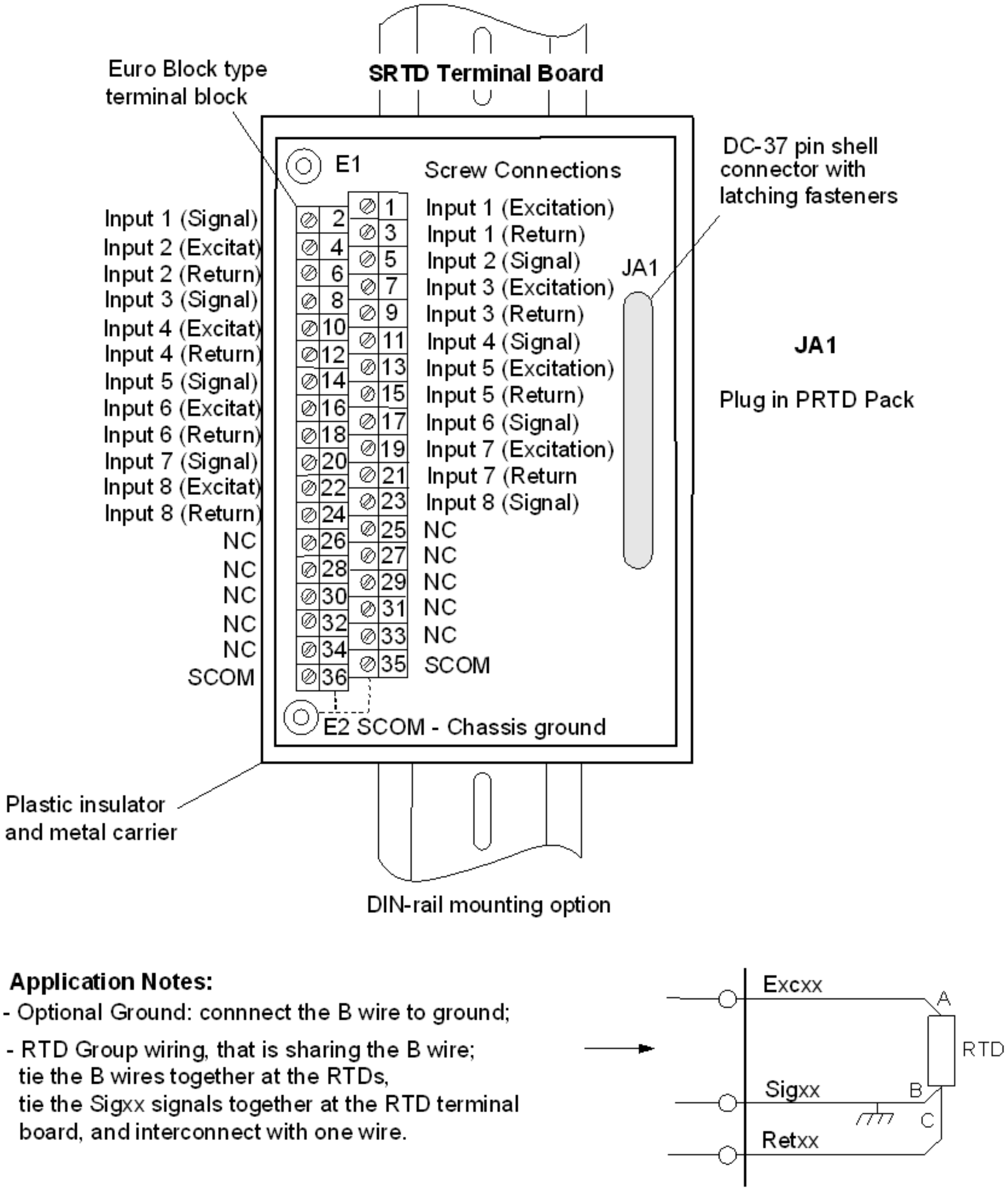
In the Mark* VIe systems, the PRTD I/O pack works with the SRTD. The I/O pack plugs into the DC-37 pin connector and communicates with the controller over Ethernet. Only simplex systems are supported.

13.4.1 Installation

The SRTD and a plastic insulator mount on a sheet metal carrier which mounts on a DIN rail. Optionally the SRTD and insulator mount on a sheet metal assembly that bolts directly to a cabinet. The eight RTDs are wired directly to the Euro style box-type terminal blocks which has 36 terminals and is available in two types. Typically #18 AWG wires (shielded twisted triplet) are used. I/O cable shield terminal uses an external mounting bracket supplied by GE or the customer. Terminals 25 through 34 are not connected. E1 and E2 are mounting holes for the chassis ground screw connection (SCOM).

Caution

Double-shielded wire must be used. All shields must be terminated at the shield terminal strip. Do not terminate shields located at the end device.



Application Notes:

- Optional Ground: connnect the B wire to ground;
- RTD Group wiring, that is sharing the B wire; tie the B wires together at the RTDs, tie the Sigxx signals together at the RTD terminal board, and interconnect with one wire.

SRTD Terminal Board Wiring and Cabling

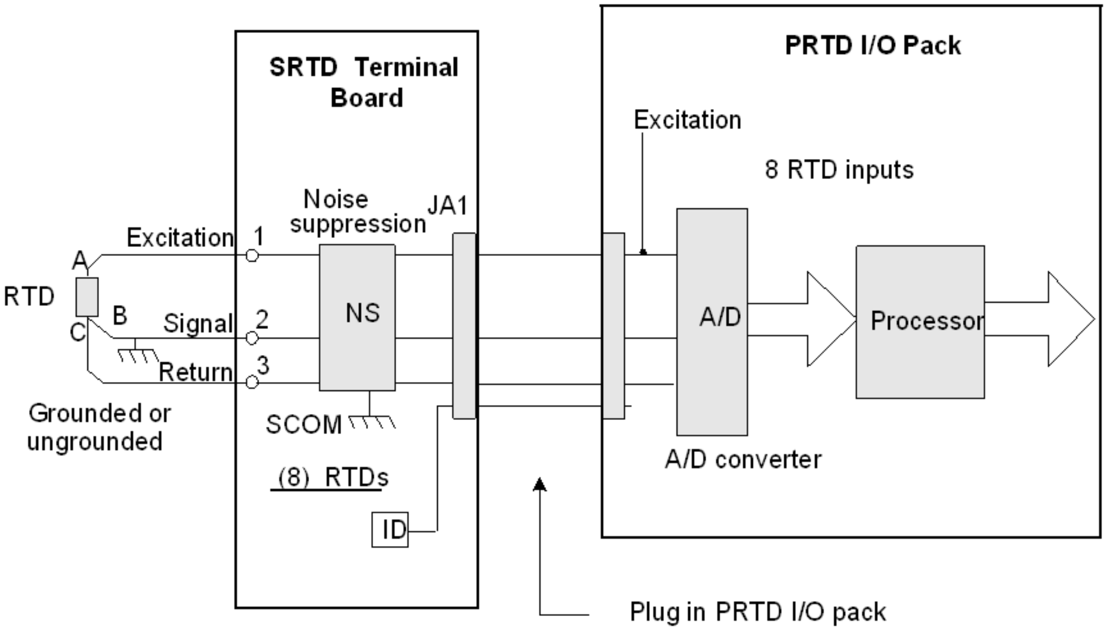
Two types of Euro style box-type terminal blocks are available:

- Terminal board SRTDH1 has a permanently mounted terminal block with 36 terminals.
- Terminal board SRTDH2 has a right-angle header accepting a range of commercially available pluggable terminal blocks, with a total of 36 terminals.

13.4.2 Operation

The terminal board supplies a 10 mA dc multiplexed (not continuous) excitation current to each RTD, which can be grounded or ungrounded. The eight RTDs can be located up to 300 m (984 ft) from the control cabinet with a maximum two-way cable resistance of 15 Ω. The on-board noise suppression is similar to that on the TRTD. The RTD inputs and signal processing are illustrated in the following figure.

The A/D converter in the PRTD I/O pack samples each signal and the excitation current four times per second for normal mode scanning, and 25 times per second for fast mode scanning, using a time sample interval related to the power system frequency. Linearization for the selection of 15 RTD types is performed by the processor.



SRTD Board and Input Processor Board

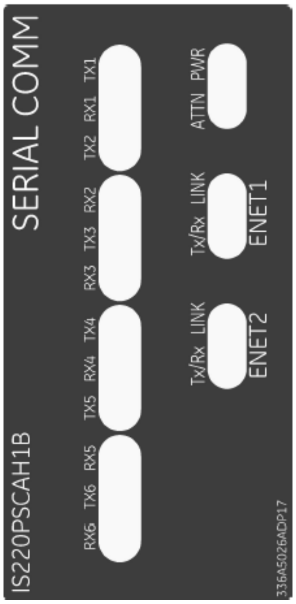
13.4.3 Specifications

Item	SRTD Specification
Number of Channels	Eight channels per terminal board
Size	15.9 cm high x 10.2 cm wide (6.25 in x 4.0 in)

Notes

14 PSCA Serial Communication Module

14.1 PSCA Serial Communication I/O Pack

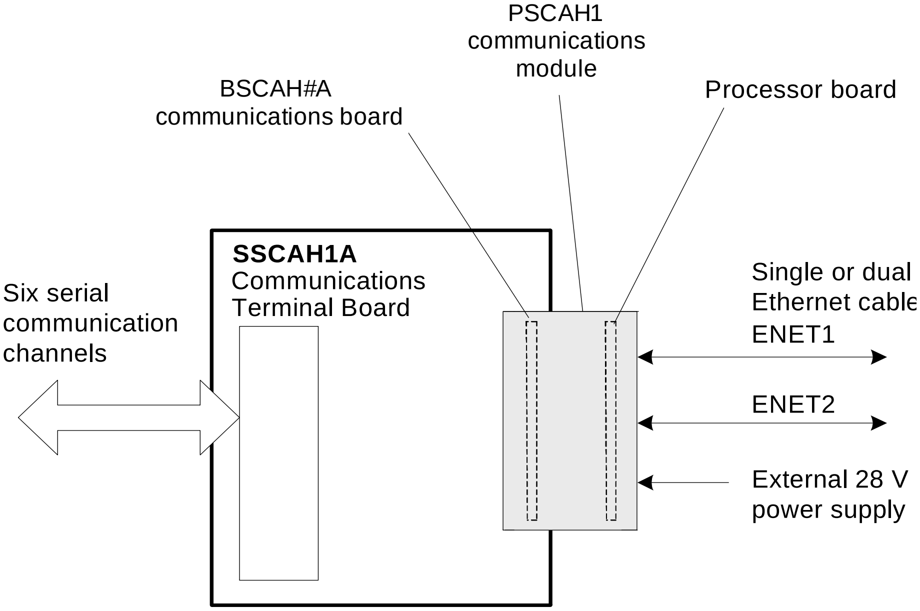


The Serial Communication PSCA I/O pack provides the electrical interface between one or two I/O Ethernet networks and a serial communications terminal board. The I/O pack contains a BPPx processor board common to all Mark* VIe distributed I/O packs and a serial communications board. The communications board contains six serial transceiver channels, each of which can be individually configured to comply with RS-232, RS-422, or RS-485 half-duplex standards.

Input to the I/O pack is through dual RJ-45 Ethernet connectors and a 3-pin power input. Output is through a DC-62 pin connector that connects directly with the associated terminal board connector. One of the Ethernet ports can be used to support Ethernet Modbus communication on Simplex networks. Visual diagnostics are provided through indicator LEDs.

The PSCA I/O pack includes one of the following compatible BPPx processor boards:

- The PSCAH1A contains a BPPB processor board.
- The PSCAH1B contains a functionally compatible BPPC that is supported in ControlST* software suite V04.07 and later.



14.1.1 Installation

➢ **To install the PSCA I/O pack**

1. Securely mount the desired terminal board.
2. Directly plug one PSCA I/O pack into the SSCA terminal board connector.
3. Mechanically secure the I/O packs using the threaded inserts adjacent to the Ethernet ports. The inserts connect with a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right angle force applied to the DC-62 pin connector between the I/O pack and the terminal board. The adjustment should only be required once in the service life of the product.

Note The PSCA mounts directly to a SSCA simplex terminal board, which has a single DC-62 pin connector that receives the PSCA.

4. Plug in one or two Ethernet cables depending on the system configuration. The I/O pack operates over either port. If dual connections are used, standard practice is to hook ENET1 to the network associated with the R controller, however, the PSCA is not sensitive to Ethernet connections and will negotiate proper operation over either port.
5. Apply power to the I/O pack by plugging in the connector on the side of the pack. It is not necessary to remove power from the cable before plugging it in because the I/O pack has inherent soft-start capability that controls current inrush on power application.
6. From the ToolboxST* application, add the PSCA module, and add and configure the required devices. From the Component Editor, press F1 for help.

14.1.2 Operation

The following features are common to the distributed I/O modules:

- *BPPx Processor*
- *Processor LEDs*
- *Power Management*
- *ID Line*
- *I/O Module Common Diagnostic Alarms*

14.1.2.1 Connectors

- The DC 62-pin connector on the underside of the I/O pack connects directly to a discrete output terminal board.
- The RJ-45 Ethernet connector (ENET1) on the I/O pack side is the primary system interface.
- The second RJ-45 Ethernet connector (ENET2) on the I/O pack side is the redundant or secondary system interface.

Note The terminal board provides fused power output from a power source that is applied directly to the terminal board, not through the I/O pack connector.

14.1.2.2 Serial Channels

The PSCA board in the I/O pack contains six independently configurable serial channels. Each of the ports can support the following modes: RS-232, RS422, RS 485 half-duplex. Jumpers on the SSCA terminal board are used to set up the terminal scheme for the selected communication mode. For details on proper wiring and jumper settings for the supported modes, refer to the section, *SSCA Simplex Serial Communication Input/Output*.

14.1.2.3 Dataflow from PSCA to Controller

Dataflow from the PSCA to the Mark VIe controller is of two types: fixed I/O and Modbus I/O. Fixed I/O is associated with the smart pressure transducers and the Kollmorgen® electric drive data. This data is completely processed every frame, the same as conventional I/O. These signals are mapped into signal space, have individual health bits, and have offset/gain scaling. Several of these signals are configured to support system limit checking.

Modbus: Modbus I/O is the I/O associated with the Modbus ports. Because of the quantity of these signals, they are not completely processed every frame; instead they are packaged and transferred to the Mark VIe controller, over the IONet through a special service. This can accommodate up to 2400 bytes, at 4 Hz, or 9600 bytes at 1 Hz, or combinations thereof. This I/O is known as second class I/O, where coherency is at the signal level only, not at the device or board level. Health bits are assigned to individual points in the same fashion as the other protocols, and system limit checking is not performed. Three consecutive time-outs are required before a signal is declared unhealthy. Diagnostic messages are used to annunciate all communication problems. The input value is cleared for a given signal after four consecutive time-outs occur on that signal.

Honeywell® Pressure Transducers: Serial ports 1 and 2 support the Honeywell pressure configuration. It reads inputs from the Honeywell Smart Pressure Transducers, type LG-1237. As an option (pressure transducers or Modbus) this service is available only on ports 1 and 2. The pressure transducer protocol utilizes interface board DS200XDSAG#AC, and RS-422. Each port can service up to six transducers. The service is 375 kbaud, asynchronous, nine data bits, (11 bits including start and stop). It includes communication miss counters, one per device, and associated diagnostics as failsafe features.

After four consecutive misses, it forces the input pressure to 1.0 psi, and posts a diagnostic. After four consecutive hits (good values) it removes the forcing and the diagnostic.

Kollmorgen Electric Drive: Three ports (any three, but no more than three) support the Kollmorgen electric drive. It communicates with a Kollmorgen Electric Fast Drive FD170/8R2-004 at a 19200 baud rate, point-to-point, using RS-422.

14.1.2.4 Serial Modbus Master Service

The current Modbus design supports the Master mode on all six serial ports. It is configurable at the port level as follows:

- Physical connection: RS-232, RS-422, RS-485
- Baud Rate: 300, 600, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200
- Parity: none, odd, even
- Data Bits: seven, eight
- Stop Bits: one, two
- Station addresses
- Multidrop is applicable only to RS-485 with up to eight devices per port; maximum of 18 devices per board
- For RS-232 or RS-422, only one station is supported for these protocols
- RTU
- Time-out (milliseconds) per device
- 32 bit data *Word* ordering (for example, Least Significant Word [LSW] or Most Significant Word [MSW] first)

Note *First* denotes which word is in the lower-numbered register. All 16-bit registers are Big-Endian per standard Modbus convention.

- Device response delay time

The Modbus service is configurable at the signal level as follows:

- Signal type
- Register number
- Read/write
- Transfer rate, 0.5, 1, 2, or 4 Hz
- Scaling: Raw min/max, Eng min/max

The service supports function codes 1-7, 15, and 16; it also supports double 16-bit registers for floating point numbers and 32-bit counters. It periodically (10 sec) attempts to reestablish communications with a dead station.

Type casting and scaling of all I/O signals to/from engineering units are supported on the PSCA and the ToolboxST* application, for both fixed I/O and Modbus I/O.

14.1.2.5 Ethernet Modbus Master Service

The PSCA can use one of its two Ethernet ports to support the Ethernet Modbus Master Protocol. This configuration can only be used with a simplex network. The Ethernet IP address for Modbus can not be included in the range of the IONet submask range. All Ethernet Modbus stations are configured on Port 7 through the ToolboxST application. The Ethernet Modbus implementation follows the Open Modbus/TCP Specification for a Class 1 device.

The ToolboxST application allows up to 18 Ethernet Modbus stations to be attached to the PSCA. The CPU loading for each station varies depending on the number of Modbus registers being requested and the update rate. Also, the field device connect and data response rate may vary. Data throughput should be validated in system test when multiple stations and/or large amounts of data are being transferred.

The following parameters are defined for all stations on the PSCA Ethernet port:

- TCP/IP address for PSCA Ethernet port
- TCP/IP subnet mask
- TCP/IP Gateway IP address of intermediate router (optional)

The following parameters are defined for each field device station:

- Field device TCP/IP address
- Field device TCP/IP port (Modbus default is 502)
- Modbus Station address (optional)
- TCP/IP Read time-out (default is 1s)

Note On initial wait for each Slave device response to a Modbus request, the PSCA will re-try its receive for up to six times for an effective time-out period of *(6 * TimeOut) = Total timeout* before indicating *No Response* and proceeding to the next message. After three *No Responses* have occurred, the connection will be closed, and the PSCA will periodically attempt to re-establish communications.

- 32–bit data *Word* ordering (for example, LSW or MSW first)

Note *First* denotes which word is in the lower-numbered register. All 16-bit registers are Big-Endian per standard Modbus convention.

- Open Modbus/TCP IP protocol

The Modbus service is configured at the signal level as follows:

- Signal type
- Register number
- Read/write
- Transfer rate, 0.5, 1, 2, or 4 Hz
- Scaling: Raw min/max, Eng min/max

The service supports function codes 1-7, 15, and 16. It also supports double 16-bit registers for floating point numbers and 32-bit counters. It periodically (10 sec) attempts to re-establish communications with a dead station.

Type casting and scaling of all I/O signals to/from engineering units are supported on the PSCA and the ToolboxST application, for both fixed I/O and Modbus I/O.

14.1.3 Specifications

Item	PSCA Specification
Channels	Six independently configurable serial channels One Ethernet Modbus Channel (simplex network)
Communication Choices	RS-232 Mode RS-422 Mode RS-485 Mode half-duplex only Ethernet Modbus Mode
RS-232 Mode	Cable distance: 15 m (50 ft) Communication Rate: 115.2 kbps maximum
RS-422 Mode	Cable distance: 305 m (1000 ft) Communication Rate: 375 kbps maximum
RS-485 Mode	Cable distance: 305 m (1000 ft) Communication Rate: 115.2 kbps maximum Number of drops: 8
Size	8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in x 1.65 in x 4.78 in)
Technology	Surface-mount
Ambient Rating for Enclosure Design†	PSCAH1B is rated from -40 to 70ºC (-40 to 158 ºF) PSCAH1A is rated from -30 to 65ºC (-22 to 149 ºF)

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

14.1.4 Diagnostics

The I/O pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set
- Analog inputs such as pressure and position have system limit checking based on configurable high and low levels. These limits can be used to generate alarms, to enable/disable, and as latching/non-latching. RESET_SYS reset the out of limits

Details of the individual diagnostics are available from the ToolboxST application. The diagnostic signals can be individually latched, and then reset with the RESET_DIA signal if they go healthy.

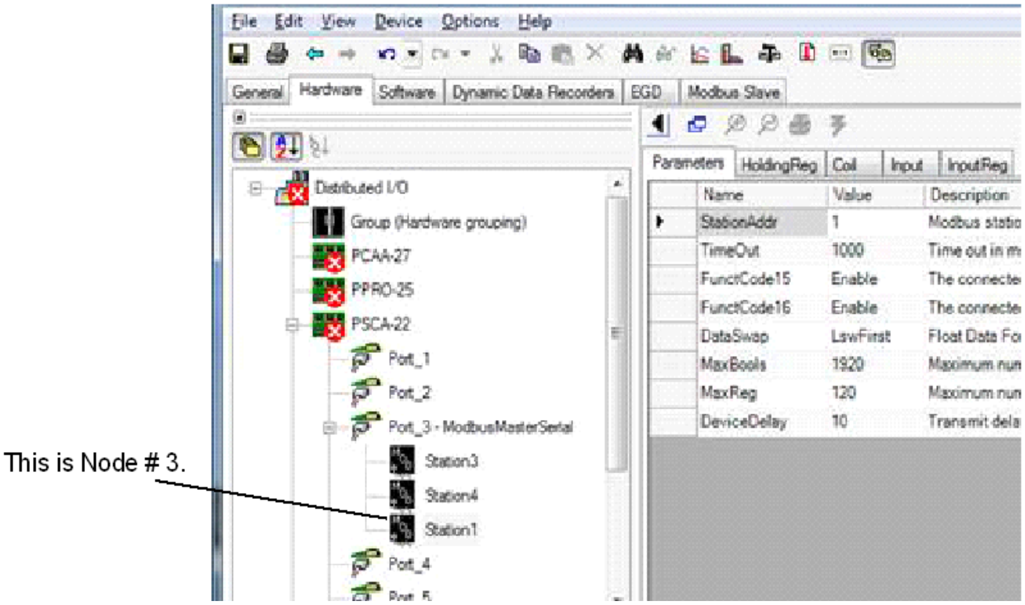
14.2 PSCA Specific Alarms

The following alarms are specific to the PSCA I/O pack.

32-67

Description Comm Port #[ ] Node #[ ] Communication Failure - No Response (see alarm help)

Possible Cause A command was sent to a field device, but no response was received. The Node number refers to the position of the station or device as listed inside the port, as displayed from the Hardware Tab Tree View. The node number is usually the same as the station number, but may not be the same if stations were rearranged.



Name	Value	Description
StationAddr	1	Modbus statio
TimeOut	1000	Time out in m
FunctCode15	Enable	The connecte
FunctCode16	Enable	The connecte
DataSwap	LswFirst	Float Data Fo
MaxBools	1920	Maximum nun
MaxReg	120	Maximum nun
DeviceDelay	10	Transmit dela

This is Node # 3.

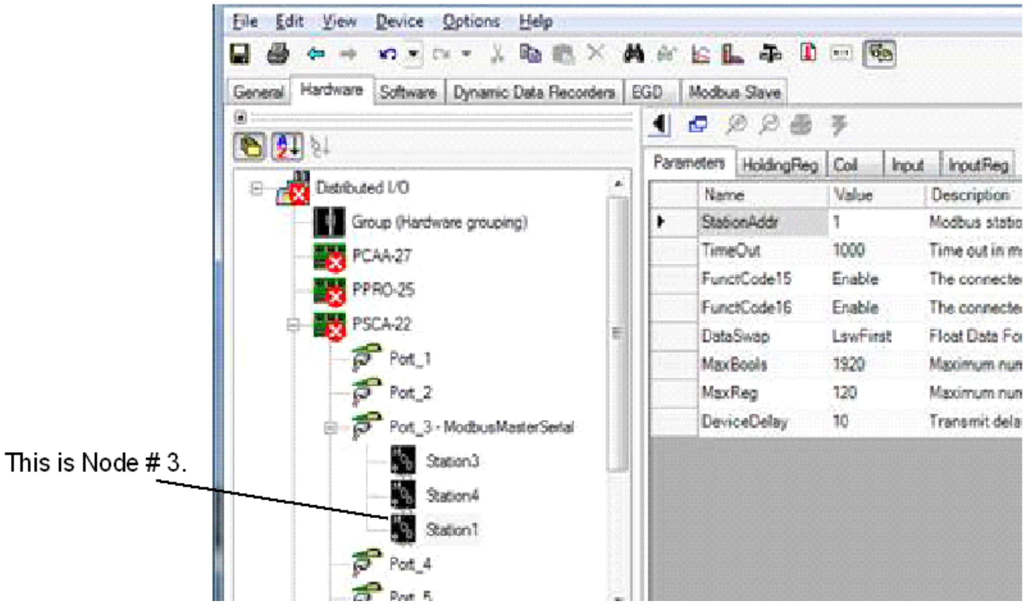
Solution

- Verify that the serial or Ethernet cable is connected to the field device.
- Verify that the device is powered-on and configured for the correct station ID.
- For serial connections, verify that the baud rate and parity are set correctly.
- For Ethernet connections, verify that the IP address is set correctly.

72-107

Description Comm Port #[ ] Node #[ ] Communication Failure - Bad Data (see alarm help)

Possible Cause The field device responded, but could not provide data for one or more points. The Node number refers to the position of the station or device as listed inside the port, as displayed from the Hardware Tab Tree View. The node number is usually the same as the station number, but may not be the same if stations were rearranged.



This is Node # 3.

Name	Value	Description
StationAddr	1	Modbus statio
TimeOut	1000	Time out in m
FunctCode15	Enable	The connecte
FunctCode16	Enable	The connecte
DataSwap	LswFirst	Float Data Fo
MaxBools	1920	Maximum nu
MaxReg	120	Maximum nu
DeviceDelay	10	Transmit dela

Solution

- Verify that the point mapping in the ToolboxST configuration matches the slave field device.
- Verify that float values request all 32 bits of the value. A float value requires two registers.

108-113

Description Configuration Problem Port #[ ]

Possible Cause The configuration file downloaded from the Toolbox ST application contained an error.

Solution

- Verify that the I/O and configuration compatibility codes agree between the ToolboxST configuration and the PSCA.
- Build and download the firmware and the configuration to the PSCA.
- If diagnostic persists, reboot the PSCA.

114-119

Description Electric Drive Port #[ ] Save Command failed

Possible Cause The last parameter set saved to the Kollmorgan drive was not successful.

Solution The verify step failed after attempting to save parameters to the drive. Retry the Save command to the Kollmorgan drive.

14.3 SSCA Simplex Serial Communication Input/Output

14.3.1 Functional Description

The Simplex Serial Communication Input/Output (SSCA) terminal board is a compact serial communication terminal board that provides up to six communication channels. Each channel may be configured for RS-232C, RS-485, or RS-422 signaling. The I/O pack plugs into the DC-62 pin connector to communicate with the Mark VIe controller over Ethernet.

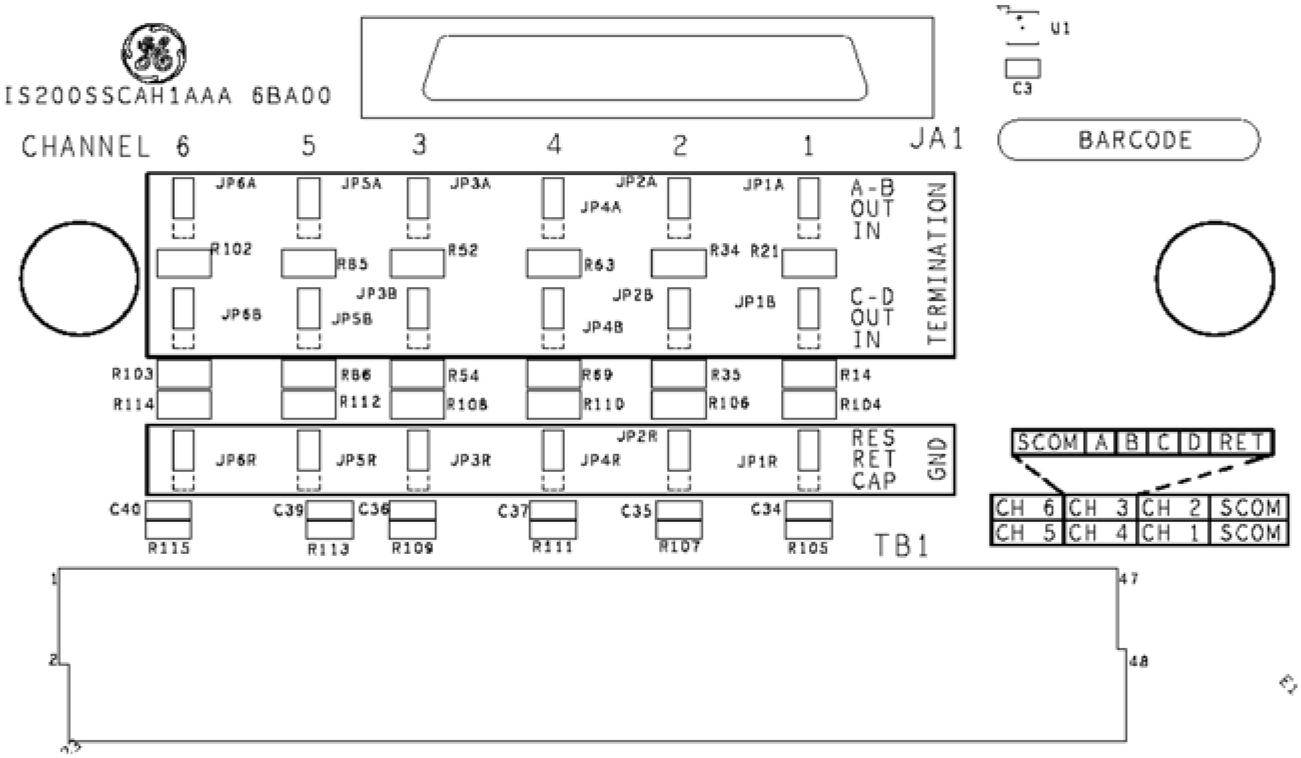
14.3.2 Installation

The SSCA is DIN-rail mounted using a sheet metal carrier and plastic insulator mount. This assembly will also bolt directly into a cabinet. There are two types of Euroblock connections available:

- SSCAH1 has a permanently mounted terminal block with 48 terminals.
- SSCAH2 has a right-angle header accepting a range of commercially available pluggable terminal blocks, with 48 terminals.

Note There is no shield termination strip with this design.

Typically, the SSCA uses #18 AWG (shielded twisted pair) wiring. The I/O cable shield termination is on an external mounting bracket supplied by the customer or by GE. The chassis ground connection uses E1 and E2 as mounting holes. One of the SCOM terminals (37-48) must be connected to a suitable shield ground.



SSCA Jumper Positions

14.3.3 Operation

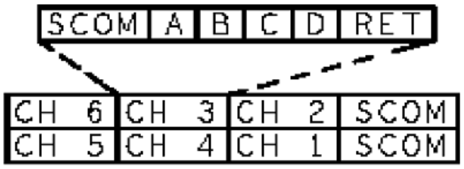
The SSCA includes six connection points for each of the six serial communication channels. The points include four signal lines A-D, a signal return, and a shield common (SCOM).

Signal Assignments

Protocol	A	B	C	D	Cable Length
RS-422	TX+	TX-	RX+	RX-	Up to 305 m (1000 ft)
RS-485	TX/RX+	TX/RX-	Jumper from A	Jumper from B	Up to 305 m (1000 ft)
RS-232C	DTR/RTS	TX	CTS	RX	Up to 15 m (50 ft) or 2500 pF

The return for RS-232C is through the terminal called *Ret*. The signals for all six serial communication channels are arranged in the same order, which is SCOM, A, B, C, D, Ret when viewed from left to right.

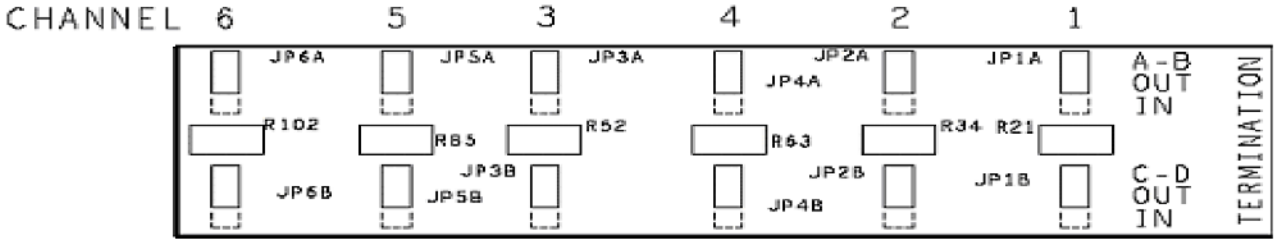
The groups of six signals for a serial channel are assigned to terminals adjacent to each other. When viewed from left to right, the channels on the bottom set of terminals are 5, 4, and 1. The top set of terminals contain channels 6, 3, and 2 when viewed from left to right. The board SCOM connections are grouped on the right side of the terminals. A signal location diagram is included on the SSCA.



Terminal Board Screw Connections

	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6
SCOM	26	25	13	14	2	1
PT_A	28	27	15	16	4	3
PT_B	30	29	17	18	6	5
PT_C	32	31	19	20	8	7
PT_D	34	33	21	22	10	9
Ret	36	35	23	24	12	11

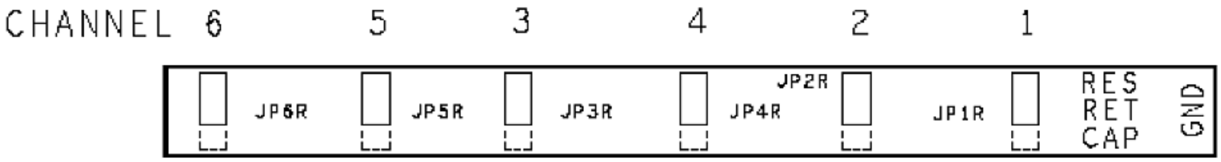
When using RS-422 or RS-485, a termination resistor must be provided at either end of a transmission line. The SSCA provides selectable termination resistors for each pair of signal lines. Jumpers JP1A and JP1B apply or remove the termination resistors between signals A-B and C-D. The same function is repeated for each serial communication channel. The default jumper position includes a disconnected termination resistor. The SSCA is clearly marked to display the relationship of the termination jumpers and the serial communication channel signals as displayed in the following figure.



Termination Jumpers

In RS-232C systems, it is often not desirable to have a hard ground of the Ret signal path on both ends of a cable. The SSCA includes jumper selectable grounding options for each of the six Ret lines. The line may be grounded through a 100 Ω resistor or through a 0.01 uF capacitor / 1M Ω resistor parallel combination. If the device attached to the SSCA has a hard ground of the Ret line, the capacitive ground should be selected on the SSCA. If there is not a hard ground on the connected equipment, the resistive ground (default position) should be selected on the SSCA.

Ret ground jumpers are identified on the SSCA as JP1R through JP6R. Positions are displayed as resistive (RES) and capacitive (CAP) return connection. All jumpers are clearly labeled.



Ground Jumpers

14.3.4 Specifications

Item	SSCA Specification
Number of Channels	Six
Termination Resistors	Jumper selectable between open and resistor of 121 Ω, ½ W, 1%
RS-232C Return Path Ground	Selectable between resistive ground of 100 Ω, ½ W, 1% or 1M Ω, ½ W, 1% in parallel with 0.01 uF, 500 V, 10% capacitor
Max Drops in RS-485 Systems	8
Size	15.9 cm high x 10.2 cm wide (6.25 in x 4.0 in)
Technology	Surface-mount

14.3.5 Diagnostics

The JA connector on the terminal board has its own ID device that is interrogated by the I/O pack. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and J connector location. When this chip is read by the I/O processor and a mismatch is encountered, a hardware incompatibility fault is generated.

14.3.6 SSCA Configuration

For the six serial communication channels:

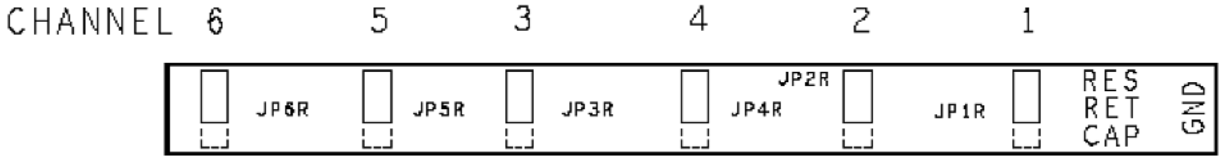
- Jumpers JP1A through JP6A apply or remove termination resistors between signal lines A and B
- Jumpers JP1B through JP6B apply or remove termination resistors between signal lines C and D
- Jumpers JP1R through JP6R select whether the return has a resistive or capacitive connection to SCOM.

All other configuration is performed from the ToolboxST application. Electronic selection of the serial communications method, either RS-232C, RS-422, or RS-485, is internal to the I/O pack.

14.3.6.1 RS-232C (Point-to-point)

- It is often not desirable to have a hard ground of the Ret signal path on both ends of a cable. SSCA includes jumper selectable grounding options for each of the six Ret lines.
- The line may be grounded through a 100 Ω resistor or, through a 0.01 uF capacitor / 1 M Ω resistor parallel combination.
- If the device attached to SSCA features a hard ground of the Ret line then the capacitive ground should be selected on SSCA. If there is not a hard ground on the connected equipment then the resistive ground (default position) should be selected on SSCA.
- Ret ground jumpers are identified on SSCA as JP1R through JP6R. Positions are displayed as RES and CAP for resistive and capacitive return connection. The jumpers are clearly labeled on the SSCA.

In general, if the information on third-party side hardware configuration (hard ground or not) is available during pre-FAT, keep Ret with resistance ground. The JP#R stays connected to RES (Default), and configuration must match the ToolboxST application configuration, as displayed in the following diagram.



Note If a computer is connected as a test simulation device (with MODSIM running), the wire from Pin-5 of D-Type connector must be connected to SCOM1.

Terminal Board Screw Connections

	SCOM	A	B	C	D	RET
Channel 1	26	28	30	32	34	36
Channel 2	25	27	29	31	33	35
Channel 3	13	15	17	19	21	23
Channel 4	14	16	18	20	22	24
Channel 5	02	04	06	08	10	12
Channel 6	01	03	05	07	09	11

Protocol	A	B	C	D	Cable Length
RS-422	TX+	TX-	RX+	RX-	Up to 305 m (1000 ft)
RS-485	TX/RX+	TX/RX-	Jumper from A	Jumper from B	Up to 305 m (1000 ft)
RS-232C	DTR/RTS	TX	CTS	RX	Up to 15 m (50 ft) or 2500 pF

14.3.6.2 RS-232C to Third-party Device (Slave)

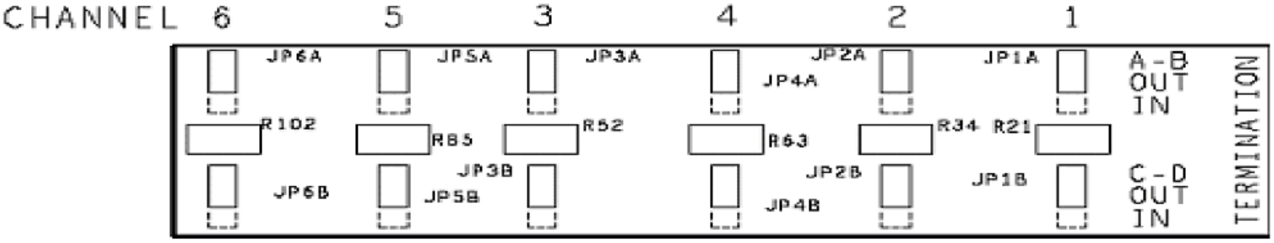
- B (TX) to third-party device (Slave) RX
- D (RX) to third-party device (Slave) TX
- A (DTR/RTS) to third-party device (Slave) CTS
- C (CTS) to third-party device (Slave) RTS
- I/O pack SSCA out (TX) —+——————+– (RX)
- I/O pack SSCA out (RX) —+—————-+– (TX)
- I/O pack SSCA out (DTR/RTS)—+—————+– (CTS)
- I/O pack SSCA out (CTS) —+—————+– (RTS)

Protocol-RS-232C	DTR/TRS	TX	CTS	RX	SCOM	RET
SSCA SIDE						
CHANNEL 1	28	30	32	34	26	36
CHANNEL 2	27	29	31	33	25	35
CHANNEL 3	15	17	19	21	13	23
CHANNEL 4	16	18	20	22	14	24
CHANNEL 5	4	6	8	10	2	12
CHANNEL 6	3	5	7	9	1	11

14.3.6.3 RS-422

- There is the need to provide a termination resistor at either end of a transmission line.
- SSCA provides selectable termination resistors for each pair of signal lines.
- Jumpers JP#A and JP#B apply or remove the termination resistors between signals A-B and C-D.
- Above Point 3 function is repeated for each serial communication channel. The default jumper position is to disconnect the termination resistor.
- The SSCA is clearly marked to display the relationship of the termination jumpers and the serial communication channel signals.

The configuration at SSCA jumper *(JP#A, JP#B set to IN)* must match the ToolboxST configuration as displayed in the following diagram. The 120 Ω resistance selection is used as an example.



Terminal Board Screw Connections

	SCOM	A	B	C	D	RET
Channel 1	26	28	30	32	34	36
Channel 2	25	27	29	31	33	35
Channel 3	13	15	17	19	21	23
Channel 4	14	16	18	20	22	24
Channel 5	02	04	06	08	10	12
Channel 6	01	03	05	07	09	11

Protocol	A	B	C	D	Cable Length
RS-422	TX+	TX-	RX+	RX-	Up to 305 m (1000 ft)
RS-485	TX/RX+	TX/RX-	Jumper from A	Jumper from B	Up to 305 m (1000 ft)
RS-232C	DTR/RTS	TX	CTS	RX	Up to 15 m (50 ft) or 2500 pF

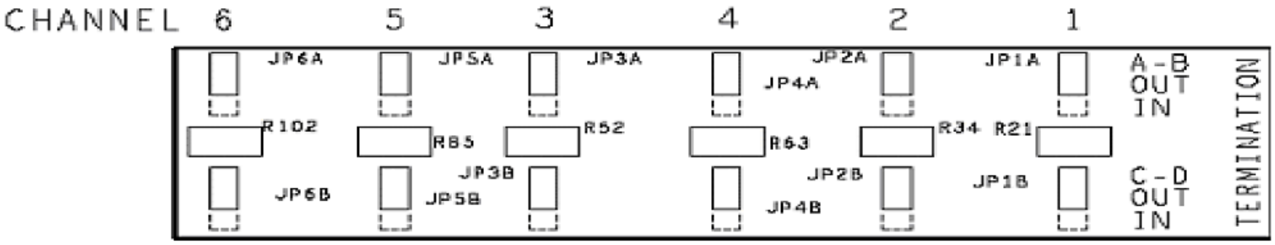
14.3.6.4 RS-485 Half-duplex to Third-party Device (Slave)

- A (TX/RX+) to third-party device (Slave) TX/RX+
- B (TX/RX-) to third-party device (Slave) TX/RX-
- C – Jumper from A
- D – Jumper from B

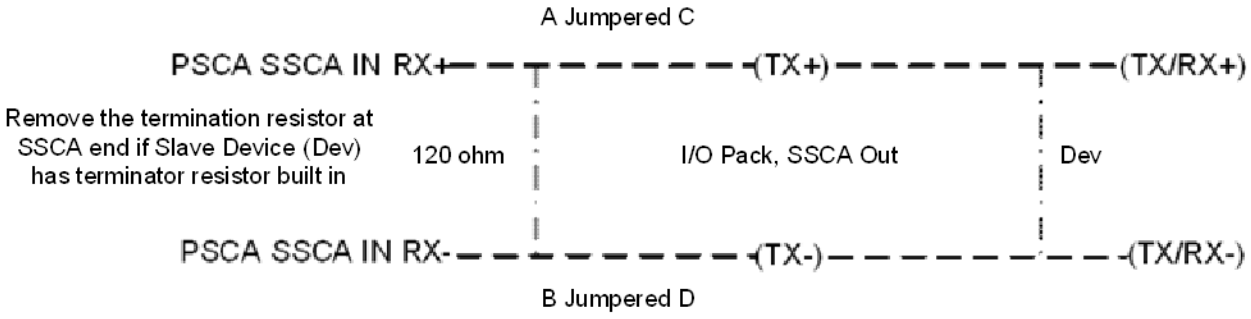
Note Put A/B termination **In**, but leave C/D termination **Out** on the terminal board.

Protocol-RS-485	**Slave Device Side**	**TX/RX+**	**TX/RX-**	**N/A**	**N/A**	**SCOM**	**RET**
SSCA SIDE	Media converter pins	DATA +	DATA -	JUMPER	JUMPER	SGND	
CHANNEL 1	RS-485	28	30	28-32	30-34	26	36
CHANNEL 2	RS-485	27	29	27-31	29-33	25	35
CHANNEL 3	RS-485	15	17	15-19	17-21	13	23
CHANNEL 4	RS-485	16	18	16-20	18-22	14	24
CHANNEL 5	RS-485	4	6	4-8	6-10	2	12
CHANNEL 6	RS-485	3	5	3-7	5-9	1	11

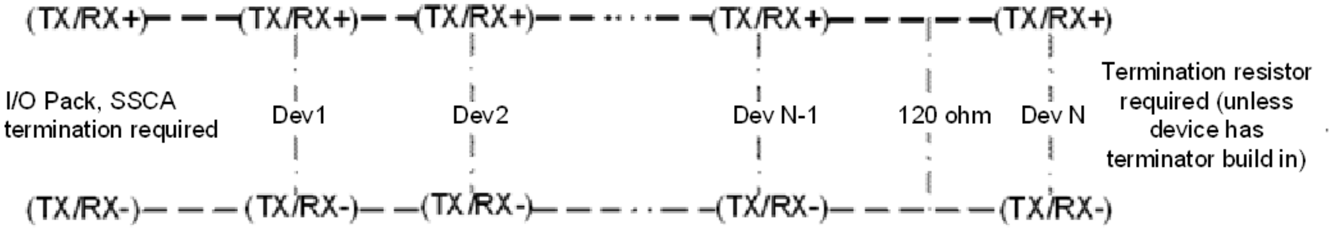
CHANNEL #	**A (TX/RX+)**	**B (TX/RX-)**	**C (JUMPERED WITH A)**	**D (JUMPERED WITH B)**	**JUMPER (JP#A)**	**JUMPER (JP#B)**
CHANNEL 1	28	30	32	34	JP1A - IN	JP1B – OUT
CHANNEL 2	27	29	31	33	JP2A - IN	JP2B – OUT
CHANNEL 3	15	17	19	21	JP3A - IN	JP3B – OUT
CHANNEL 4	16	18	20	22	JP4A - IN	JP4B – OUT
CHANNEL 5	4	6	8	10	JP5A - IN	JP5B – OUT
CHANNEL 6	3	5	7	9	JP6A - IN	JP6B – OUT



14.3.6.5 RS-485 (half-duplex) – Point-to-point



14.3.6.6 RS-485 (half-duplex) – Multidrop



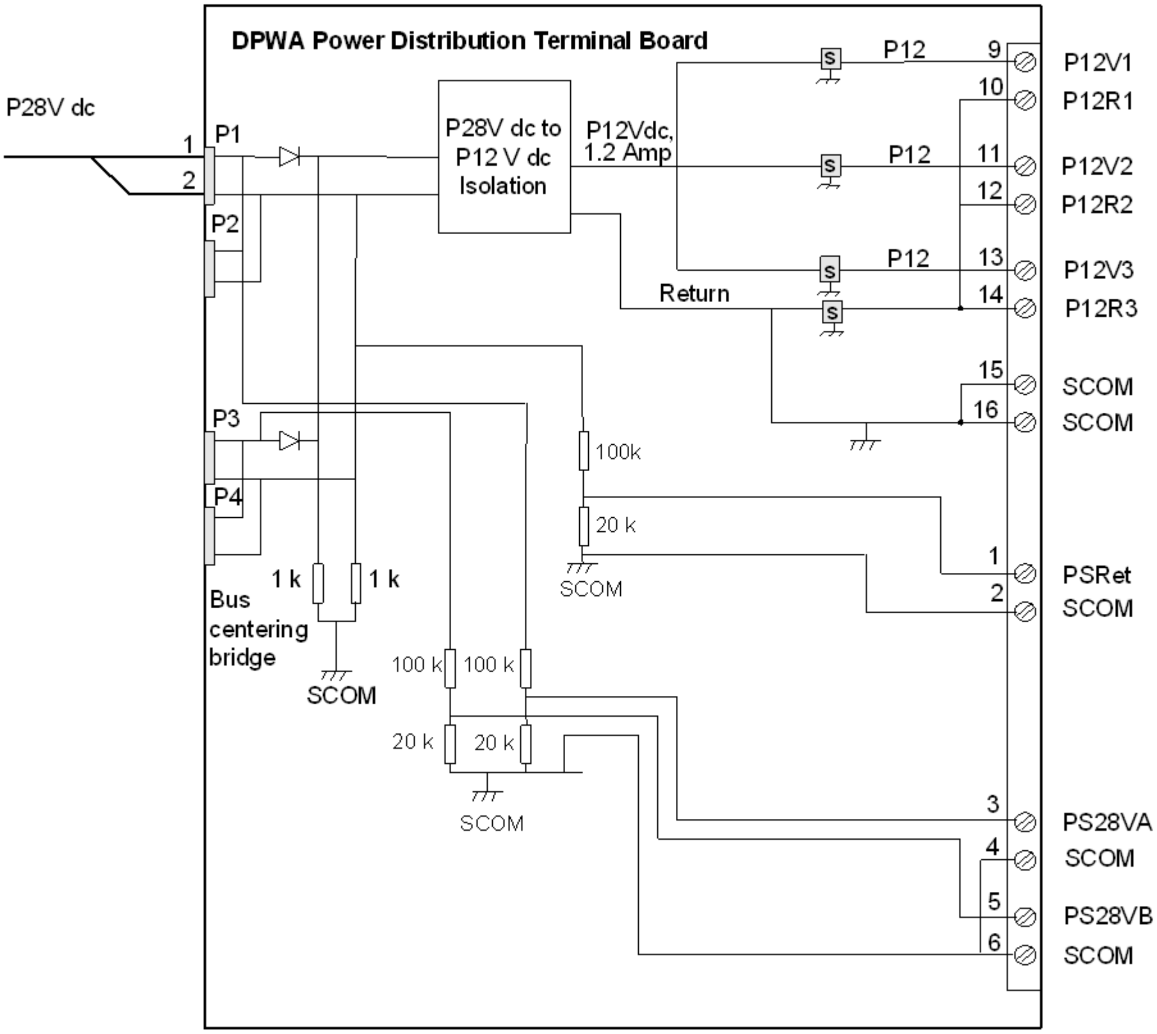
14.4 DPWA Transducer Power Distribution

The Transducer Power Distribution (DPWA) terminal board is a DIN-rail mounted power distribution board. It accepts input voltage of 28 V dc ±5%, provided through a two-pin Mate-N-Lok® connector. Connectors are provided for two independent power sources to allow the use of redundant supplies. The input can accept power from a floating isolated voltage source. DPWA provides excitation power to LG-1237 Honeywell pressure transducers.

The input to DPWA includes two 1 kΩ resistors from positive and negative input power to SCOM. These center a floating power source on SCOM. Attenuated input voltage is provided for external monitoring. Output power of 12 V dc ±5% is connected to external devices through a Euro-type terminal block, using screw terminals and AWG#18 twisted-pair wiring. The DPWA provides three output terminal pairs with a total output rated at 0 to 1.2 A. The outputs are compatible with the XDSAG#AC interface board. Outputs are short circuit-protected and self-recovering.

14.4.1 Installation

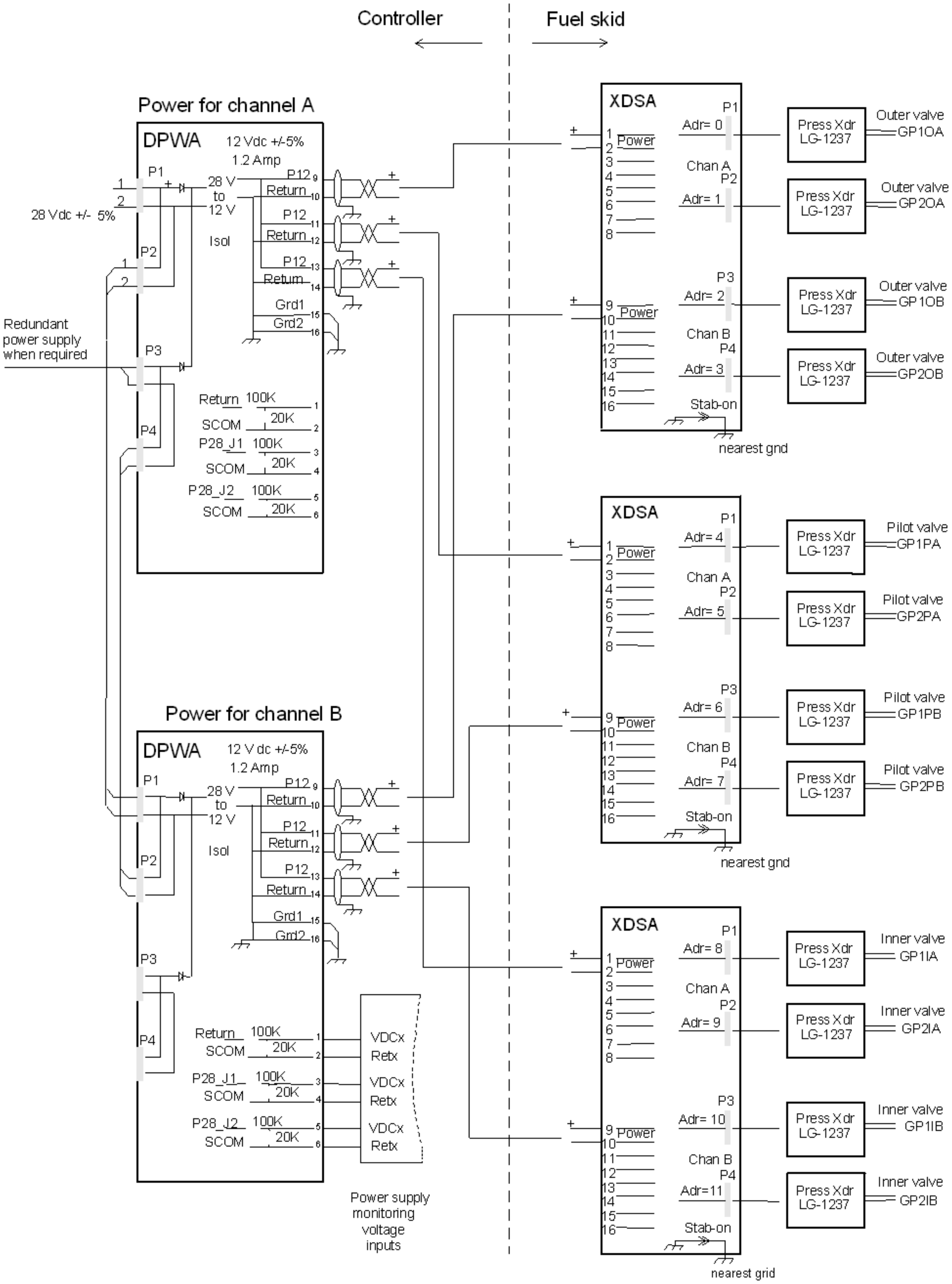
Mount the DPWA assembly on a standard DIN-rail. Connect input power to connector P1. If multiple DPWA boards are used, use connector P2 as a pass-through connection point for the power to additional boards. If a redundant power input is provided, connect power to connector P3 and use connector P4 as the pass-through to additional boards. Connect the wires for the three output power circuits on screw terminal pairs 9-10, 11-12, and 13-14. The DPWA terminal board includes two screw terminals, 15 and 16, for SCOM (ground) that must be connected to a good shield ground.



DPWA Board Block Diagram

14.4.2 Operation

The DPWA has an on-board power converter that changes the 28 V dc to 12 V dc for the transducers. A redundant 28 V dc supply can be added if needed. The following figure displays the DPWA power distribution system feeding power to 12 LG-1237 pressure transducers.



DPWA Power Distribution to XDSA and Smart Pressure Transducers

14.4.3 Specifications

Item	DPWA Specification
Number of Channels	Three power output terminal pairs
Input Voltage	28 V dc ±5%, provisions for redundant source
Input Current	Limited by protection to no more than 1.6 A steady state
Output Voltage	12 V dc ±5%, maximum total current of 1.2 A, short circuit protected, and self-recovering
Monitor Voltages	Attenuated by 6:1 ratio

14.4.4 Diagnostics

The DPWA features three voltage outputs to permit monitoring of the board input power. The voltage monitor outputs are all attenuated by a 6:1 ratio to permit reading the 28 V dc using an input voltage with 5 V dc full scale input. Terminal 1 (PSRet) is the attenuated voltage present on the power input return line. Terminal 3 (PS28VA) is the attenuated voltage present on the P1 positive power input line. Terminal 5 (PS28VB) is the attenuated voltage present on the P3 positive power input line. Terminals 2, 4, and 6 provide a return SCOM path for the attenuator signals.

In redundant systems, monitoring PS28VA and PS28VB permits the detection of a failed or missing redundant input. In systems with floating 28 V power, with the input centered on SCOM, the positive and return voltages should be approximately the same magnitude as a negative voltage on the return. If a ground fault is present in the input power, it may be detected by positive or return attenuated voltage approaching SCOM while the other signal doubles.

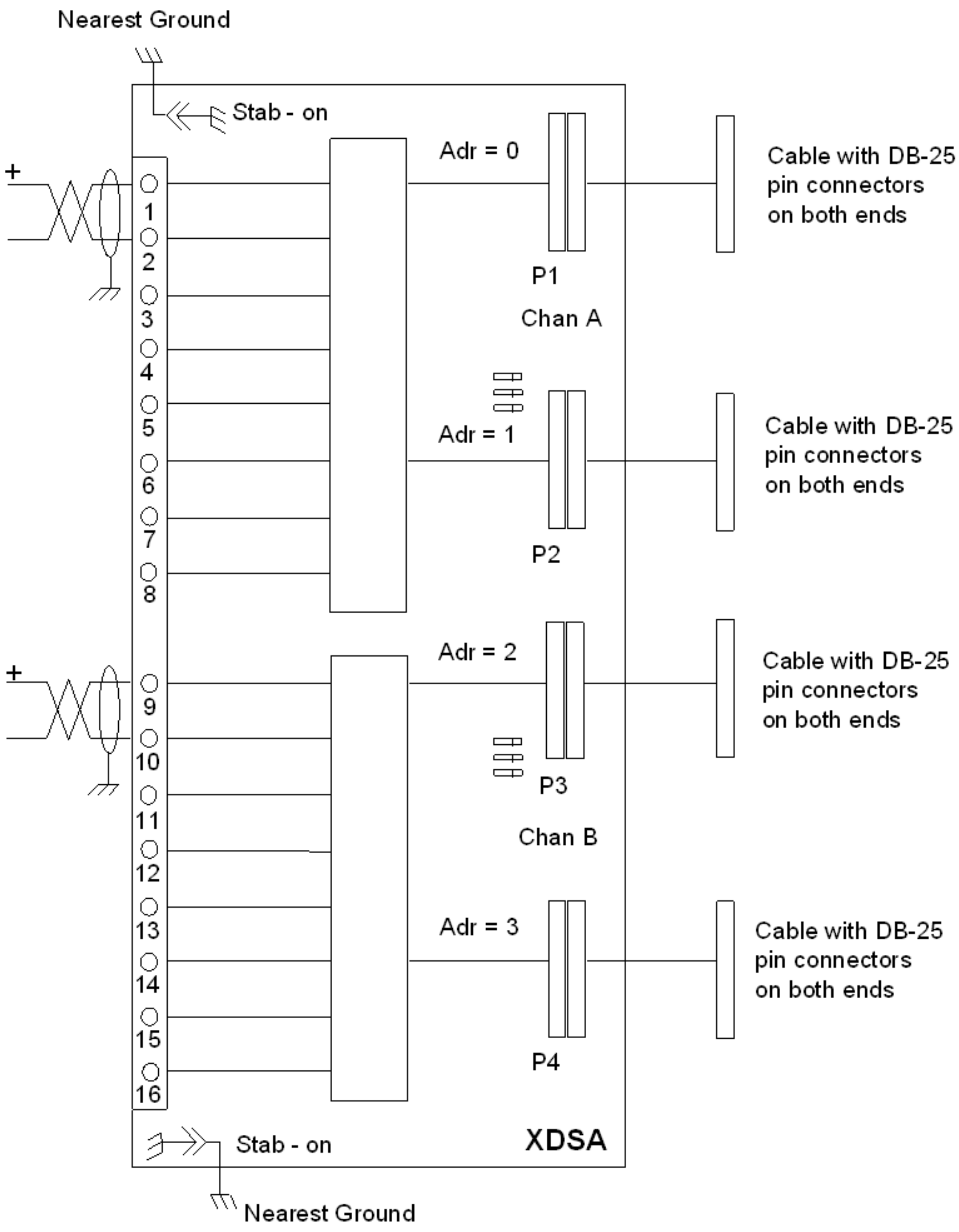
14.5 XDSA Transducer Interface

14.5.1 Functional Description

The Transducer Interface (XDSA) terminal board is intended for installation adjacent to one or more type LG-1237 Honeywell Smart Pressure Transducers featuring serial communications. The board accepts 12 V dc input power and serial data communications and routes the signals through four cables, with DB-25 connectors on each end, compatible with the Honeywell sensors. The board is designed with two independent circuits that support redundant sensor arrangements. Jumpers are provided to set sensor addresses and to select serial communications termination resistance. XDSA has features allowing connection of multiple XDSA boards in one system. XDSA provides signal routing to type LG-1237 Honeywell Smart Pressure Transducers.

14.5.2 Installation

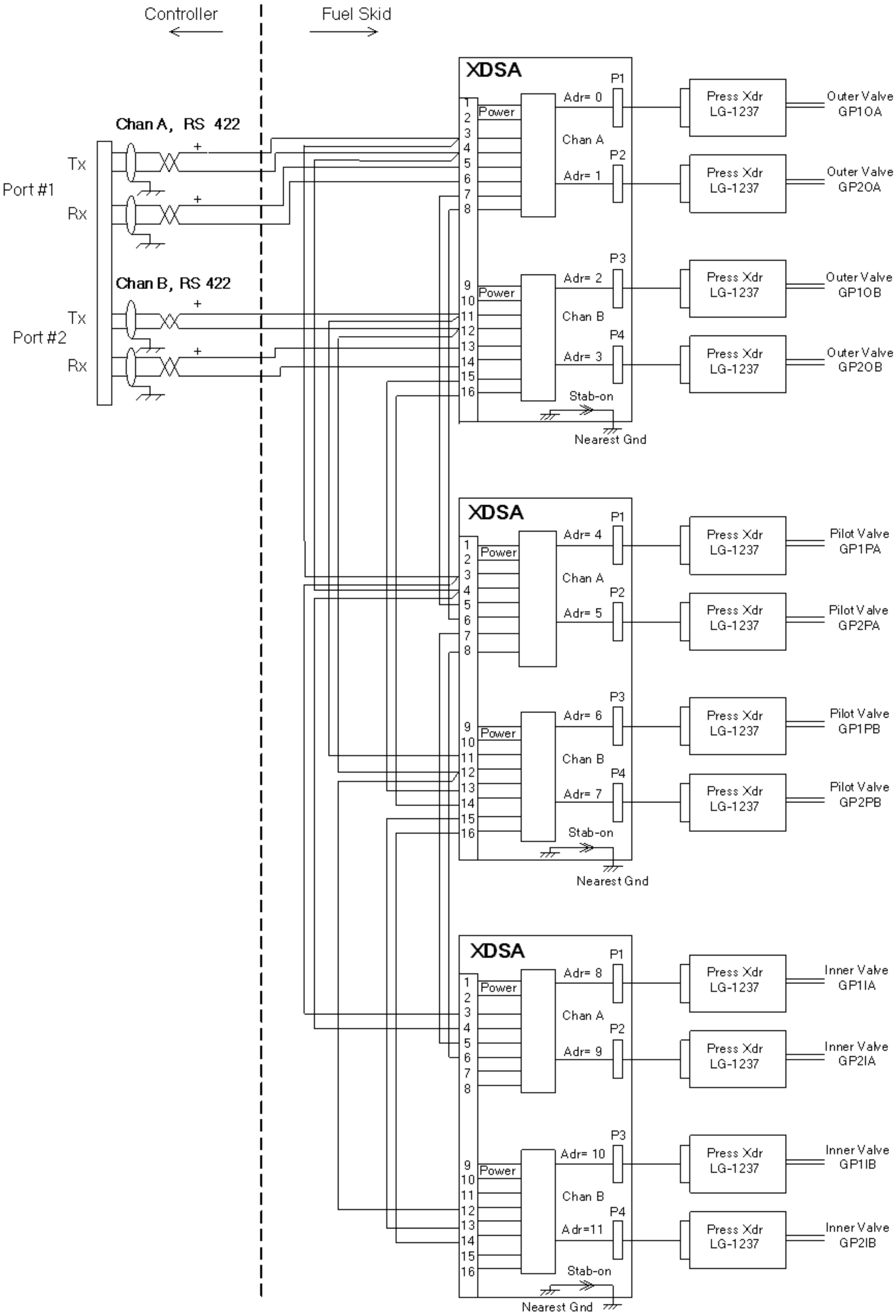
Two DPWA terminal boards supply 12 V dc ±5% to terminals 1, 2, 9, and 10. Terminals 3 through 8 and 11 through 16 are used for RS-422 multidrop communications. Each XDSA terminal board functions as two independent boards. A stab-on ground connection is located on each end of the board, one for each of the board sections. The board connects to four pressure sensors using cables with DB25 connectors on each end. The following figure displays the wiring connections for the XDSA terminal board.


Nearest Ground
Stab - on
+
1
2
3
4
5
6
7
8
Adr = 0
P1
Chan A
Cable with DB-25 pin connectors on both ends
Adr = 1
P2
Cable with DB-25 pin connectors on both ends
+
9
10
11
12
13
14
15
16
Adr = 2
P3
Chan B
Cable with DB-25 pin connectors on both ends
Adr = 3
P4
Cable with DB-25 pin connectors on both ends
Stab - on
XDSA
Nearest Ground

XDSA Terminal Board Block Diagram

The DPWA boards supply 12 V dc ±5% using AWG#18 shielded twisted-pair wiring. Each XDSA terminal board supplies power for four LG-1237 pressure transducers using cables with DB-25 connectors on each end. Power is separated between the two sections of the XDSA terminal board preserving the redundancy of the pressure sensing system. A separate ground is also provided for each section of the board. Refer to the figure, *DPWA Power Distribution to XDSA and Smart Pressure Transducers*.

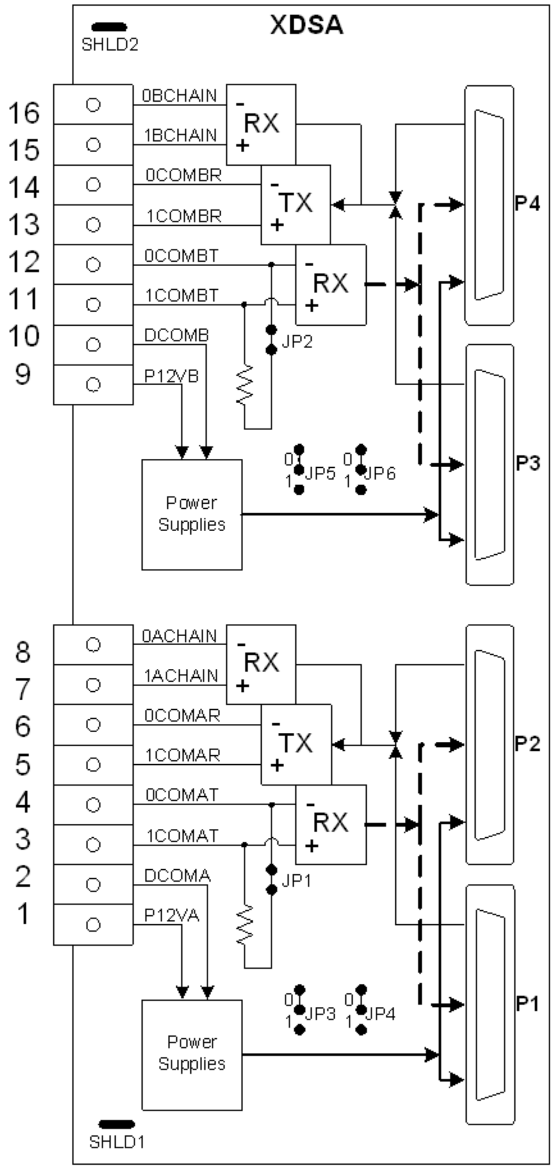
The following figure displays the serial communication wiring for three XDSA terminal boards connected to a pair of serial communication channels. The pass-through serial path is wired for signals from the sensors to the control.



XDSA Serial Communication Wiring Diagram

14.5.3 Operation

The following figure displays the functional block diagram and actual board layout for the XDSA terminal board. Input terminal 1 and output connector P1 are at the bottom of the board. Input power of 12 V dc ±5% is applied to terminals 1 (positive) and 2 (negative). Serial transmissions from a control are received on terminals 3 (positive) and 4 (negative) with transmission path termination set by jumper JP1. Serial output from connected pressure sensors is on terminals 5 (positive) and 6 (negative). Terminals 7 (positive) and 8 (negative) provide a pass-through path for an additional XDSA board as displayed in the section, *Installation*. Device address selections are determined by jumpers JP3 and JP4.



XDSA Functional Block Diagram and Smart Pressure Transducers

14.5.4 Specifications

Item	XDSA Specification
Number of Channels	DB-25 connections for four pressure sensors
Input Voltage	12 V dc ±5% from DPWA or equivalent

14.5.5 Configuration

Six jumpers are provided on the XDSA terminal board to select both RS-422 serial communication termination resistors and the address of the pressure sensors.

Jumpers JP1 and JP2 determine if the serial input terminating resistor is in or out. In is selected for the XDSA board that is at the end of the transmission path. Out is selected for all other XDSA boards within the signal path.

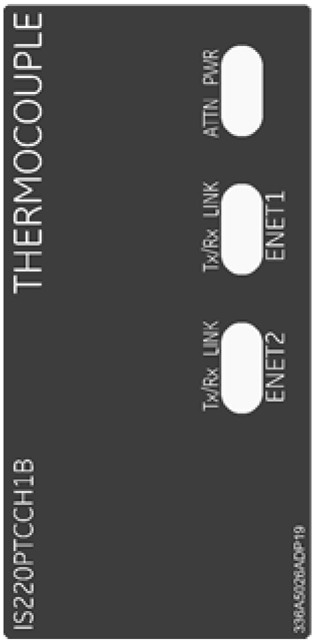
Jumpers JP3 through JP6 set the address of the sensors wired to P1 through P4. The sensor address is set by four signals on the DB-25 connector. The signals are a combination of fixed wiring and jumper positions on the two least significant bits. Each jumper has two positions, labeled 0 and 1. Refer to the following table to determine the correct sensor address.

J3/J4	0/0	1/0	0/1
P1	0	4	8
P2	1	5	9

J5/J6	0/0	1/0	0/1
P3	2	6	10
P4	3	7	11

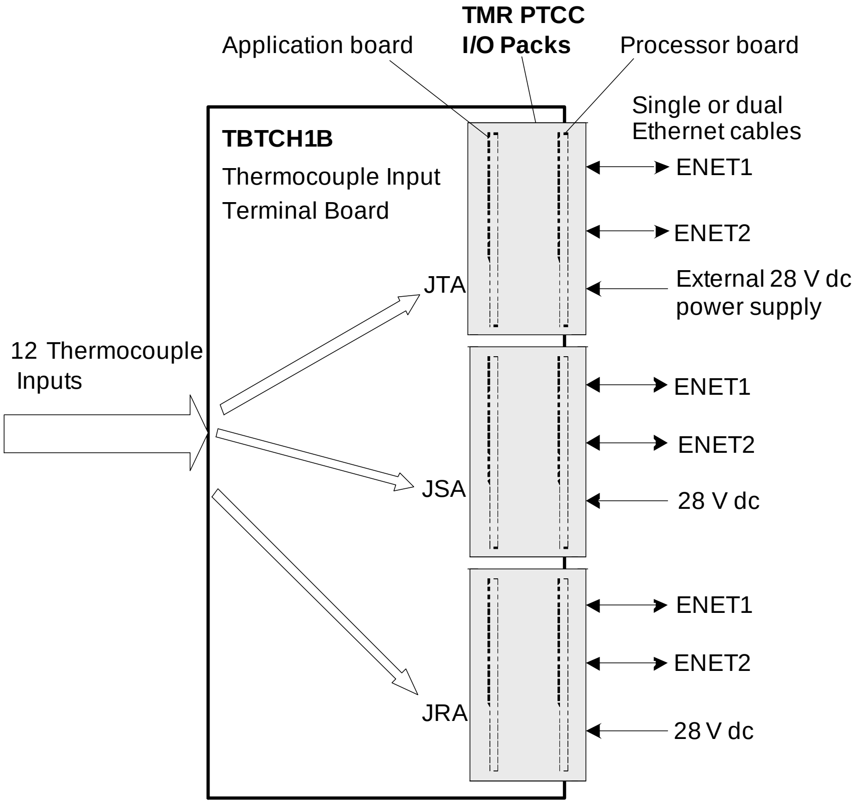
15 PTCC, YTCC Thermocouple Input Modules

15.1 Mark VIe PTCC Thermocouple Input Pack



The Thermocouple Input PTCC provides the electrical interface between one or two I/O Ethernet networks (IONet) and a thermocouple input terminal board. The I/O pack contains a BPPx processor board and an acquisition board specific to the thermocouple input function. Input to the PTCC is through dual RJ-45 Ethernet connectors and a three-pin power input. Output is through a DC-37 pin connector that mates directly with the associated terminal board connector. Visual diagnostics are provided through indicator LEDs.

In a simplex configuration using the TBTCH1C terminal board, each PTCC is capable of handling up to 12 thermocouple inputs, for a total of 24 inputs (with two of them). In simplex configuration using the TBTCH1B terminal board, each PTCC is capable of handling up to 12 thermocouple inputs (for a total of 24 inputs), provided the two PTCCs are installed at the JRA and JTB connectors. In TMR configuration with the TBTCH1B, three PTCCs are used with three cold junctions, but only 12 thermocouples are available.



15.1.1 Compatibility

The PTCC includes one of the following compatible processor boards:

- PTCCH1A and H2A contain a BPPB processor board
- PTCCH1B and H2B contains a functionally compatible BPPC processor board that is supported in the ControlST* software suite V04.06 and later

The PTCC is available in the following two versions:

- PTCCH1A and PTCCH1B support E, J, K, S, and T types of standard thermocouples and mV inputs. The mV span is –8 to 45 mV.
- PTCCH2A and H2B support E, J, K, S, T, B, N, and R types of standard thermocouples and mV inputs. The mV span for PTCCH2 is –20 to 95 mV.

Attention

B, N and R types of thermocouples should only be selected if PTCCH2A or PTCCH2B is used. These types of thermocouples must not be used or selected with PTCCH1A or PTCCH1B I/O packs.

The PTCC is compatible with the thermocouple input terminal board TBTC, and the simplex STTC terminal board, but not the DIN-rail mounted DTTC board. The following table provides the details of the terminal board compatibility.

Terminal Board	Configuration	# Packs	Thermocouple Inputs	Connectors
TBTCH1B, S1B	Simplex	1	12	Any
		2	24†	JRA and JTB
	TMR	3	12	JRA, JSA, JTA
TBTCH1C, S1C	Simplex	1 or 2	12 or 24	JA1, JB1
STTCH1A, S1A, H2A, S2A	Simplex	1	12	JA1

† Support of 24 thermocouple inputs on the TBTC_1B in simplex configuration requires the use of two PTCC I/O packs, which must be connected to JRA and JTB.

15.1.2 Installation

➢ To install the PTCC

1. Securely mount the desired terminal board.
2. Directly plug the PTCC into the terminal board connectors.
3. Mechanically secure the PTTC(s) using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right-angle force applied to the DC-37 connector between the PTCC and the terminal board. The adjustment should only be required once in the service life of the product.

Note The PTCC mounts directly to a Mark* VIe terminal board. Simplex terminal boards (TBTCH1C) have two DC-37 pin connectors that receive the PTCC, one for each set of 12 TC inputs. TMR capable terminal boards (TBTCH1B) have six DC-37 pin connectors. The PTCC directly supports all of these connections.

4. Plug in one or two Ethernet cables depending on the system configuration. The PTCC will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
5. Apply power by plugging in the connector on the side of the PTCC. It is not necessary to remove power from the cable before plugging it in because the PTCC has inherent soft-start capability that controls current inrush on power application.
6. Use the ToolboxST* application to configure the PTCC as necessary.

15.1.3 Operation

The following features are common to the distributed I/O modules:

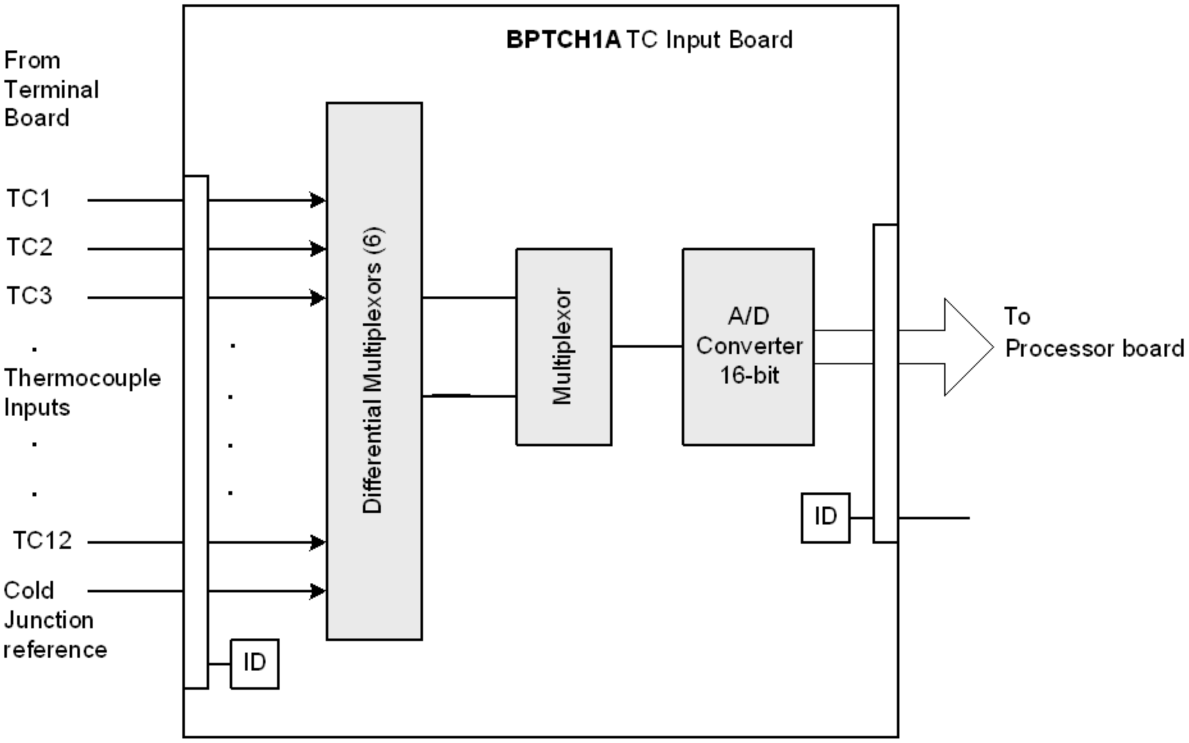
- *BPPx Processor*
- *Processor LEDs*
- *Power Management*
- *ID Line*
- *I/O Module Common Diagnostic Alarms*

15.1.3.1 Analog Input Hardware

The PTCC internal input board (BPTC) accepts 12 signals at mV levels from the thermocouples wired to the terminal board. The analog input section consists of six differential multiplexers, a main multiplexer, and a 16-bit analog to digital converter that sends the digital data to the adjacent processor board. Each input has hardware and firmware filters, and the converter samples at up to 120 Hz.

Type E, J, K, S, and T thermocouples can be used with PTCCH1A, and they can be grounded or ungrounded. Type E, J, K, S, T, B, N and R thermocouples can be used with PTCCH2A, and they can be grounded or ungrounded. Thermocouples can be located up to 300 meters (984 feet) from the turbine I/O panel with a maximum two-way cable resistance of 450 Ω.

Linearization for individual thermocouple types is performed in software by the I/O pack board. A thermocouple, which is determined to be out of the hardware limits, is removed from the scanned inputs to prevent adverse effects on other input channels. If two I/O packs are used, and both Cold Junction (CJ) devices are within the configurable limits, then the average of the two is used for CJ compensation.



15.1.3.2 Thermocouple Limits

TBTC with PTCCH1

Thermocouple inputs support a full-scale input range of –8.0 mV to 45.0 mV. The following table displays typical input voltages for different thermocouple types versus the minimum and maximum temperature range. The CJ temperature is assumed to range from –30 to 65°C (–22 to 149 °F). The units (°C or °F) are based on the *ThermCplUnit* parameter.

TC Limits for I/O Pack Type PTCCH1

Item	Thermocouple Type				
	E	**J**	**K**	**S**	**T**
Low range, °F	-60	-60	-60	0	-60
Low range, °C	-51	-51	-51	-17.78	-51
mV at low range with reference at 70°C (158 °F)	-7.174	-6.132	-4.779	-0.524	-4.764
High range, °F	1100	1400	2000	3200	750
High range, °C	593	760	1093	1760	399
mV at high range with reference at 0°C (32 °F)	44.547	42.922	44.856	18.612	20.801

TBTC with PTCCH2

Thermocouple inputs support a full-scale input range of -20.0 mV to 95.0 mV. The following table displays typical input voltages for different thermocouple types versus the minimum and maximum temperature range. The CJ temperature is assumed to range from -30 to 65°C (-22 to 149 °F).

TC Limits for I/O Pack Type PTCCH2

Item	Thermocouple Type				
	E	**J**	**K**	**S**	**T**
Low range, °F	-60	-60	-60	0	-60
Low range, °C	-51	-51	-51	-17.78	-51
mV at low range with reference at 70°C (158 °F)	-7.174	-6.132	-4.779	-0.524	-4.764
High range, °F	1832	2192	2372	3200	752
High range, °C	1000	1200	1300	1760	400
mV at high range with reference at 0°C (32 °F)	76.373	69.553	52.41	18.612	20.869

TC Limits for I/O Pack Type PTCCH2

Item	Thermocouple Type		
	B	**N**	**R**
Low range, °F	32	-60	0
Low range, °C	0	-51	-17.78
mV at low range with reference at 70°C (158 °F)	-0.0114	-3.195	-0.512
High range, °F	3272	2282	3092
High range, °C	1800	1250	1700
mV at high range with reference at 0°C (32 °F)	13.593	45.694	20.220

15.1.3.3 Cold Junctions

The CJ signal goes into signal space and is available for monitoring. Acceptable limits are configured, and if a CJ goes outside the limit, a logic signal is set. A 1 °F error in the CJ compensation will cause a 1 °F error in the thermocouple reading.

Hard-coded limits are set at -50 to 85°C (-58 to 185 ºF), and if a CJ goes outside this, it is regarded as unhealthy. Most CJ failures are open or short circuit. If the CJ is declared bad, the backup value (CJBackup, an output variable sent from the controller) is used. This backup value can be derived from CJ readings on other terminal boards, or can be the configured default value. The units (°C or °F) are based on the *ColdJuncUnit* parameter.

15.1.4 PTCC Specifications

Item	PTCC Specification
Number of Channels	12 channels per I/O pack
Thermocouple Types	E, J, K, S, T thermocouples, and mV inputs for PTCCH1. E, J, K, S, T, B, N, R thermocouples, and mV inputs for PTCCH2. ***B, N and R types of thermocouples should only be selected with PTCCH2A or PTCCH2B.***
Span	-8 mV to 45 mV for PTCCH1 -20 mV to 95 mV for PTCCH2
A/D Converter	Sampling type 16-bit A/D converter
Cold Junction Compensation	Reference junction temperature measured in each module TMR board has three cold junction references
Cold Junction Temperature Accuracy	Over the Celsius operating range: 1.1°C Over the Fahrenheit operating range: 2 °F
Conformity Error	Maximum software error 0.14ºC (0.25 ºF)
Measurement Accuracy	PTCCH1 = 53 µV (excluding cold junction reading). Example: For type K, at 1000 °F, including cold junction contribution, RSS error= 3 °F PTCCH2 = 115 µV (excluding cold junction reading). Example: For type K, at 1000 °F, including cold junction contribution, RSS error= 6 °F
Common Mode Rejection	AC common mode rejection 110 dB at 50/60 Hz, for balanced impedance input. Both hardware and firmware filtering.
Common Mode Voltage	±5 Volts
Normal Mode Rejection	Rejection of 250 mV rms at 50/60 Hz, ±5%, Both hardware and firmware filtering provides a total of 80 dB NMRR
Scan Time	All inputs are sampled at up to 120 times per second per input
Fault Detection	High/low (hardware) limit check High/low system (software) limit check Monitor readings from all TCs, CJs, calibration voltages, and calibration zero readings
Ambient Rating for Enclosure Design†	PTCCH1B is rated from -40 to 70°C (-40 to 158 °F) PTCCH1A is rated from -30 to 65°C (-22 to 149 °F)

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

15.1.5 Diagnostics

The I/O pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set

Details of the individual diagnostics are available in the ToolboxST application. The diagnostic signals can be individually latched, and then reset with the RESET_DIA signal if they go healthy.

15.1.6 Configuration

15.1.6.1 Parameters

Parameter	Description	Choices
SysFreq	System Frequency (used for noise rejection)	60 Hz, 50 Hz
SystemLimits	Allows user to temporarily disable all system limit checks for testing purposes. Setting this parameter to Disable will cause a diagnostic alarm to occur.	Enable (default), Disable
AutoReset	Automatic restoring of thermocouples removed from scan	Disable, Enable

15.1.6.2 Thermocouples

Thermocouple Name	Thermocouple Description	Choices
Thermocouple01	First of 24 thermocouples, point signal	Point Edit (Input FLOAT)
Thermocouple12		
ThermCplType	Select thermocouples type or mV input. Unused inputs are removed from scanning. The mV inputs are primarily for maintenance, but can also be used for custom remote CJ compensation. Standard remote CJ compensation is also available.	PTCCH1– Unused, mV, T, K, J, E, or S PTCCH2 – Unused, mV, T, K, J, E, S, B, N, or R B, N and R types of thermocouples should only be selected if PTCCH2A or PTCCH2B is used.

Thermocouple Name	Thermocouple Description	Choices
ThermCplUnit	Select thermocouples display unit in °C or °F. This value needs to match units of attached variable. The ThermCplUnit parameter affects the native units of the controller application variable. It is only indirectly related to the tray icon and associated unit switching capability of the HMI. This parameter should not be used to switch the display units of the HMI.	deg_F, deg_C
	Caution **Do not change the ThermCplUnit parameter because these changes will require corresponding changes to application code and to the Format Specifications or units of the connected variable. This parameter modifies the actual value sent to the controller as seen by application code. Application code that is written to expect degrees Fahrenheit will not work correctly if this setting is changed. External devices, such as HMIs and Historians, may also be affected by changes to this parameter.**	
ReportOpenTC	For PTCCH2 version only; this parameter sets the failed state of an open thermocouple to either hot (high) or cold (low). This parameter is not applicable to the PTCCH1 version.	Fail_Cold, Fail_Hot
LowPassFiltr	Enable 2 Hz low pass filter	Enable, Disable
SysLimit1	System Limit 1 in °C, °F, or mV	-450 to 3500 (FLOAT)
SysLim1Enabl	Enable system limit 1 fault check, a temperature limit which can be used to create an alarm.	Enable, Disable
SysLim1Latch	Latch system limit 1 fault Determines whether the limit condition will latch or unlatch; reset used to unlatch	NotLatch, Latch
SysLim1Type	System limit 1 check type limit occurs when the temperature is greater than or equal (≥), or less than or equal to (≤) a preset value	≥ or ≤
SysLimit2	System Limit 2 in °C, °F, or mV	-450 to 3500 (FLOAT)
SysLim2Enabl	Enable system limit 2 fault check, a temperature limit which can be used to create an alarm.	Enable, Disable
SysLim2Latch	Latch system limit 2 fault Determines whether the limit condition will latch or unlatch; reset used to unlatch System limit 2 check type limit occurs when the temperature is greater than or equal (≥), or less than or equal to (≤) a preset value	NotLatch, Latch

Thermocouple Name	Thermocouple Description	Choices
SysLim2Type	System limit 2 check type limit occurs when the temperature is greater than or equal (≥), or less than or equal to (≤), a preset value.	≥ or ≤
TMR_DiffLimt	Diagnostic limit, TMR input vote difference in engineering units Limit condition occurs if three temperatures in R, S, T differ by more than a preset value (engineering units); this creates a voting alarm condition.	-450 to 3500 (FLOAT)

15.1.6.3 Cold Junctions

Cold junctions are similar to thermocouples but without low pass filters.

Cold Junction Name	Cold Junction Description	Choices
ColdJuncType	Select CJ Type	Remote, Local
ColdJuncUnit	Select TC Display Unit Deg °C or °F. Value needs to match units of attached variable	Deg_F, Deg_C
SysLimit1	System Limit 1 - Deg °F or Deg °C	-40 to 185 (FLOAT)
SysLim1Enabl	Enable System Limit 1 Fault Check	Disable, Enable
SysLim1Latch	Latch System Limit 1 Fault	NotLatch, Latch
SysLim1Type	System Limit 1 Check Type (≥ or ≤)	≥ or ≤
SysLimit2	System Limit 2 - Deg °F or Deg °C	-40 to 185 (FLOAT)
SysLim2Enabl	Enable System Limit 2 Fault Check	Disable, Enable
SysLim2Latch	Latch System Limit 2 Fault	NotLatch, Latch
SysLim2Type	System Limit 2 Check Type (≥ or ≤)	≥ or ≤
TMR_DiffLimt	Diag Limit, TMR Input Vote Difference, in Eng Units	-450 to 3500 (FLOAT)

15.1.6.4 Variables

Variable	Description	Direction	Type
L3DIAG_PTCC	I/O Diagnostic Indication	Input	BIT
LINK_OK_PTCC	I/O Link Okay Indication	Input	BIT
ATTN_PTCC	I/O Attention Indication	Input	BIT
PS18V_PTCC	I/O 18 V Power Supply Indication	Input	BIT
PS28V_PTCC	I/O 28 V Power Supply Indication	Input	BIT
IOPackTmpr	I/O Pack Temperature (deg °F)	AnalogInput FLOAT	
SysLim1TC1	System limit 1 for thermocouple 1	Input	BIT
↓	↓	↓	
SysLim1TC12	System limit 1 for thermocouple 12	Input	BIT
SysLim1CJ1	System limit 1 for cold junction 1	Input	BIT
SysLim2TC1	System limit 2 for thermocouple 1	Input	BIT
↓	↓	↓	
SysLim2TC12	System limit 2 for thermocouple 12	Input	BIT
SysLim2CJ1	System limit 2 for cold junction 1	Input	BIT
CJBackup	Backup Cold Junction Temperature (°F or °C based on Cold Junction configuration)	AnalogOutput FLOAT	
CJRemote1	Remote Cold Junction Temperature. Used when Cold Junction set to Remote (°F or °C based on Cold Junction configuration)	AnalogOutput FLOAT	

15.2 PTCC Specific Alarms

The following alarms are specific to the PTCC I/O pack.

32-43

Description Thermocouple [ ] input voltage exceeds HW limit ([ ])

Possible Cause

- Thermocouple millivolt input to the analog-to-digital converter exceeded the converter limits and will be removed from the scan.

Solution

- Check field wiring, including shields.
- Check installation of the I/O pack on the terminal board. Problem is usually not a I/O pack or terminal board failure if other thermocouples are working correctly.

80

Description Cold Junction [ ] input voltage exceeds HW limit ([ ])

Possible Cause Cold junction input to the analog-to-digital converter exceeded the limits of the converter. If a cold junctions fails, the **CJ_Backup** value is used.

Solution

- Check the mounting of the I/O pack on the terminal board.
- Replace the terminal board.
- Replace the I/O pack.

92-103

Description Thermocouple [ ] value beyond range of configured TC type ([ ] deg)

Possible Cause

- Thermocouple mV input exceeded range of linearization (lookup) table for this TC type. Refer to documentation for specified thermocouple ranges.
- Thermocouple configured as wrong type.
- Board detected a thermocouple open, applied bias to circuit, driving it to a large negative number.
- Stray voltage or noise caused the input to exceed its range.

Solution

- Check field wiring, including shields.
- Check thermocouple for open circuit.
- Verify that the thermocouple type matches the configuration.
- Measure incoming mV signal and verify that it is within the specified thermocouple range.

128

Description Logic Signal [ ] Voting Mismatch

Possible Cause N/A

Solution N/A

160

Description Internal pack power supply not OK.

Possible Cause A power supply internal to the pack is not working properly. All thermocouple readings are suspect.

Solution Replace the I/O pack.

161

Description Reference Voltage out of limits

Possible Cause The reference voltage for the inputs is more than +/-5% beyond the expected value, indicating hardware failure.

Solution Replace the I/O pack.

163

Description Null Voltage out of limits

Possible Cause The Null voltage for the inputs is more than +/-5% beyond the expected value, indicating hardware failure.

Solution Replace the I/O pack.

224-236

Description Input Signal [ ] Voting Mismatch, Local=[ ], Voted=[ ]

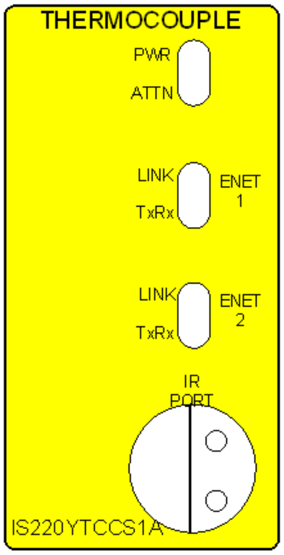
Possible Cause

- The specified input signal varies from the voted value of the signal by more than the **TMR_DiffLimt**.
- A problem exists with the input, either from the device, the wire to the terminal board, or the terminal board.

Solution

- Verify that **TMR_DiffLimt** is set to the proper value.
- Check the grounding of the connected inputs and terminal board.
- Reboot the I/O pack.
- Replace the I/O pack.
- Replace the terminal board.

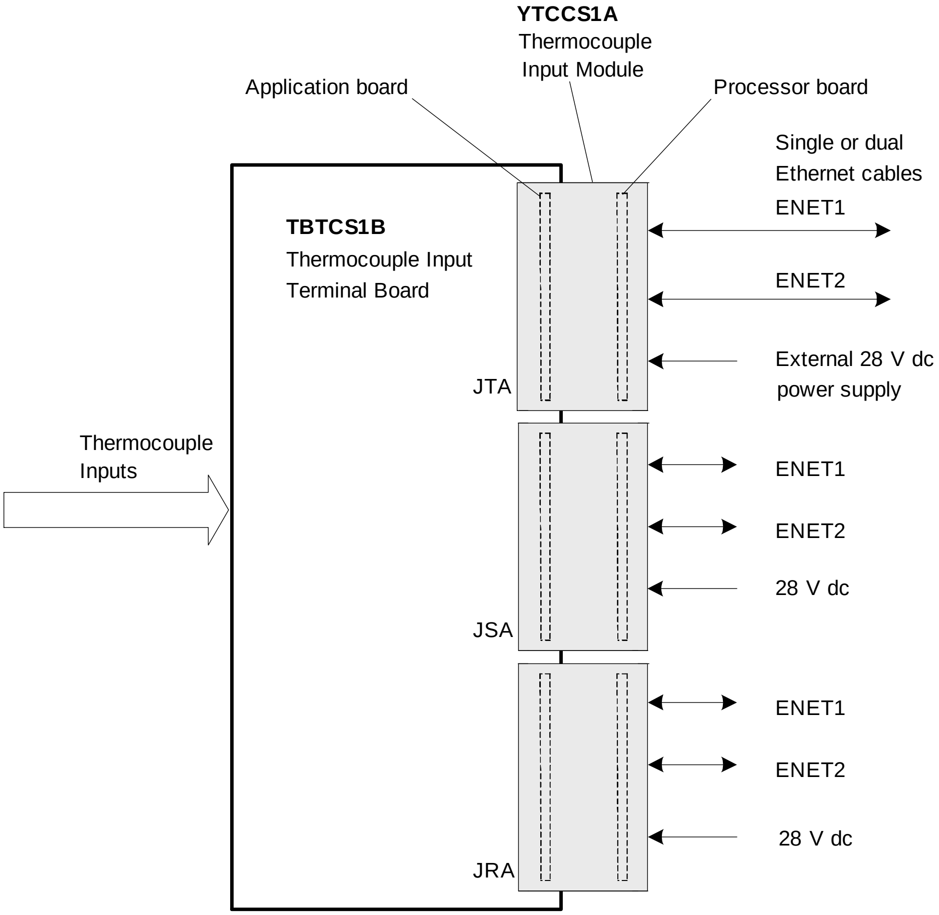
15.3 Mark VIeS YTCC Thermocouple Input Pack



Infrared Port Not Used

The Thermocouple Input (YTCC) pack provides the electrical interface between one or two I/O Ethernet networks and a thermocouple (TC) input terminal board. The YTCC contains a common processor board and an acquisition board specific to the thermocouple input function. The YTCC is capable of handling up to 12 thermocouple inputs. Two YTCCs can handle 24 inputs on the TBTCS1C terminal board. In the TMR configuration with the TBTCS1B terminal board, three YTCCs are used with three cold junctions, but only 12 thermocouples are available.

Input to the pack is through dual RJ-45 Ethernet connectors and a three-pin power input. Output is through a DC-37 pin connector that mates directly with the associated terminal board connector. Visual diagnostics are provided through indicator LEDs.



TMR Redundancy

15.3.1 Compatibility

The YTCC I/O pack is compatible with the TBTC and STTC terminal boards as listed in the following table.

Terminal Board	Thermocouple Inputs	Redundancy	YTCC I/O packs	Connectors
TBTCS1B	12	Simplex	1	Any
		TMR	3	JRA, JSA, JTA
TBTCS1C	12	Simplex	1	JA1
	24		2	JA1, JB1
STTCS1A (fixed) and S2A (pluggable)	12	Simplex	1	JA1

15.3.2 Installation

➢ **To install the YTCC pack**

1. Securely mount the desired terminal board.
2. Directly plug in the YTCC(s) to the terminal board connectors as listed in the section, *Compatibility*.
3. Mechanically secure the YTCC(s) using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right-angle force applied to the DC-37 connector between the pack and the terminal board. The adjustment should only be required once in the life of the product.
4. Plug in one or two Ethernet cables depending on the system configuration. The YTCC will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
5. Apply power to the YTCC by plugging in the connector on the side of the pack. It is not necessary to insert this connector with the power removed from the cable as the YTCC has inherent soft-start capability that controls current inrush on power application.
6. Use the ToolboxST application to configure the YTCC as necessary.

15.3.3 Operation

The following features are common to the safety I/O modules:

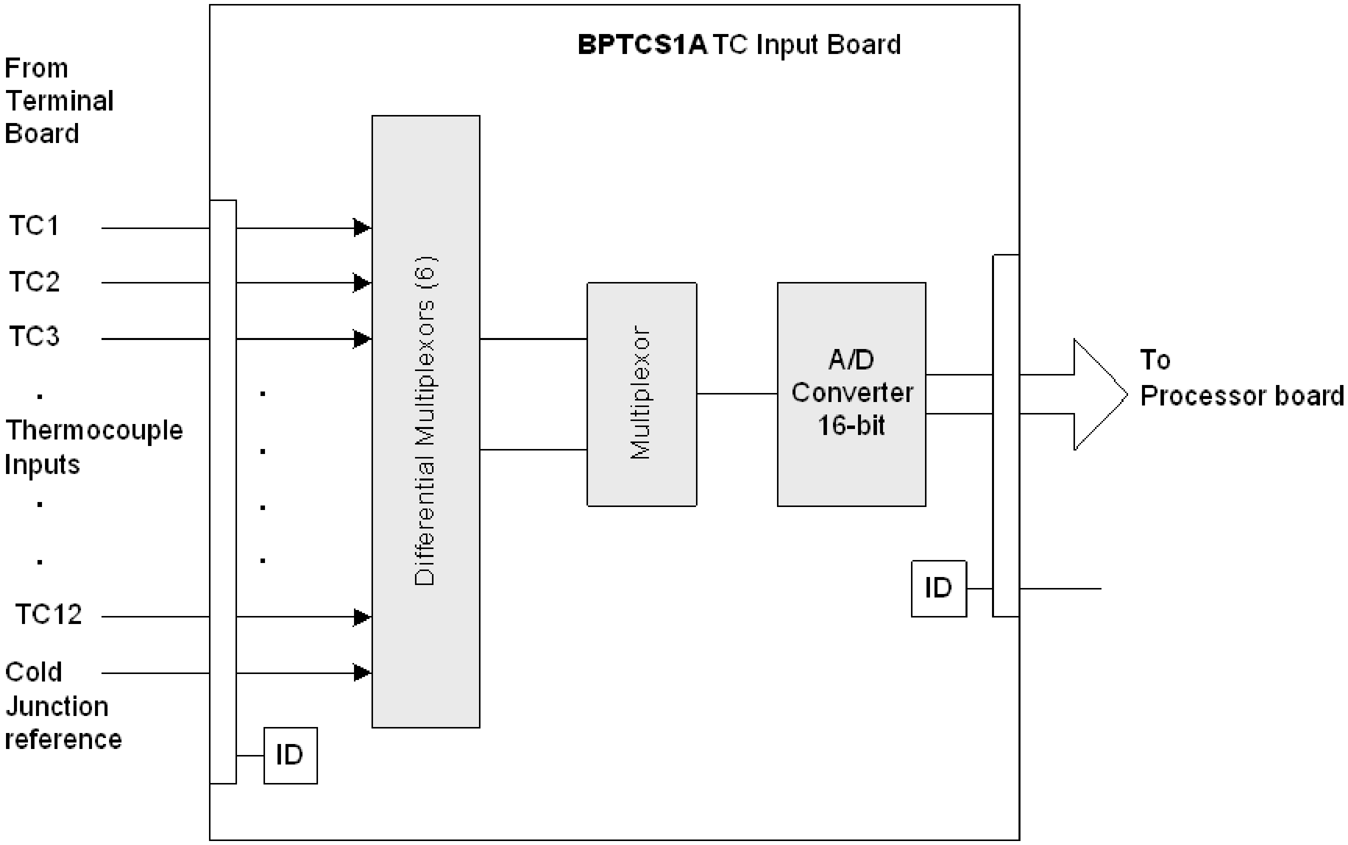
- *BPPx Processor Board*
- *Processor LEDs*
- *I/O Module Common Diagnostic Alarms*

15.3.3.1 YTCC Analog Input Hardware

The YTCC input board (BPTCS1A) accepts 12 signals at mV levels from the thermocouples wired to the terminal board. The analog input section consists of six differential multiplexers, a main multiplexer, and a 16-bit ADC that sends the digital data to the adjacent processor board. Each input has hardware and firmware filters, and the converter samples at up to 120 Hz.

Type E, J, K, S, and T thermocouples can be used, and they can be grounded or ungrounded. Thermocouples can be located up to 300 meters (984 feet) from the turbine I/O panel with a maximum two-way cable resistance of 450 Ω.

Linearization for individual thermocouple types is performed in software by the I/O pack board. A thermocouple, which is determined to be out of the hardware limits, is removed from the scanned inputs in order to prevent adverse affects on other input channels. If two packs are used, and both Cold Junction (CJ) devices are within the configurable limits, then the average of the two is used for CJ compensation.



15.3.3.2 YTCC Thermocouple Limits

Thermocouple inputs support a full-scale input range of -8.0 mV to + 45.0 mV. The following table displays typical input voltages for different thermocouple types versus minimum and maximum temperature range. It is assumed the cold junction temperature ranges from -30 to 65°C (-22 to 149 °F).

Thermocouple Type	E	J	K	S	T
Low range, °F	-60	-60	-60	0	-60
°C	-51	-51	-51	-17.78	-51
mV at low range with reference at 70°C (158 °F)	-7.174	-6.132	-4.779	-0.524	-4.764
High range, °F	1100	1400	2000	3200	750
°C	593	760	1093	1760	399
mV at high range with reference at 0°C (32 °F)	44.547	42.922	44.856	18.612	20.801

15.3.3.3 YTCC Cold Junctions

The CJ signals go into signal space and are available for monitoring. Normally the average of the two is used. Acceptable limits are configured, and if a CJ goes outside the limit, a logic signal is set. A 1 °F error in the CJ compensation will cause a 1°F error in the thermocouple reading. Refer to signals in the section, *YTCC Configuration*.

Hard-coded limits are set at -30 to 65 °C (-22 to 149 °F), and if a CJ goes outside these, it is regarded as faulted. Most CJ failures are open or short circuit. If the CJ is declared fault, the backup value is used, which can be derived from CJ readings on other terminal boards, or can be the configured default value.

15.3.4 Specifications

Item	YTCC Specification
Number of Channels	12 channels per I/O pack
Thermocouple Types	E, J, K, S, T thermocouples, and mV inputs
Span	-8 mV to +45 mV
A/D Converter	Sampling type 16-bit A/D converter
Cold Junction Compensation	Reference junction temperature measured in each module TMR board has three cold junction references
Cold Junction Temperature Accuracy	1.1ºC (2 ºF)
Conformity (Max Software) Error	0.14ºC (0.25 ºF)
Measurement Accuracy	53 microvolt (excluding cold junction reading). Example: For type K, at 1000 °F, including cold junction contribution, RSS error= 3 °F
Common Mode Rejection	AC CMR 110 dB 50/60 Hz, for balanced impedance input. Both hardware and firmware filtering
Common Mode Voltage	±5 volts
Normal Mode Rejection	Rejection of 250 mV rms at 50/60 Hz, ±5%, Both hardware and firmware filtering provides a total of 80 dB NMRR
Scan Time	All inputs are sampled at up to 120 times per second per input
Fault Detection	High/low (hardware) limit check High/low system (software) limit check Monitor readings from TCs, CJs, calibration voltages, and calibration zero readings
Ambient Rating for Enclosure Design†	-30 to 65°C (-22 to 149 °F)

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

15.3.5 Diagnostics

The I/O pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set.
- An internal precision voltage reference is used to continuously check A/D converter accuracy.

Details of the individual diagnostics are available in the ToolboxST application. The diagnostic signals can be individually latched, and then reset with the RESET_DIA signal if they go healthy.

Note Refer to the Common Safety Module, Processor LEDs section.

15.3.6 YTCC Configuration

Parameter	Description	Choices
Parameters		
SysFreq	System frequency (used for noise rejection)	50 or 60 Hz
SystemLimits	Allows user to temporarily disable all system limit checks for testing purposes. Setting this parameter to Disable will cause a diagnostic alarm to occur.	Enable, Disable
Auto Reset	Automatic restoring of thermocouples removed from scan	Enable, Disable
Thermocouples		
ThermCplType	Select thermocouples type or mV input Unused inputs are removed from scanning, mV inputs are primarily for maintenance, but can also be used for custom remote CJ compensation. Standard remote CJ compensation also available.	Unused, mV, T,K,J, E, or S
ThermCplUnit	Select thermocouples display unit in °C or °F. This value needs to match units of attached variable. The ThermCplUnit parameter affects the native units of the controller application variable. It is only indirectly related to the tray icon and associated unit switching capability of the HMI. This parameter should not be used to switch the display units of the HMI. **Caution** **Do not change the ThermCplUnit parameter because these changes will require corresponding changes to application code and to the Format Specifications or units of the connected variable. This parameter modifies the actual value sent to the controller as seen by application code. Application code that is written to expect degrees Fahrenheit will not work correctly if this setting is changed. External devices, such as HMIs and Historians, may also be affected by changes to this parameter**	deg_F, deg_C
LowPassFiltr	Enable 2 Hz low pass filter	Enable, Disable
SysLimit1	System Limit 1 in °C, °F, or mV	-60 to 3500 (FLOAT)
SysLim1Enabl	Enable system limit 1 fault check, a temperature limit which can be used to create an alarm.	Enable, Disable
SysLim1Latch	Latch system limit 1 fault Determines whether the limit condition will latch or unlatch; reset used to unlatch	NotLatch, Latch
SysLim1Type	System limit 1 check type limit occurs when the temperature is greater than or equal (≥), or less than or equal to (≤) a preset value	≥ or ≤
SysLimit2	System Limit 2 in °C, °F, or mV	-60 to 3500 (FLOAT)
SysLim2Enabl	Enable system limit 2 fault check, a temperature limit which can be used to create an alarm.	Enable, Disable

Parameter	Description	Choices
SysLim2Latch	Latch system limit 2 fault Determines whether the limit condition will latch or unlatch; reset used to unlatch System limit 2 check type limit occurs when the temperature is greater than or equal (≥), or less than or equal to (≤) a preset value	NotLatch, Latch
SysLim2Type	System limit 2 check type limit occurs when the temperature is greater than or equal (≥), or less than or equal to (≤), a preset value	≥ or ≤
TMR_DiffLimt	Diagnostic limit, TMR input vote difference in engineering units Limit condition occurs if three temperatures in R, S, T differ by more than a preset value (engineering units); this creates a voting alarm condition.	-60 to 3500 (FLOAT)

15.3.6.1 YTCC Cold Junctions

Cold junctions are similar to thermocouples but without low pass filters.

Cold Junction Name	Cold Junction Description	Choices
ColdJuncType	Select CJ Type	Remote, Local
ColdJuncUnit	Select TC Display Unit Deg °C or °F. Value needs to match units of attached variable	Deg_F, Deg_C
SysLimit1	System Limit 1 - Deg °F or Deg °C	-40 to 185 (FLOAT)
SysLim1Enabl	Enable System Limit 1 Fault Check	Disable, Enable
SysLim1Latch	Latch System Limit 1 Fault	NotLatch, Latch
SysLim1Type	System Limit 1 Check Type (≥ or ≤)	≥ or ≤
SysLimit2	System Limit 2 - Deg °F or Deg °C	-40 to 185 (FLOAT)
SysLim2Enabl	Enable System Limit 2 Fault Check	Disable, Enable
SysLim2Latch	Latch System Limit 2 Fault	NotLatch, Latch
SysLim2Type	System Limit 2 Check Type (≥ or ≤)	≥ or ≤
TMR_DiffLimt	Diag Limit, TMR Input Vote Difference, in Eng Units	-60 to 3500 (FLOAT)

15.3.6.2 YTCC Variables

I/O Points (Signals)

Points (Signals)	Description - Point Edit (Enter Signal Connection Name)	Direction	Type
L3DIAG_YTCC	I/O diagnostic indication	Input	BIT
LINK_OK_YTCC	I/O link okay indication	Input	BIT
ATTN_YTCC	I/O attention indication	Input	BIT
IOPackTmpr	I/O pack temperature	Input	FLOAT
SysLim1TC1	System limit 1 for thermocouple 1	Input	BIT
:	:	Input	BIT
SysLim1TC12	System limit 1 for thermocouple 12	Input	BIT
SysLim1CJ1	System limit 1 for cold junction	Input	BIT
SysLim2JC1	System limit 2 for cold junction	Input	BIT
SysLim2TC1	System limit 2 for thermocouple 1	Input	BIT
:	:	Input	BIT
SysLim2TC12	System limit 2 for thermocouple 12	Input	BIT
CJBackup	Cold junction backup	Output	FLOAT
CJRemote1	Cold junction remote	Output	FLOAT
Thermocouple01	Thermocouple reading	Output	FLOAT
:	:	Output	FLOAT
Thermocouple12	Thermocouple reading	Output	FLOAT
ColdJunction1	Cold junction for TCs 1-12	Output	FLOAT

15.4 YTCC Specific Alarms

32-43

Description Thermocouple [ ] raw counts high

Possible Cause Thermocouple millivolt input to the analog-to-digital converter exceeded the converter limits and will be removed from the scan.

Solution

- Check field wiring, including shields.
- Check installation of the I/O pack on the terminal board. Problem is usually not a I/O pack or terminal board failure if other thermocouples are working correctly.

56-67

Description Thermocouple [ ] Raw Counts Low

80

Description Cold junction 1 raw counts high

Possible Cause Cold junction input to the analog-to-digital converter exceeded the limits of the converter. If a cold junctions fails, the **CJ_Backup** strong value is used.

Solution

- Check the mounting of the I/O pack on the terminal board.
- Replace the terminal board.
- Replace the I/O pack.

82

Description Cold Junction 1 raw counts low

Possible Cause Cold junction input to the analog-to-digital converter exceeded the limits of the converter. If a cold junctions fails, the **CJ_Backup** strong value is used.

Solution

- Check the mounting of the I/O pack on the terminal board.
- Replace the terminal board.
- Replace the I/O pack.

84

Description Calibration reference 1 raw counts high.

Possible Cause With each scan, the I/O pack uses the internal analog-to-digital converter to read a precision voltage reference. This reference input exceeded the converter specified limits, indicating a hardware fault.

Solution The precision reference voltage, signal multiplexing, or analog-to-digital converter in the I/O pack failed. Replace the pack.

86

Description Calibration reference 1 raw counts Low.

Possible Cause With each scan, the I/O pack uses the internal analog-to-digital converter to read a precision voltage reference. This reference input exceeded the converter specified limits, indicating a hardware fault.

Solution The precision reference voltage, signal multiplexing, or analog-to-digital converter in the I/O pack failed. Replace the pack.

88

Description Null reference 1 raw counts high

Possible Cause With each scan, the I/O pack uses the internal analog/digital converter to read a zero voltage reference. This reference input exceeded the converter specified limits, indicating a hardware fault.

Solution The signal multiplexing or analog-to-digital converter on the I/O pack failed. Replace the pack.

90

Description Null Reference 1 Raw Counts Low

Possible Cause With each scan, the I/O pack uses the internal analog/digital converter to read a zero voltage reference. This reference input exceeded the converter specified limits, indicating a hardware fault.

Solution The signal multiplexing or analog-to-digital converter on the I/O pack failed. Replace the pack.

92-103

Description Thermocouple [ ] Linearization Table High

Possible Cause

- Thermocouple mV input exceeded range of linearization (lookup) table for this TC type. Refer to documentation for specified thermocouple ranges.
- Thermocouple configured as wrong type.
- Board detected a thermocouple open, applied bias to circuit, driving it to a large negative number.
- Stray voltage or noise caused the input to exceed its range.

Solution

- Check field wiring, including shields.
- Check thermocouple for open circuit.
- Verify that the thermocouple type matches the configuration.
- Measure incoming mV signal and verify that it is within the specified thermocouple range.

116-127

Description

Possible Cause

- Thermocouple mV input exceeded range of linearization (lookup) table for this TC type. Refer to documentation for specified thermocouple ranges.
- Thermocouple configured as wrong type.
- Board detected a thermocouple open, applied bias to circuit, driving it to a large negative number.
- Stray voltage or noise caused the input to exceed its range.

Solution

- Check field wiring, including shields.
- Check thermocouple for open circuit.
- Verify that the thermocouple type matches the configuration.
- Measure incoming mV signal and verify that it is within the specified thermocouple range.

160

Description Internal pack power supply not OK

Possible Cause A power supply internal to the pack is not working properly. All thermocouple readings are suspect.

Solution Replace the pack.

161

Description Reference Voltage out of limits

Possible Cause The reference voltage for the inputs is more than ±5% beyond the expected value, indicating hardware failure.

Solution Replace the pack.

163

Description Null Voltage out of limits

Possible Cause The Null voltage for the inputs is more than ±5% beyond the expected value, indicating hardware failure.

Solution Replace the pack.

128

Description Logic Signal [ ] Voting Mismatch

Possible Cause N/A

Solution N/A

224–236

Description Input Signal [ ] Voting Mismatch, Local=[ ], Voted=[ ]

Possible Cause

- The specified input signal varies from the voted value of the signal by more than the **TMR_DiffLimt**.
- A problem exists with the input, either from the device, the wire to the terminal board, or the terminal board.

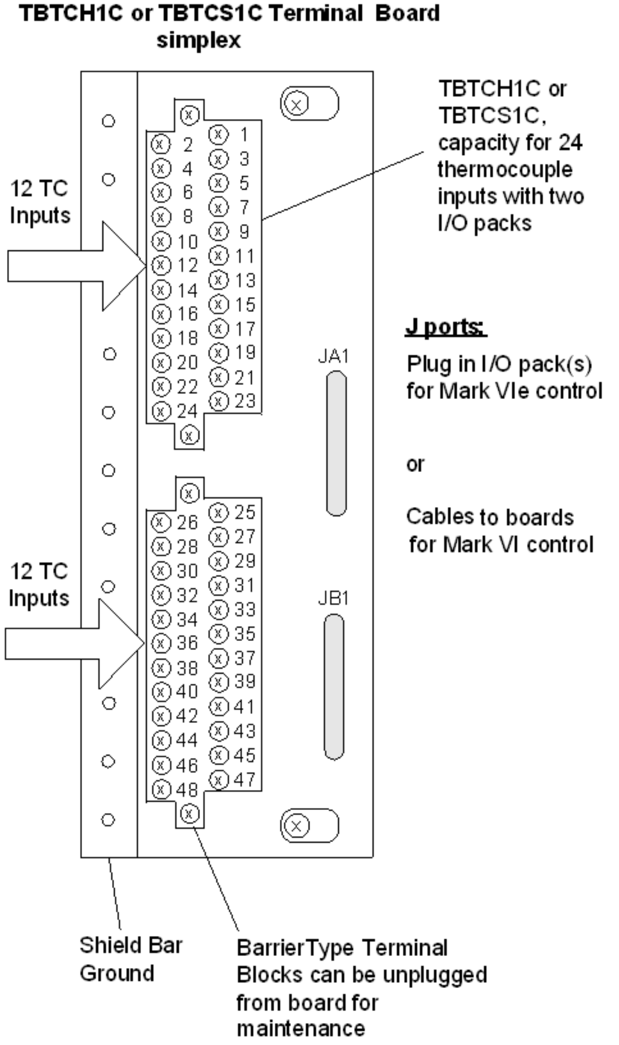
Solution

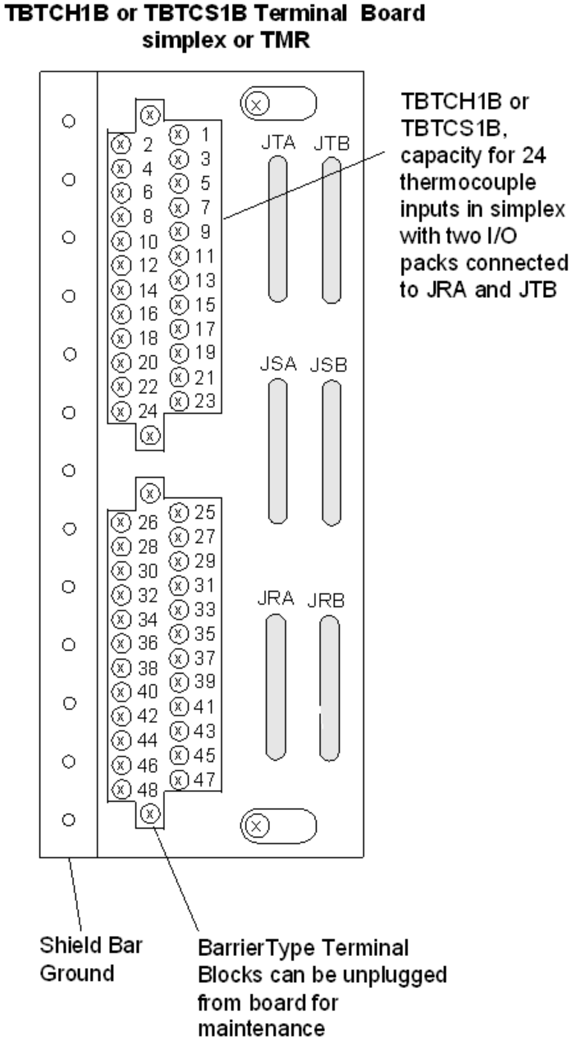
- Verify that **TMR_DiffLimt** is set to the proper value.
- Check the grounding of the connected inputs and terminal board.
- Reboot the pack.

15.5 TBTCH1B, H1C, S1B, S1C Thermocouple Input

The Thermocouple Input (TBTC) terminal board accepts 24 type E, J, K, S, or T thermocouple inputs. It accepts additional B, N, and R types of thermocouple inputs only when used with PTCCH2A or PTCCH2B in the Mark VIe control system. These inputs are wired to two barrier-type blocks on the terminal board. TBTC communicates with the I/O pack through dc-type connectors. Two types of the TBTC are available, as follows:

- TBTC_1C for simplex applications has two dc-type connectors
- TBTC_1B for simplex and TMR applications has six dc-type connectors


TBTCH1C or TBTCS1C Terminal Board
simplex
12 TC Inputs
12 TC Inputs
2 4 6 8 10 12 14 16 18 20 22 24
1 3 5 7 9 11 13 15 17 19 21 23
26 28 30 32 34 36 38 40 42 44 46 48
25 27 29 31 33 35 37 39 41 43 45 47
JA1
JB1
TBTCH1C or TBTCS1C, capacity for 24 thermocouple inputs with two I/O packs
J ports:
Plug in I/O pack(s) for Mark VIe control
or
Cables to boards for Mark VI control
Shield Bar Ground
BarrierType Terminal Blocks can be unplugged from board for maintenance


TBTCH1B or TBTCS1B Terminal Board
simplex or TMR
2 4 6 8 10 12 14 16 18 20 22 24
1 3 5 7 9 11 13 15 17 19 21 23
26 28 30 32 34 36 38 40 42 44 46 48
25 27 29 31 33 35 37 39 41 43 45 47
JTA
JTB
JSA
JSB
JRA
JRB
TBTCH1B or TBTCS1B, capacity for 24 thermocouple inputs in simplex with two I/O packs connected to JRA and JTB
Shield Bar Ground
BarrierType Terminal Blocks can be unplugged from board for maintenance

15.5.1 Compatibility

Terminal Board	Redundancy and # of TCs
TBTCH1B TBTCS1B†	Simplex, one I/O pack: 12 thermocouple inputs Simplex, two I/O packs: 24 thermocouple inputs TMR, three I/O packs: 12 thermocouple inputs
TBTCH1C TBTCS1C†	Simplex, one I/O pack: 12 thermocouple inputs Simplex, two I/O packs: 24 thermocouple inputs
† IEC 61508 safety certified with Mark VIeS YTCC	

I/O Pack	TC Types
Mark VIe PTCCH1A, H1BMark VIeS YTCCS1A	E, J, K, S, or T thermocouple inputs
Mark VIe PTCCH2A, H2B	E, J, K, S, T, B, N, or R thermocouple inputs.

15.5.2 Installation

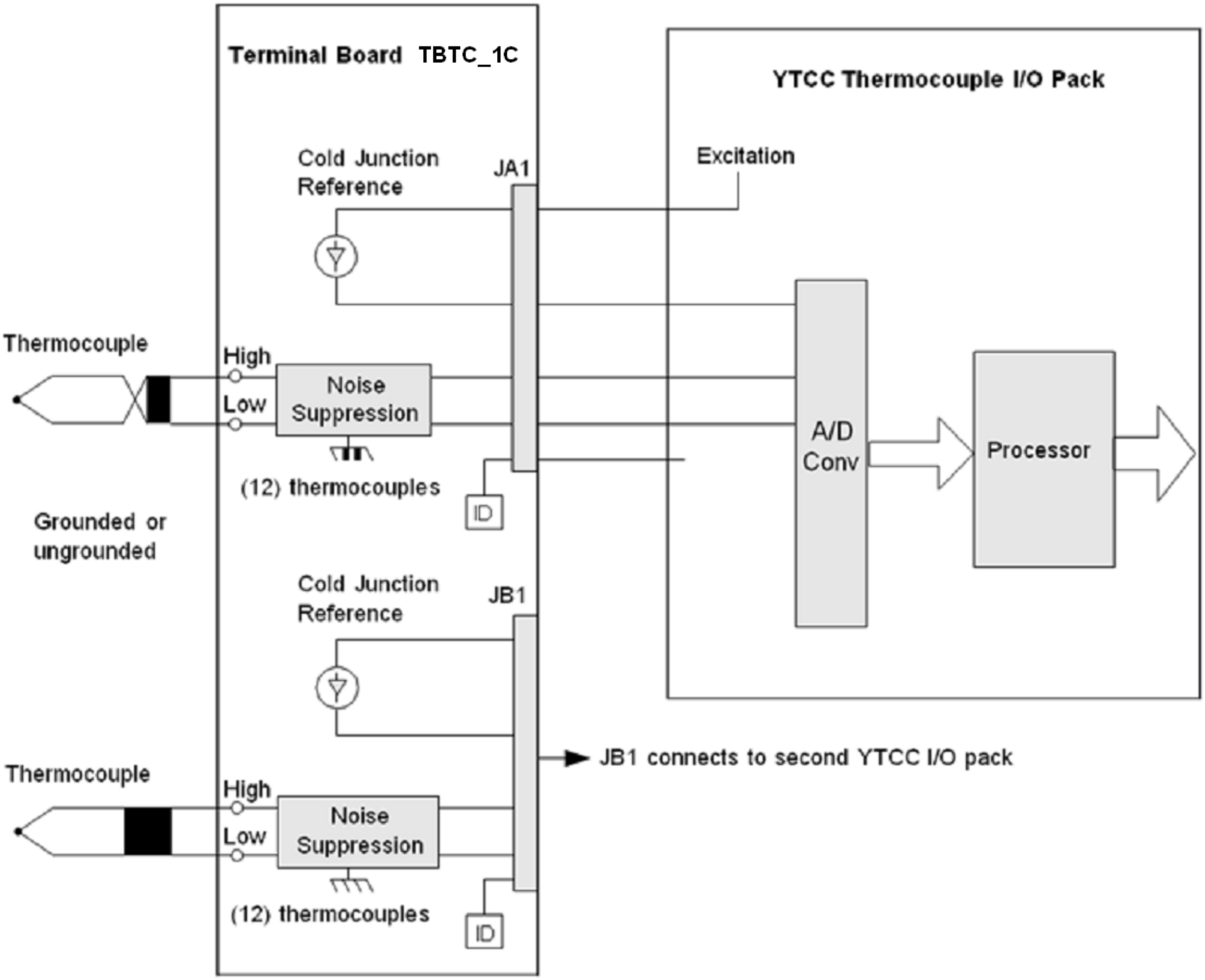
Connect the thermocouple wires directly to the two I/O terminal blocks. These removable blocks are mounted on the terminal board and held down with two screws. Each block has 24 terminals accepting up to #12 AWG wires.

A shield terminal strip attached to chassis ground is located on the left side of each terminal block. Plug the I/O packs directly into the TBTC J-type connectors. The number of cables or I/O packs depends on the level of redundancy required.

15.5.3 Operation

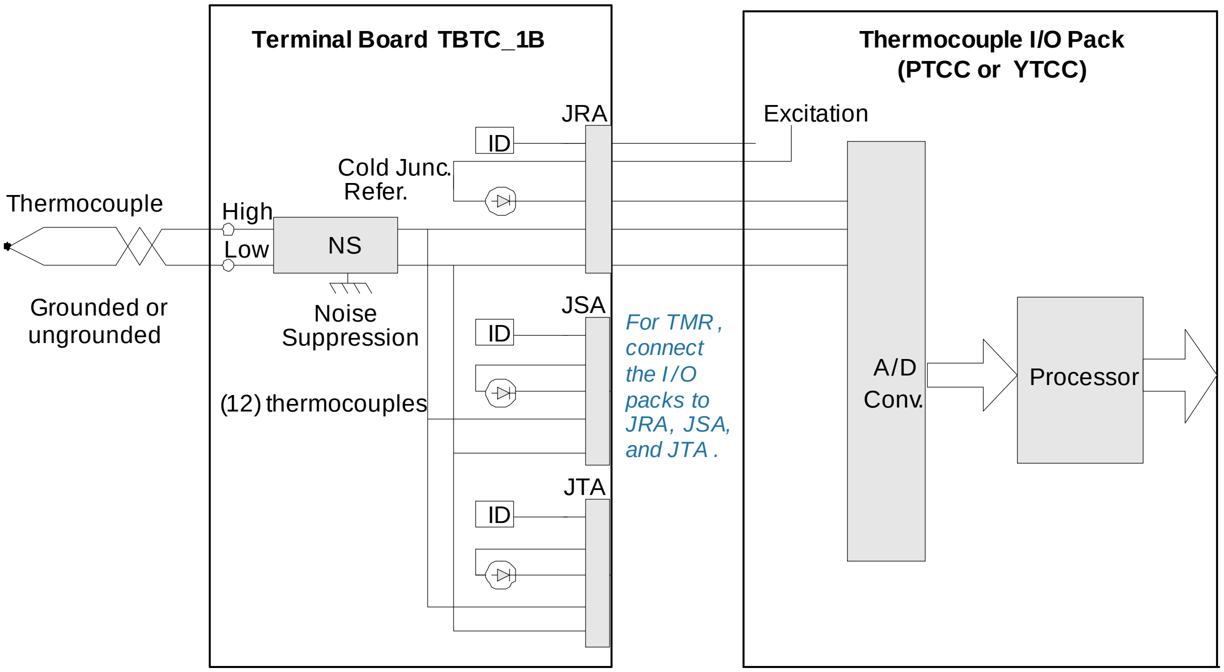
15.5.3.1 Simplex

For simplex systems, two I/O packs plug into TBTC_1C, obtaining 24 thermocouple inputs.



15.5.3.2 TMR

For TMR redundancy using TBTC_1B, the 12 thermocouple signals fan out to three I/O packs.



Twelve Thermocouple Inputs with TMR Redundancy

15.5.3.3 Thermocouple Limits

Thermocouple inputs support full-scale input ranges. The following tables display typical input voltages for different thermocouple types versus the minimum and maximum temperature range. Cold junction (CJ) temperature ranges are assumed to be from -30 to 65°C (-22 to 149 °F).

TBTC_1B and TBTC_1C Limits

Limits	E	J	K	S	T
Low range, °F	-60	-60	-60	0	-60
°C	-51	-51	-51	-17.78	-51
mV at low range with reference at 70°C (158 °F)	-7.174	-6.132	-4.779	-0.524	-4.764
High range, °F	1100	1400	2000	3200	750
°C	593	760	1093	1760	399
mV at high range with reference at 0°C (32 °F)	44.547	42.922	44.856	18.612	20.801

TBTC Limits with Mark VIe PTCCH2A, H2B

Limits	B	E	J	K	N	R	S	T
Low range, °F	32	-60	-60	-60	-60	0	0	-60
°C	0	-51	-51	-51	-51	-17.78	-17.78	-51
mV at low range with reference at 70°C (158 °F)	-0.0114	-7.174	-6.132	-4.779	-3.195	-0.512	-0.524	-4.764
High range, °F	3272	1832	2192	2372	2282	3092	3200	752
°C	1800	1000	1200	1300	1250	1700	1760	400
mV at high range with reference at 0°C (32 °F)	13.593	76.373	69.553	52.41	45.694	20.220	18.612	20.869

15.5.3.4 Cold Junctions

The CJ signals go into signal space and are available for monitoring. Acceptable limits are configured, and if a CJ goes outside the limit, a logic signal is set. A 1 °F error in the CJ compensation will cause a 1 °F error in the thermocouple reading.

Hard-coded limits are set at -50 to 85°C (-58 to 185 ºF), and if a CJ goes outside this, it is regarded as bad. Most CJ failures are open or short circuit. If the CJ is declared bad, the backup value is used. This backup value can be derived from CJ readings on other terminal boards, or can be the configured default value.

15.5.4 Specifications

Item	TBTC Specification
Number of Channels	24 channels per terminal board
Thermocouple Types	E, J, K, S, T thermocouples, and mV inputs if TBTC is connected to PTCCH1A, PTCCH1B, or YTCCS1A. E, J, K, S, T, B, N, R thermocouples, and mV inputs if TBTC is connected to PTCCH2A or PTCCH2B ***B, N and R types of thermocouples should only be selected if using PTCCH2A or PTCCH2B***
Span	-8 mV to 45 mV if TBTC is connected to PTCCH1A, PTCCH1B, or YTCCS1A -20 mV to 95 mV if TBTC is connected to PTCCH2A or PTCCH2B
Cold Junction Compensation	Reference junction temperature measured at two locations on each H1C / S1C terminal board. TMR H1B or S1B boards have six CJ references. Only three are available with I/O packs.
Cold Junction Temperature Accuracy	CJ accuracy 1.1ºC (2 ºF)
Fault Detection	High/low (hardware) limit check Monitor readings from all TCs, CJs, calibration voltages, and calibration zero readings.

15.5.5 Diagnostics

Diagnostic tests to components on the terminal boards are as follows:

- Each thermocouple type has hardware-limit checking (HLC) based on preset (non-configurable) high and low levels set near the ends of the operating range. If this limit is exceeded, a logic signal is set and the input is no longer scanned. If any one of the inputs hardware limits is set, it creates a composite diagnostic alarm.
- Each terminal board connector has its own ID device that is interrogated by the I/O pack. The terminal board ID is coded into a read-only chip containing the terminal board serial number, board type, revision number, and the J connector location. If a mismatch is encountered, a hardware incompatibility fault is created.
- When operating with the I/O pack, a very small current is injected into each thermocouple path. This is done to detect open circuits and is of a polarity to create a low temperature reading should a thermocouple open.

15.6 STTCH#A, S#A Simplex Thermocouple Input

The Simplex Thermocouple Input (STTC) terminal board is a compact terminal board designed for DIN-rail or flat mounting. The board has 12 thermocouple inputs and connects to the thermocouple I/O pack. The on-board signal conditioning and cold junction reference is identical to those on the larger TBTC board. An on-board ID chip identifies the board to the I/O pack for system diagnostic purposes.

Two types of Euro-block terminal blocks are available as follows:

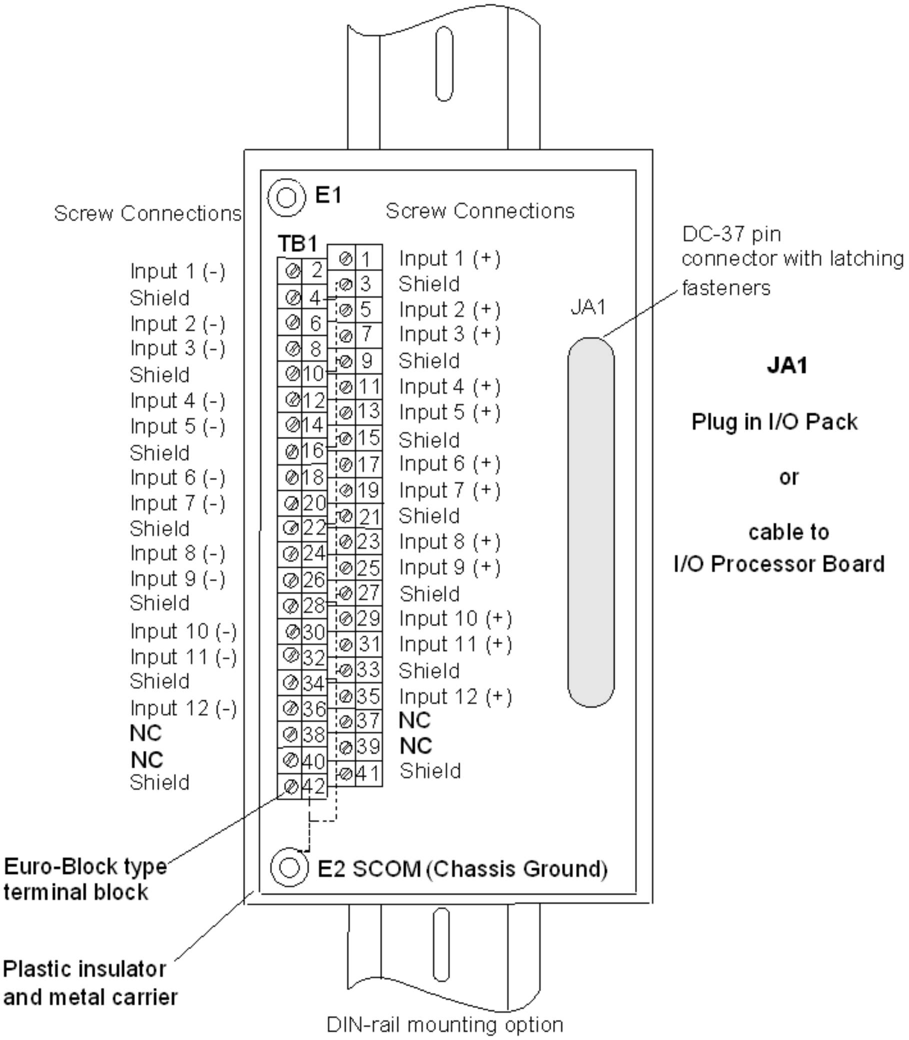
- Terminal boards STTCH1A and STTCS1A have a permanently mounted terminal block with 42 terminals.
- Terminal board STTCH2A and STTCS2A have a right-angle header accepting a range of commercially available removeable terminal blocks, with a total of 42 terminals.

Compatibility

Board Revision	Mark VIe Control IS220PTCC	Mark VIeS Safety Control IS200YTCC	Comments
STTCH1A	Yes	No	Euro-block fixed terminals
STTCH2A		No	Euro-block removable terminals
STTCS1A		Yes	Fixed terminals, IEC 61508 safety certified with Mark VIeS YTCC
STTCS2A			Removable terminals, IEC 61508 safety certified with Mark VIeS YTCC

15.6.1 Installation

The STTC and a plastic insulator mount on a sheet metal carrier, which mounts on a DIN rail. The STTC and insulator mount on a sheet metal assembly that bolts directly in a panel. Thermocouples are wired directly to the terminal block using typical #18 AWG wires. Shield screws are internally connected to SCOM. Shields should be terminated on designated terminals on TB1.

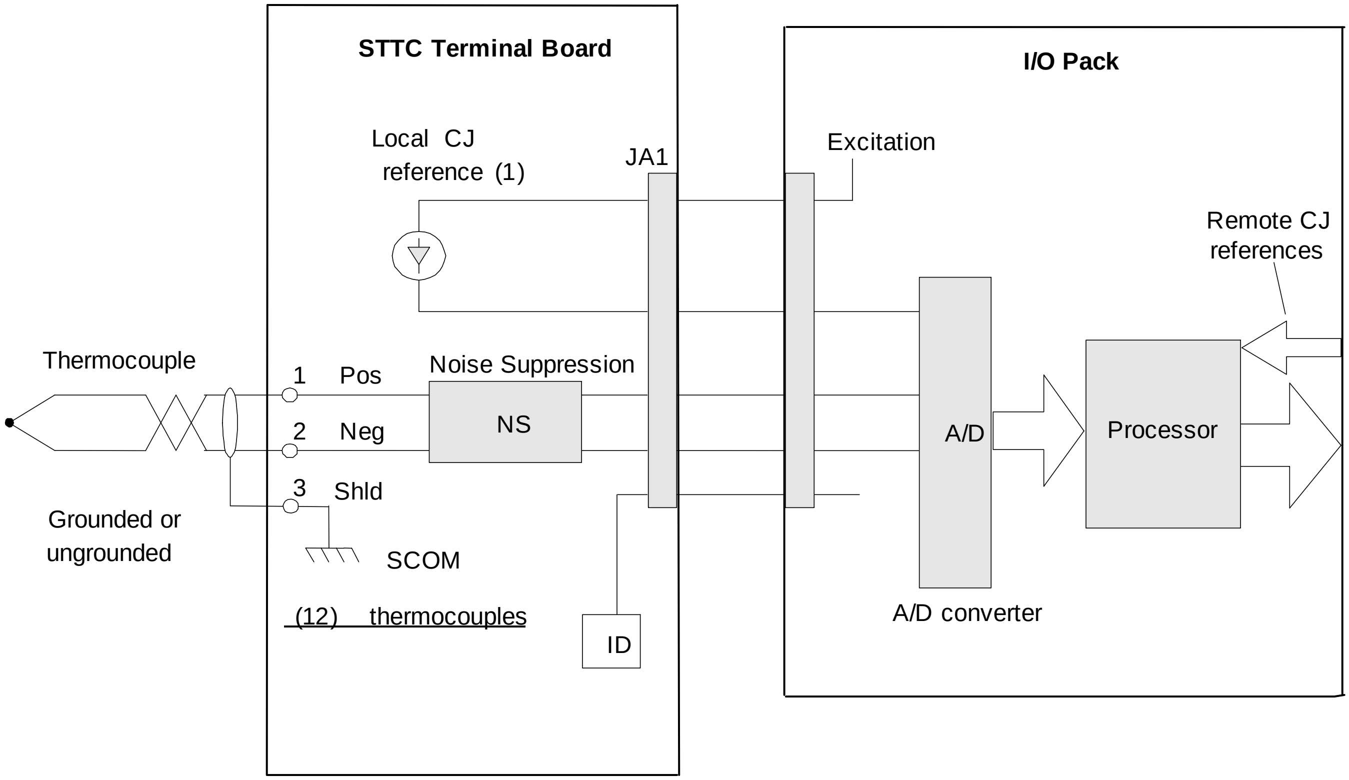


STTC Thermocouple Terminal Board

Note E1 and E2 are holes for chassis grounding screws.

15.6.2 Operation

The connection from the STTC to the I/O pack containing the A/D converter is displayed in the following figure. The I/O pack provides excitation for the cold junction (CJ) reference on the terminal board. The 12 thermocouple signals plus the CJ signal and the connection to the identity chip (ID) come through connector JA1.



15.6.3 Specifications

Item	STTC Specification
Number of Channels	12 channels per terminal board
Thermocouple Types	E, J, K, S, T thermocouples, and mV inputs if STTC is connected to PTCCH1A, PTCCH1B, or YTCCS1A E, J, K, S, T, B, N, R thermocouples, and mV inputs if STTC is connected to PTCCH2A or PTCCH2B ***B, N and R types of thermocouples should only be selected if PTCCH2A or PTCCH2B is used.***
Span	-8 mV to 45 mV if STTC is connected to PTCCH1A, PTCCH1B, or YTCCS1A -20 mV to 95 mV if STTC is connected to PTCCH2A or PTCCH2B
Cold Junction Compensation	Reference junction temperature measured at one location
Cold Junction Temperature Accuracy	Over the Celsius operating range: 1.1°C Over the Fahrenheit operating range: 2 °F
Fault Detection	High/low (hardware) limit check Check ID chip on JA1 connector

15.6.4 Diagnostics

Diagnostic tests to components on the terminal boards are as follows:

- Each thermocouple type has hardware-limit checking based on preset (non-configurable) high and low levels set near the ends of the operating range. If this limit is exceeded, a logic signal is set and the input is no longer scanned. If any one of the inputs hardware limits is set, it creates a composite diagnostic alarm.
- Each terminal board connector has its own ID device that is interrogated by the I/O pack. The board ID is coded into a read-only chip containing the terminal board serial number, board type, revision number, and the J connector location. If a mismatch is encountered, a hardware incompatibility fault is created.
- When operating with the I/O pack a very small current is injected into each thermocouple path. This is done to detect open circuits and is of a polarity to create a low temperature reading should a thermocouple open.

Notes

16 PVIB, YVIB Vibration Monitor Modules

16.1 Vibration Monitoring Overview

16.1.1 Mechanical Vibration Standards

ISO 7919-4:2009 provides the standard for evaluation of machine vibration by measurements on the rotating shafts. The broad-band vibration is measured radially or transverse to the shaft axis of the Heavy Duty Gas Turbines (HDGTs) with fluid-film bearings. The frequency range is from one hertz to three times the maximum normal operating frequency. Eddy-current transducers are located orthogonal to each other, pointed radially at the shaft. Traditionally, either narrow-band or spectral analysis is used to monitor the mechanical vibration. The typical peak-to-peak, relative-vibration displacement values for a newly commissioned 3600 rpm machine is 3.15 mils.

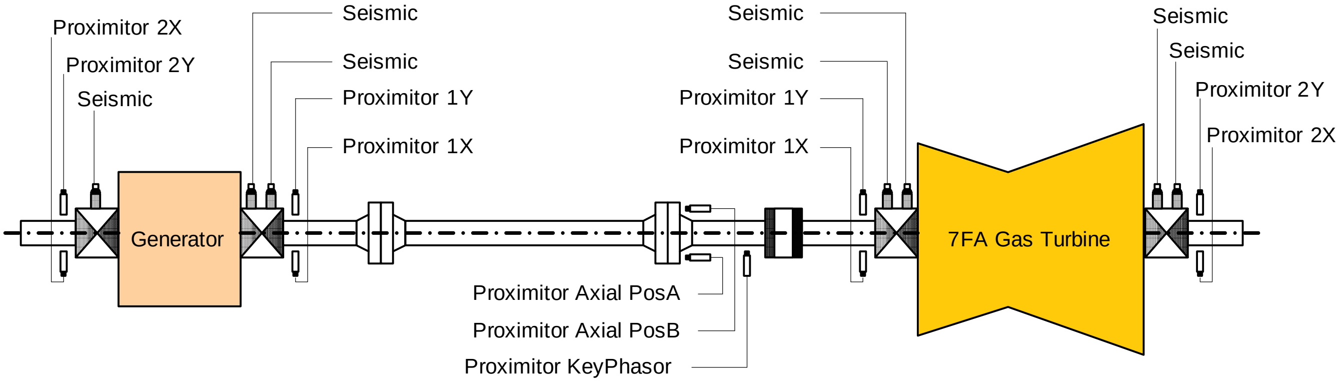
ISO 10816-4:2009 defines a standard for the evaluation of machine vibration by measurements on the non-rotating parts. The broad-band vibration is measured radially or transverse to the shaft axis on all main bearing housings or pedestals and in the axial direction on thrust bearings. The measurement system must be capable of measuring broad-band vibration over a frequency range from 10 hertz to at least 500 hertz or six times the maximum normal operating frequency, whichever is greater. The common measurement parameter for assessing machine vibration severity is the broad-band root mean square (r. m.s.) velocity measurement. The vibration consists mainly of one frequency component, which is the rotating frequency. Typical values for bearing housing or pedestal vibration velocity for a newly commissioned gas turbines is 0.177 inches / sec.

16.1.2 Heavy-duty Gas Turbine (HDGT) Vibration Monitoring

The 7FA diagram is representative of most HDGT installations driving a generator. Journal or fluid-film bearing vibration, eccentricity, and rotor expansion are monitored with eddy-current sensors (Proximitors*****). These sensors are radially mounted with respect to the shaft axis, and are used for monitoring shaft movement on both sets of generator bearings and both sets of gas turbine bearings.

The Mark VIe Vibration Module, PVIB or the Safety version, YVIB use the signal feedback from the sensors to provide the following:

- Gap or relative distance between the shaft surface and the eddy-current head
- Broad-band peak-to-peak changes in shaft position relative to the sensor
- Vibration magnitude 1X rotating at shaft rpm and location relative to Keyphasor*****
- Vibration magnitude 2X rotating at twice shaft rpm and location relative to Keyphasor



Two eddy-current sensors (Proximitors) monitor the differential expansion in the shafts longitudinal direction that is caused by generator and turbine loading. The YVIB or PVIB provides position information for the user.

A single eddy-current sensor (Proximitor) is used to monitor the key slot or the actual key in the shaft. The once per revolution key slot / pedestal provides the reference point for the Vibration 1X/2X magnitudes. The YVIB or PVIB also uses the Keyphasor input to calculate the shaft rotation speed in rpm.

Seismic sensors are mounted to the generator and gas turbine bearing housings or pedestals. One is mounted on the non-load side of the generator and two are mounted on the load side. Two seismic sensors are mounted on both sides of the gas turbine. The seismic sensors are mounted on the bearing housing to sense the radial vibration caused by the rotating shaft or any bearing issues. With firmware version 5.01 or later and Enhanced mode enabled, the YVIB or PVIB monitors the seismic sensors to provide the root mean square (RMS) velocity measurement of the bearing housing. Legacy mode uses ½*Pk-Pk for this function.

16.1.3 Land Marine Gas Turbines (LMGTs) Vibration Monitoring

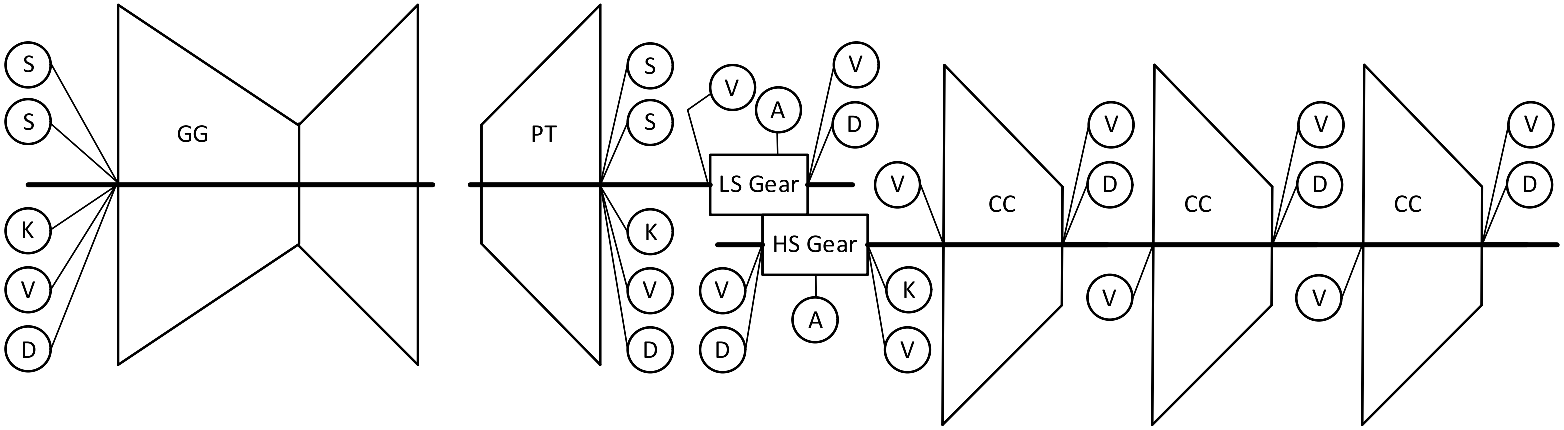
LM gas turbines are applied in the Oil & Gas industry for driving compressors in transporting gas down pipelines and power generation. The YVIB Safety and PVIB vibration IO modules are approved for use with the LM2500 SAC and LM2500 DLE gas turbine vibration applications.

LM applications use accelerometers mounted to the case of the compressor rear frame and the power turbine frame. The acceleration signal is integrated and filtered in a charge amplifier provided external to the Mark VIe Vibration product. The integrated acceleration or velocity signal is monitored by the YVIB (safety version) or PVIB Vibration I/O module. For this application, a broad-band root mean square (RMS) velocity measurement from the sensors is required, as well as monitoring of compressor and power turbine vibration components at a defined shaft frequency, using tracking filters and customer-supplied RPM feedback signals from controller blockware/application code.

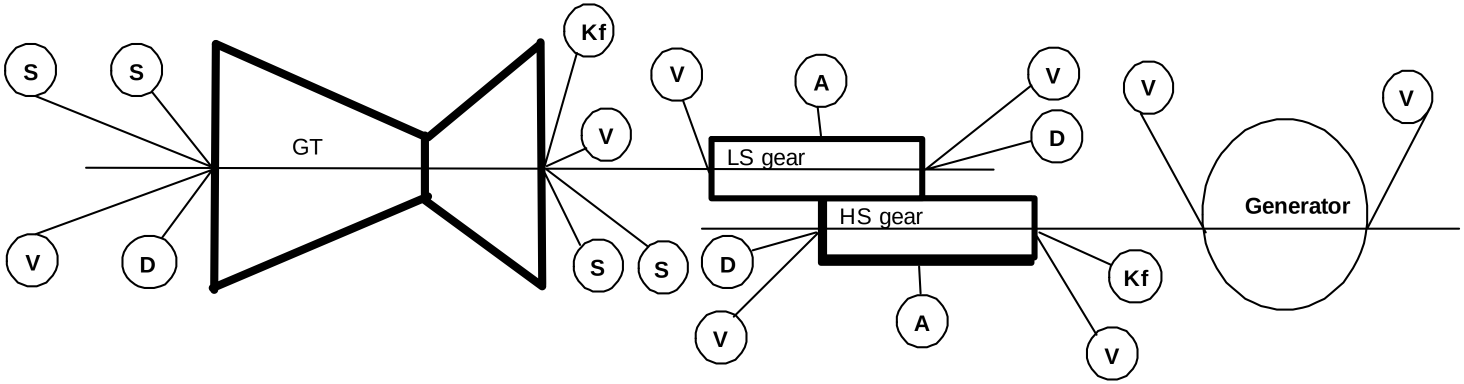
Index for Application Diagrams

Sensor Tag	Measure	Sensor Type	Prox. Type	Function	Sensor Filter Capability
S	Seismic vibration	Metrix 5486C-008	na	Monitoring & Protection	10 – 1000 Hz
V	X-Y radial vibration	Bently Nevada 330101	Bently Nevada	Monitoring & Protection	5 – 1200 Hz
		(3300 XL 8mm probe)	330100		
			(3300 Proximity transducer)		
D	Dual axial displacement	Bently Nevada 330101	Bently Nevada	Monitoring & Protection	na
		(3300 XL 8mm probe)	330100		
			(3300 Proximity transducer)		
A	Accelerometer	Bently Nevada	na	Monitoring	10 – 20000 Hz
		330400-01-05			
Kf	KeyPhasor	Bently Nevada 330101	Bently Nevada	Monitoring	na
		(3300 XL 8mm probe)	330100		
			(3300 Proximity transducer)		

Use the table on the previous page to decode the letters within the following figures.

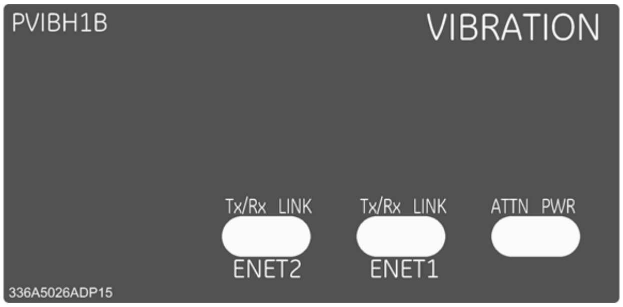


Two Shaft Gas Turbine Mechanical Drive Application Max Case



Single Shaft Gas Turbine Generator Drive Application Max Case

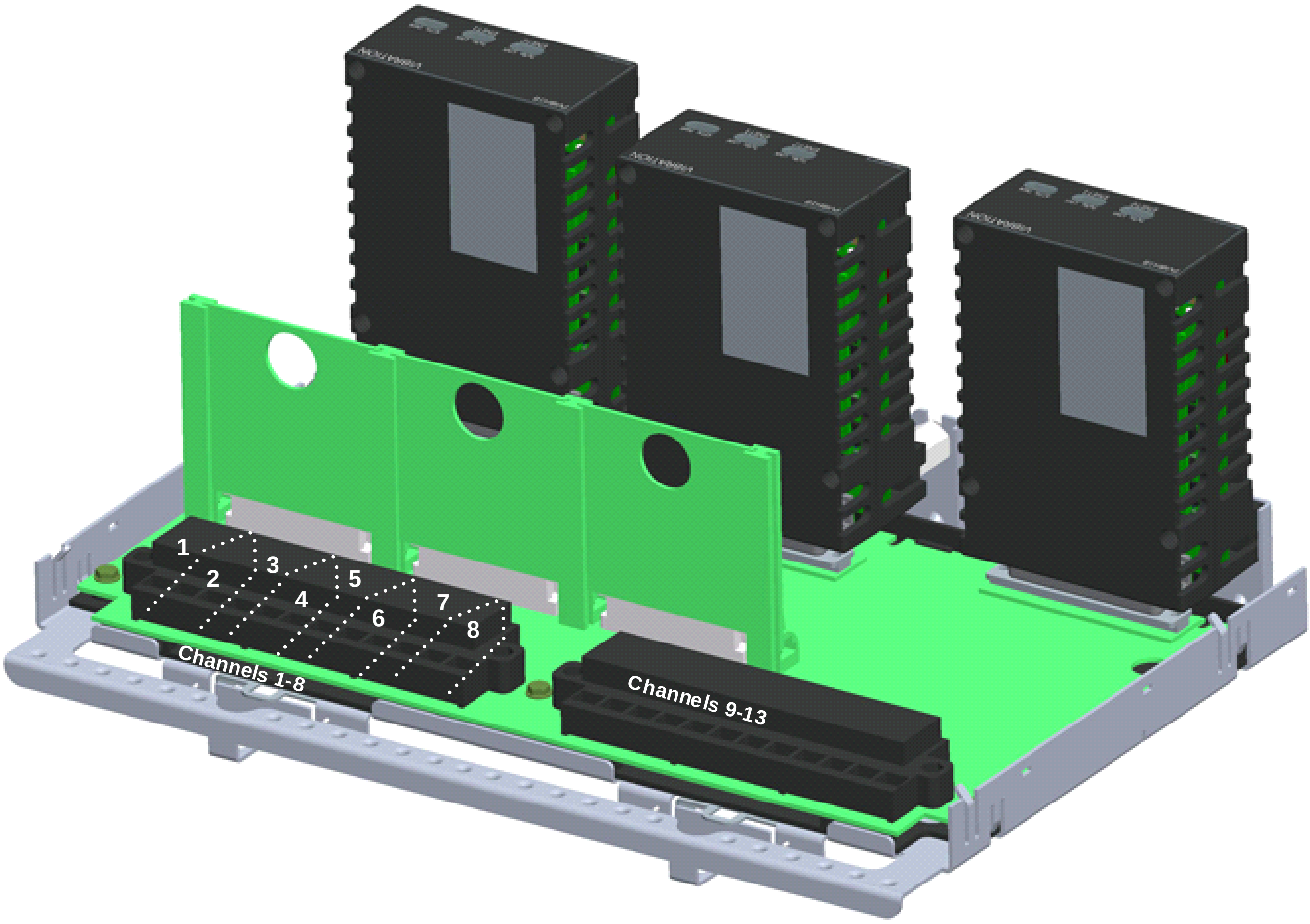
16.2 Mark VIe PVIB Vibration Monitor I/O Pack



The PVIB vibration monitoring module contains a local processor and data acquisition board, which are housed in an I/O pack. Either one or three I/O packs can be mounted on the TVBA terminal board, to provide either Simplex or TMR module redundancy. The TVBA provides two 24-point, barrier-type terminal blocks that accept two 3.0 mm2 (#12AWG) wires with 300 V insulation and spade or ring type lugs.

Captive clamps are provided for terminating bare wires. Signal flow between the terminal blocks and the I/O packs is conditioned with passive suppression circuits and electromagnetic interference protection. In addition, a pull-up bias is applied to signals for open circuit fault detection.

The PVIB can monitor 13 sensors, and has the flexibility to mix sensor types based on specific channel configuration and PVIB processor type. The I/O pack has two RJ-45 Ethernet connectors, one 3-pin power input, and a DC-37 pin connector that connects directly to the TVBA terminal board. Visual diagnostics are provided through indicator LEDs.



16.2.1 PVIB Compatibility

There are currently two versions of the I/O pack as follows:

- The PVIBH1A contains a BPPB processor board and two application boards. These internal boards have reached end of life.
- The PVIBH1B contains a BPPC processor board and a single application board. This I/O pack is supported with ControlST V06.01 or later. It provides support for Dual IONets at 10 ms frame period, an additional KeyPhasor input, and a Combustion Dynamics Monitoring (CDM) input.

PVIBH1A and PVIBH1B can be mixed on a TMR module, but cannot be configured for Enhanced signal mode unless all three packs are PVIBH1B. In this mixed TMR configuration, all three I/O packs must be upgraded to firmware version 5.01 or later. In addition, there are manual steps needed to correct some existing configuration because of the additional GAP12 capabilities that are introduced in firmware version 5.01. Refer to the section *PVIB I/O pack replacement* for detailed procedures.

Caution

An online replacement is only available for PVIB if the firmware version is 5.01 or later. It is recommended that the site perform a firmware upgrade during their next outage time frame to equip these I/O packs for any necessary online replacement should one fail.

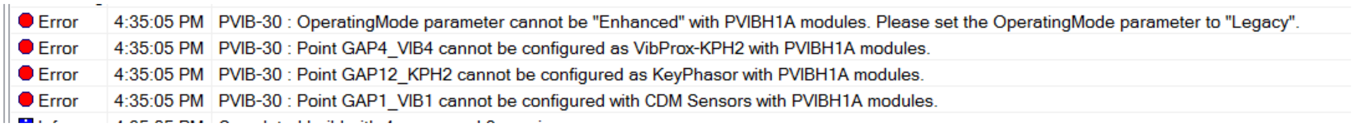
Attention

PVIBH1A can be upgraded to firmware version 5.01 or later, however, configuration in the ToolboxST application is required to manually fixed some existing GAP12 configurations. Refer to the replacement procedure for detailed instructions.

With GAP12 on PVIBH1A, Gain adjustments of 2x and 8x are not valid.

For existing PVIBH1A applications where upgrading to PVIBH1B, the user may need to use the configurable low-pass filter to roll-off response to match the H1A for peak-to-peak calculations because PVIBH1B has an increased input signal bandwidth of 4500 Hz.

From the ToolboxST application, if the user chooses to configure a PVIBH1A with any of the options that are only available with the PVIBH1B, the following build errors (example) are generated.



```
● Error   4:35:05 PM   PVIB-30 : OperatingMode parameter cannot be "Enhanced" with PVIBH1A modules. Please set the OperatingMode parameter to "Legacy".
● Error   4:35:05 PM   PVIB-30 : Point GAP4_VIB4 cannot be configured as VibProx-KPH2 with PVIBH1A modules.
● Error   4:35:05 PM   PVIB-30 : Point GAP12_KPH2 cannot be configured as KeyPhasor with PVIBH1A modules.
● Error   4:35:05 PM   PVIB-30 : Point GAP1_VIB1 cannot be configured with CDM Sensors with PVIBH1A modules.
```

The following table provides a summary of differences for the PVIBH1A and PVIBH1B I/O pack versions.

Summary of Differences in PVIB Versions

Revision	Processor ‡	Application Board(s)‡	PVIB Firmware Version	ToolboxST Version	Mark VIe Controller Firmware Version	Enhanced Signal Mode	IONets	Channels / Sensor Types
PVIBH1A	BPPB	BAFA KAPA	Any	Any	Any	No	Dual IONets only if frame rate is slower than 10 ms	13 / (H1A is different) *Supported Sensor Types*
PVIBH1B	BPPC	BBAA	≥ 5.01 bundled on ControlST V06.01 or later	≥ 4.04 is required minimum version	≥ 4.04 is required minimum version	Yes	Dual is supported even at 10 ms rate	13 / (H1B is different) *Supported Sensor Types*
‡These boards are internal to the I/O pack and are not replaceable.								

The following table displays the available sensor types per channel with respect to the two different version of PVIB.

PVIB Supported Sensor Inputs

Sensor Type	Typical Application	PVIB Channel	
		PVIBH1A	PVIBH1B
Accelerometer	Aero-derivative gas turbines	1 - 8	1 - 8
Combustion Dynamics	Heavy-duty gas turbines	N/A	1 - 8
Proximitors (Vibration)	Radial or axial measurements of turbine-driven generators, compressors, and pumps.	1 - 8	1 - 8
Velomitor*	Structural Vibration (mounted to case)	1 - 8	1 - 8
Pedestal or slot-type Keyphasor	Rotor velocity and phase measurements	13	12, 13
Seismics	Structural Vibration (mounted to case)	1 - 8	1 - 8
Proximitors (Position)	Axial measurements	1-13	1-13

The PVIB I/O pack is compatible with the Vibration Terminal Board (TVBA) with simplex or TMR module redundancy.

PVIB and TVBA Compatibility

Terminal Board	Description
TVBAH1A	Does not have buffered outputs
TVBAH2A	Provides buffered outputs and output connections
TVBAH1B	Vibration terminal board without buffered outputs; WNPS function integrated into terminal board and PVIB I/O pack S-position is lined up vertically with R and T positions.
TVBAH2B	Vibration terminal board with buffered outputs; WNPS function integrated into terminal board and PVIB I/O pack S-position is lined up vertically with R and T positions.

Note Refer to the section *TVBA Compatibility* for additional information.

16.2.2 PVIB Specifications

Item	PVIB Specification
Orderable Part Numbers	Contact your nearest GE sales or service office, or an authorized GE sales representative.
Input Signal Bandwidth	PVIBH1A: 1150 Hz PVIBH1B: 4500 Hz
Number of Channels	13 sensor inputs are supported. Refer to the table *Supported Sensor Inputs*
Buffered Outputs (only with TVBAH2A and TVBAH2B)	Amplitude accuracy is 0.1 % for signal to GE Bently Nevada 3500 system
	A -11 V dc ±5% bias is added to output when a seismic probe used.
	Sinks a minimum of 3 mA when interfacing a velomitor
Accuracy	Refer to these tables: *Accuracy Vibration Inputs*, *Accuracy Position Inputs*
Probe Power	-24 V dc from the -28 V dc bus, from the WNPS daughterboard Each probe supply is current limited with 12 mA load per transducer
Probe Signal Resolution	Minimum of 14-bit resolution for full scale ranges defined
Open Circuit Detection	Open circuit is defined as a gap voltage that is > 1.0 V for Proximity, Accelerometer, Keyphasor, and CDM BN at terminals > -1.0 V for Velomitor at terminals < -1.0 V for CDM PCB at terminals < -3.0 V for Seismic at terminals
Common Mode Voltage	Minimum of 5 V dc
CMRR at 50/60 Hz	-50 dB
Size	8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in x 1.65 in x 4.78 in)
Technology	Surface-mount
† Ambient rating for enclosure design	PVIBH1B is rated from -40 to 70°C (-40 to 158 °F) PVIBH1A is rated from -30 to 65°C (-22 to 149 °F)

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

16.2.3 PVIB Installation

➢ **To install a new PVIB module into an existing Mark VIe panel**

1. Securely mount the desired terminal board.
2. Directly plug the PVIB I/O pack(s) into the terminal board connectors (JR1 for Simplex pack, all three for TMR packs).
3. Mechanically secure the I/O packs using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right-angle force applied to the DC-37 pin connector between the I/O pack and the terminal board. The adjustment should only be required once in the service life of the product. Spacers are needed for the S-pack in a TMR set.
4. Plug in one or two Ethernet cables depending on the system configuration. The I/O pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
5. For the TVBAH#A, verify that the WNPS daughterboard(s) (one per I/O pack) are seated properly in the connector. (TVBAH#B does not have a WNPS daughterboard; the N28 function is integrated into the terminal board.)
6. Apply power to the I/O pack by plugging in the connector on the side of the I/O pack. It is not necessary to remove power from the cable before plugging it in because the I/O pack has inherent soft-start capability that controls current inrush on power application.
7. Use the ToolboxST* application to configure the I/O pack as necessary. The following table provides links to some typical configurations examples, based on application (not necessarily any site-specific configuration).

Application	Configuration Example
In Heavy Duty turbine applications, Proximitors are used to monitor the position of a rotating shaft.	*Position Application Example*
In Heavy Duty turbine applications, a Keyphasor is used to calculate the position and rotating speed of a rotating shaft.	*Keyphasor Application Example*
In Heavy Duty turbine applications, Vibration Displacement algorithms report a filtered air gap value, and peak-to-peak displacement value, and an optional vibration phasor relative to a specified Keyphasor channel.	*Vibration Displacement Application Example*
In LM turbine applications, Velocity sensors are mounted on bearing housings or machine casing to provide measurements of vibration.	*Velocity Application Example*
In Heavy Duty turbine applications, Combustion Dynamics Monitoring is used.	*CDM Application Example*

16.2.4 Operation

The following features are common to the distributed I/O modules:

- *BPPx Processor*
- *Processor LEDs*
- *Power Management*
- *ID Line*
- *I/O Module Common Diagnostic Alarms*

16.2.5 PVIB I/O Pack Replacement

➢ **To replace a PVIB I/O pack**

Caution

Follow all site safety procedures.

1. Remove the power plug located in the connector on the side of the failed I/O pack.
2. Unplug the Ethernet cable(s) from the failed I/O pack, and mark the positions of the removed cable(s).
3. Loosen the two mounting nuts on the I/O pack threaded shafts.
4. Unplug the I/O pack.
5. Plug in the replacement I/O pack. Make sure the I/O pack connector is fully seated on all sides, then properly tighten mounting nuts.
6. Plug the Ethernet and power cables back into the I/O pack.

Use the following table to determine the correct replacement procedures for the I/O pack firmware.

PVIB I/O Pack Replacement Use Cases

Module Redundancy	Failed Hardware Form	New Hardware Form
Simplex	PVIBH1A	*PVIBH1A* *PVIBH1B*
	PVIBH1B	*PVIBH1B*
TMR	PVIBH1A	*PVIBH1A* *PVIBH1B* (mixed with other PVIBH1As does not allow enhanced mode) *PVIBH1B* (all three are now H1Bs)
	PVIBH1B	*PVIBH1B*

➢ **To replace with the same PVIB firmware/configuration**

1. If the Auto-Reconfiguration feature is enabled, the Mark VIe controller detects the newly installed I/O pack running with a different configuration than what is in the ToobloxST application, and a reconfiguration file is automatically downloaded from the controller to the new I/O module.
2. If Auto-reconfiguration is not enabled, use the ToolboxST application to download the existing configuration to the new I/O pack.

➢ To upgrade only one PVIB I/O pack (H1A to H1B) in a TMR set (offline)

Attention

Enhanced features are not available on mixed H1A/H1B TMR sets.

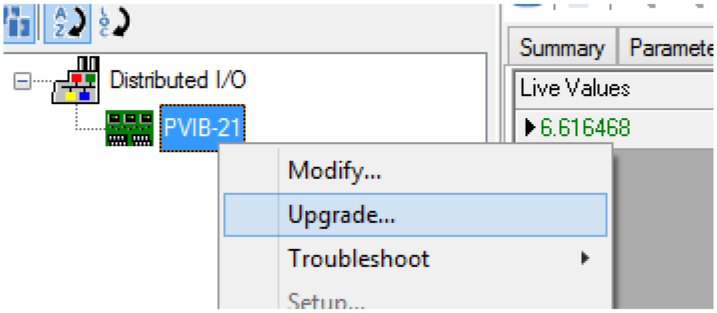
Caution

An online replacement is not available for PVIB if the firmware of the existing I/O packs is not minimum version 5.01. It is recommended that the site perform a firmware upgrade during their next outage time frame to equip their I/O packs for any necessary online replacement should a I/O pack fail. The necessary firmware is available on the ControlST 6.02 or later DVD.

1. Do not enable Enhanced mode. In addition, review the PVIB Compatibility information for other configurations that are only available when using all PVIBH1B I/O packs on the same terminal board.
2. Complete steps in the procedure *To Upgrade hardware forms in a PVIB module*.

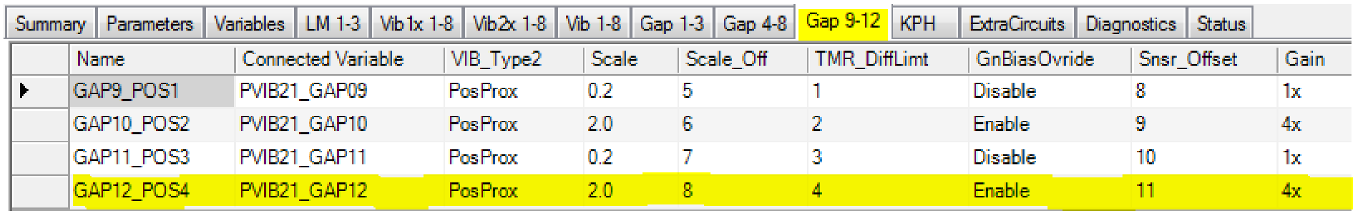
➢ To Upgrade hardware forms (from H1A to H1B) in a Simplex PVIB module or all three PVIBs in a TMR module

1. The site's ControlST software must be minimum V04.04. Verify the version and upgrade the site if needed.
2. The PVIB must have an installed firmware version of 5.01 or later on the computer that is running ToolboxST application. Verify the available version and install new software if needed. The necessary firmware is available from the ControlST 6.02 or later DVD.
3. From the ToolboxST application, run an I/O report to identify the current configuration for the PVIB module. This is important because some manual reconfiguration may be required after upgrade.
4. From the ToolboxST Component Editor, Tree View, right-click the PVIB and select **Upgrade**.



5. Click **OK** to go offline with the ToolboxST application.
6. Refer to the I/O report generated prior to Upgrade and the Gap 9–12 configuration.

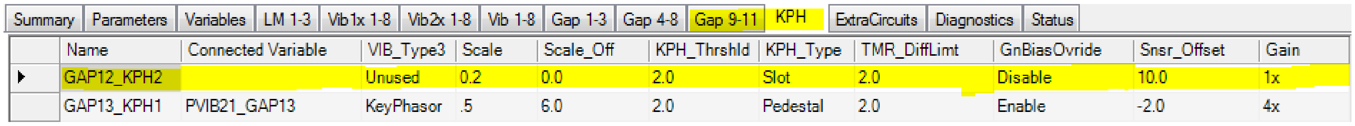
Gap 9–12 Before Upgrade (example)



Name	Connected Variable	VIB_Type2	Scale	Scale_Off	TMR_DiffLimt	GnBiasOvride	Snsr_Offset	Gain
GAP9_POS1	PVIB21_GAP09	PosProx	0.2	5	1	Disable	8	1x
GAP10_POS2	PVIB21_GAP10	PosProx	2.0	6	2	Enable	9	4x
GAP11_POS3	PVIB21_GAP11	PosProx	0.2	7	3	Disable	10	1x
GAP12_POS4	PVIB21_GAP12	PosProx	2.0	8	4	Enable	11	4x

7. GAP12_POS4 configuration is reset to defaults after the upgrade and renamed GAP12_KPH2. It will need to be manually reconfigured, and have the variable reattached after the upgrade. The variable has been moved from Gap 9-12 tab to KPH tab. Use the following screens as examples for making this correction.

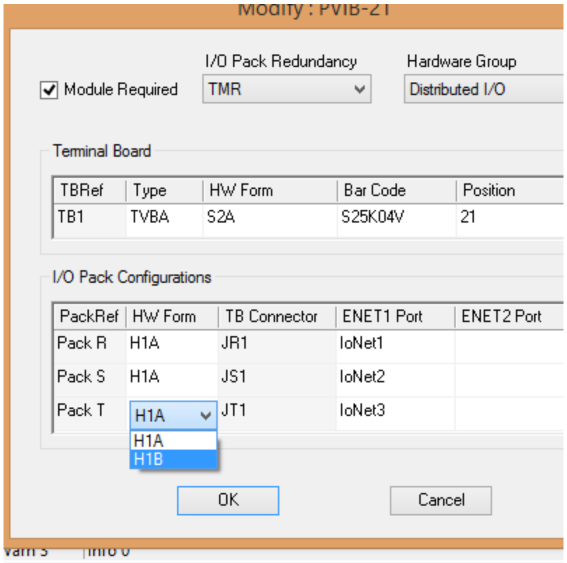
GAP12 in the KPH tab After Upgrade Before Correction (example)



Name	Connected Variable	VIB_Type3	Scale	Scale_Off	KPH_Thrshld	KPH_Type	TMR_DiffLimt	GnBiasOvride	Snsr_Offset	Gain
GAP12_KPH2		Unused	0.2	0.0	2.0	Slot	2.0	Disable	10.0	1x
GAP13_KPH1	PVIB21_GAP13	KeyPhasor	.5	6.0	2.0	Pedestal	2.0	Enable	-2.0	4x

8. If running a ToolboxST application that is a version prior to V06.01, then make the changes to the PVIB configuration as detailed in the section, *PVIB Reconfiguration After Firmware Upgrade, when using an older version of ToolboxST application*.

9. From the Component Editor, modify the hardware form of the PVIBH1B I/O pack(s).



☑ Module Required

I/O Pack Redundancy: TMR

Hardware Group: Distributed I/O

Terminal Board

TBRef	Type	HW Form	Bar Code	Position
TB1	TVBA	S2A	S25K04V	21

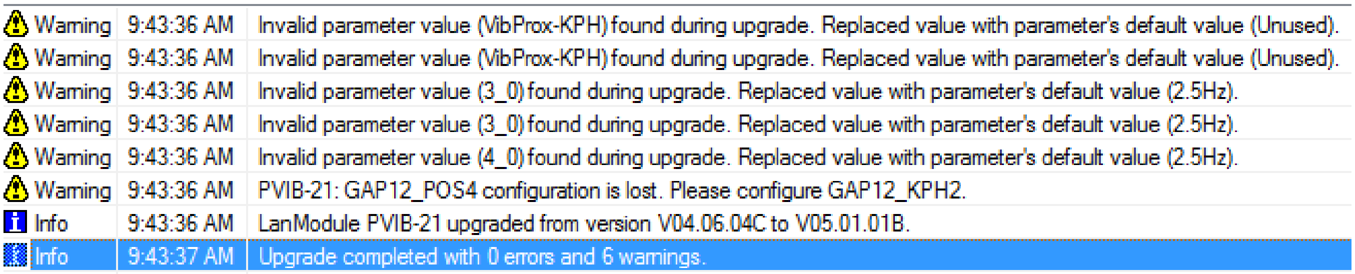
I/O Pack Configurations

PackRef	HW Form	TB Connector	ENET1 Port	ENET2 Port
Pack R	H1A	JR1	IoNet1	
Pack S	H1A	JS1	IoNet2	
Pack T	H1A	JT1	IoNet3	

10. Perform a build and download. Build errors will display if invalid configurations are chosen.

16.2.5.1 PVIB Reconfiguration After Firmware Upgrade, when using an older version of ToolboxST application

After performing an Upgrade of the PVIB firmware in the ToolboxST application, changes are displayed in the Log. If ToolboxST is earlier than 6.01 version, existing configurations for LMlpcutoff (Gap 1-3 tab), VIB_Type4 (Gap 1-3 tab), and VIB_Type (Gap 4-8 tab) are changed to default values. It is necessary for the user to take the following steps to restore these configurations.

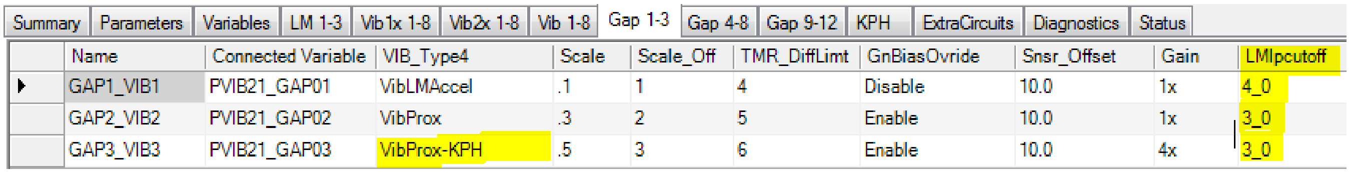


```
Warning  9:43:36 AM  Invalid parameter value (VibProx-KPH) found during upgrade. Replaced value with parameter's default value (Unused).
Warning  9:43:36 AM  Invalid parameter value (VibProx-KPH) found during upgrade. Replaced value with parameter's default value (Unused).
Warning  9:43:36 AM  Invalid parameter value (3_0) found during upgrade. Replaced value with parameter's default value (2.5Hz).
Warning  9:43:36 AM  Invalid parameter value (3_0) found during upgrade. Replaced value with parameter's default value (2.5Hz).
Warning  9:43:36 AM  Invalid parameter value (4_0) found during upgrade. Replaced value with parameter's default value (2.5Hz).
Warning  9:43:36 AM  PVIB-21: GAP12_POS4 configuration is lost. Please configure GAP12_KPH2.
Info     9:43:36 AM  LanModule PVIB-21 upgraded from version V04.06.04C to V05.01.01B.
Info     9:43:37 AM  Upgrade completed with 0 errors and 6 warnings.
```

➢ To fix the GAP 1-3 and GAP 4-8 configurations

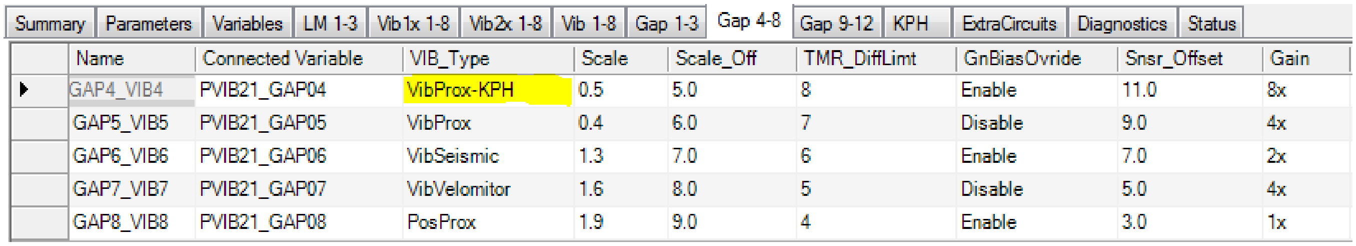
1. Refer to the I/O report (that the prior procedure asked you to generate prior to Upgrade) and the Gap 1-3 and Gap 4-8 configuration.

Gap 1-3 Before Upgrade (example)



	Name	Connected Variable	VIB_Type4	Scale	Scale_Off	TMR_DiffLimt	GnBiasOvride	Snsr_Offset	Gain	LMIpcutoff
▶	GAP1_VIB1	PVIB21_GAP01	VibLMAccel	.1	1	4	Disable	10.0	1x	4_0
	GAP2_VIB2	PVIB21_GAP02	VibProx	.3	2	5	Enable	10.0	1x	3_0
	GAP3_VIB3	PVIB21_GAP03	VibProx-KPH	.5	3	6	Enable	10.0	4x	3_0

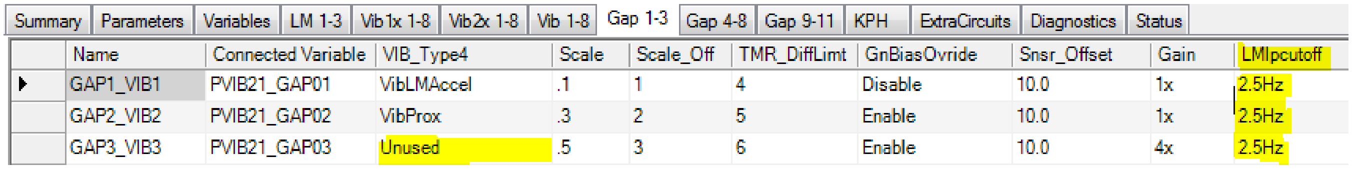
Gap 4-8 Before Upgrade (example)



	Name	Connected Variable	VIB_Type	Scale	Scale_Off	TMR_DiffLimt	GnBiasOvride	Snsr_Offset	Gain
▶	GAP4_VIB4	PVIB21_GAP04	VibProx-KPH	0.5	5.0	8	Enable	11.0	8x
	GAP5_VIB5	PVIB21_GAP05	VibProx	0.4	6.0	7	Disable	9.0	4x
	GAP6_VIB6	PVIB21_GAP06	VibSeismic	1.3	7.0	6	Enable	7.0	2x
	GAP7_VIB7	PVIB21_GAP07	VibVelomitor	1.6	8.0	5	Disable	5.0	4x
	GAP8_VIB8	PVIB21_GAP08	PosProx	1.9	9.0	4	Enable	3.0	1x

2. Navigate to the **Gap 1-3** tab and notice that items have been reset to default values.

Gap 1-3 After Upgrade

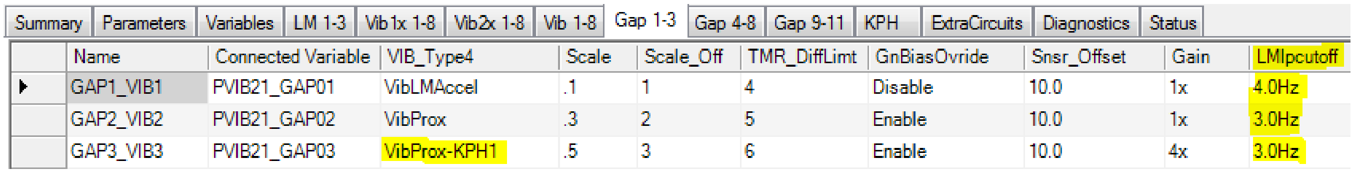


	Name	Connected Variable	VIB_Type4	Scale	Scale_Off	TMR_DiffLimt	GnBiasOvride	Snsr_Offset	Gain	LMIpcutoff
▶	GAP1_VIB1	PVIB21_GAP01	VibLMAccel	.1	1	4	Disable	10.0	1x	2.5Hz
	GAP2_VIB2	PVIB21_GAP02	VibProx	.3	2	5	Enable	10.0	1x	2.5Hz
	GAP3_VIB3	PVIB21_GAP03	Unused	.5	3	6	Enable	10.0	4x	2.5Hz

3. From the **Gap 1-3** tab, make the following corrections to reset the original values where they were replaced with default values.

• Any sensors configured for VibProx-KPH will be marked Unused after the upgrade. They will need to be set to VibProx-KPH1 manually.
• The values of LMIpcutoff for GAP1_VIB1, GAP2_VIB2, and GAP3_VIB3 will be automatically set to 2.5 Hz after the upgrade. They will need to be manually reset to their renamed original values after the upgrade (3_0 becomes 3.0Hz).

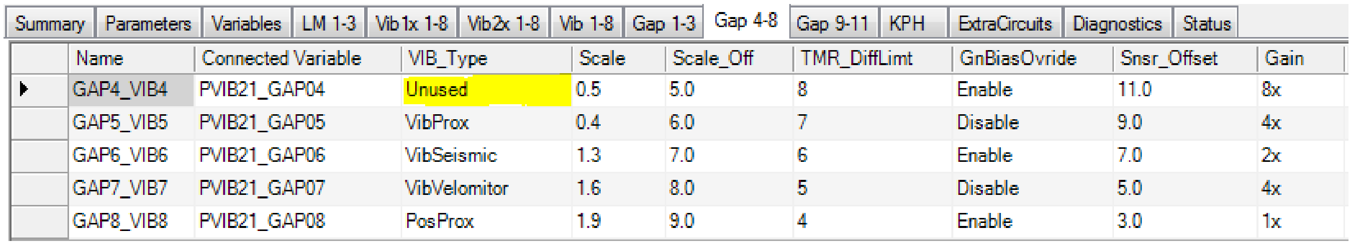
Gap 1-3 Corrected (example)



	Name	Connected Variable	VIB_Type4	Scale	Scale_Off	TMR_DiffLimt	GnBiasOvride	Snsr_Offset	Gain	LMIpcutoff
▶	GAP1_VIB1	PVIB21_GAP01	VibLMAccel	.1	1	4	Disable	10.0	1x	4.0Hz
	GAP2_VIB2	PVIB21_GAP02	VibProx	.3	2	5	Enable	10.0	1x	3.0Hz
	GAP3_VIB3	PVIB21_GAP03	VibProx-KPH1	.5	3	6	Enable	10.0	4x	3.0Hz

4. Navigate to the **GAP4_VIB4** tab and notice that the VIB_Type for **VibProx-KPH** has been set to **Unused** after the Upgrade.

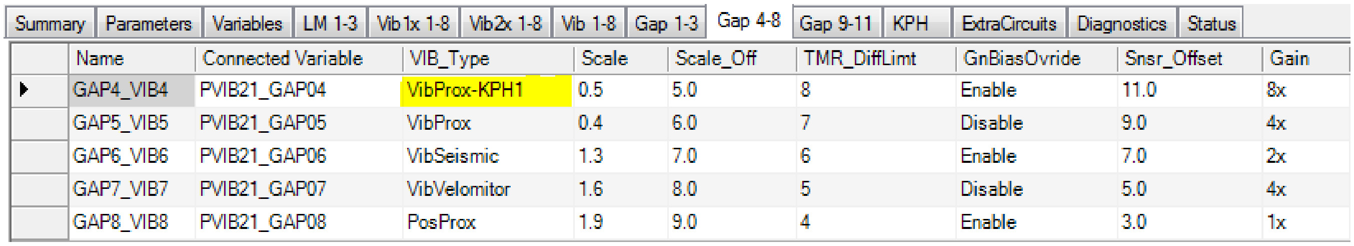
GAP 4-8 After Upgrade



	Name	Connected Variable	VIB_Type	Scale	Scale_Off	TMR_DiffLimt	GnBiasOvride	Snsr_Offset	Gain
▶	GAP4_VIB4	PVIB21_GAP04	Unused	0.5	5.0	8	Enable	11.0	8x
	GAP5_VIB5	PVIB21_GAP05	VibProx	0.4	6.0	7	Disable	9.0	4x
	GAP6_VIB6	PVIB21_GAP06	VibSeismic	1.3	7.0	6	Enable	7.0	2x
	GAP7_VIB7	PVIB21_GAP07	VibVelomitor	1.6	8.0	5	Disable	5.0	4x
	GAP8_VIB8	PVIB21_GAP08	PosProx	1.9	9.0	4	Enable	3.0	1x

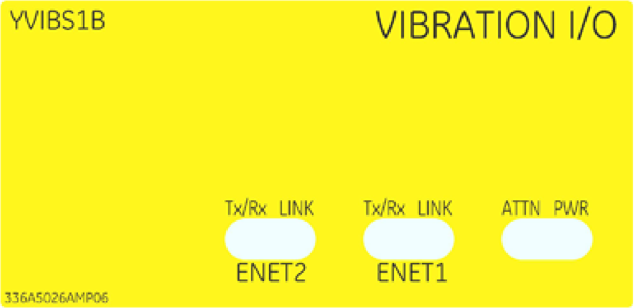
5. Set the **VIB_Type** for what was VibProx-KPH to now be **VIBProx-KPH1**.

GAP 4-8 Corrected (example)



	Name	Connected Variable	VIB_Type	Scale	Scale_Off	TMR_DiffLimt	GnBiasOvride	Snsr_Offset	Gain
▶	GAP4_VIB4	PVIB21_GAP04	VibProx-KPH1	0.5	5.0	8	Enable	11.0	8x
	GAP5_VIB5	PVIB21_GAP05	VibProx	0.4	6.0	7	Disable	9.0	4x
	GAP6_VIB6	PVIB21_GAP06	VibSeismic	1.3	7.0	6	Enable	7.0	2x
	GAP7_VIB7	PVIB21_GAP07	VibVelomitor	1.6	8.0	5	Disable	5.0	4x
	GAP8_VIB8	PVIB21_GAP08	PosProx	1.9	9.0	4	Enable	3.0	1x

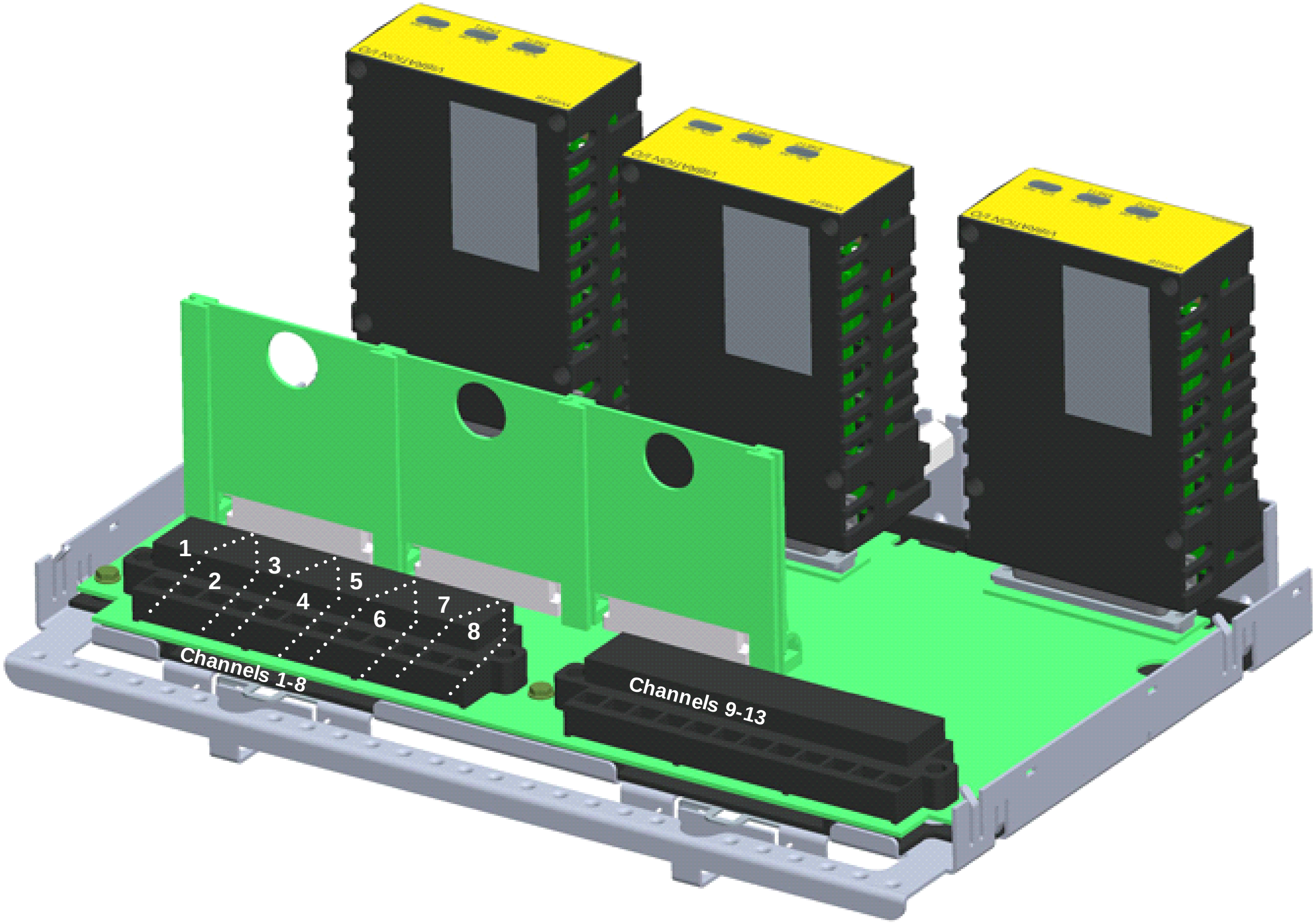
16.3 Mark VIeS YVIB Vibration Monitor I/O Pack



The YVIB vibration monitoring module contains a local processor and data acquisition board, which are housed in an I/O pack. Either one or three I/O packs can be mounted on the TVBA terminal board, to provide either Simplex or TMR module redundancy. The TVBA provides two 24-point, barrier-type terminal blocks that accept two 3.0 mm2 (#12AWG) wires with 300 V insulation and spade or ring type lugs.

Captive clamps are provided for terminating bare wires. Signal flow between the terminal blocks and the I/O packs is conditioned with passive suppression circuits and electromagnetic interference protection. In addition, a pull-up bias is applied to signals for open circuit fault detection.

The YVIB can monitor 13 sensors, and has the flexibility to mix sensor types based on specific channel configuration and YVIB processor type. The I/O pack has two RJ-45 Ethernet connectors, one 3-pin power input, and a DC-37 pin connector that connects directly to the TVBA terminal board. Visual diagnostics are provided through indicator LEDs.



16.3.1 YVIB Compatibility

The YVIB I/O pack contains an internal processor board. The following table lists the available versions of the YVIB.

YVIB Version Compatibility

I/O Pack	Processor Board	Compatible (Supported) Firmware	ControlST Software Suite Versions
YVIBS1A	BPPB	V04.06	Supported in V04.06 and all later versions
YVIBS1B	BPPC	V05.01 and later	Supported in V06.02 and later versions

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Attention

YVIBS1A and YVIBS1B cannot be mixed on a TMR module.

Attention

If upgrading to YVIBS1B with an existing YVIBS1A configuration, use the ToolboxST application to correct the GAP12 configuration. Refer to the replacement procedure *To replace a YVIB I/O pack* in the section *YVIB I/O Pack Replacement*.

After upgrading existing YVIBS1A applications to YVIBS1B, the user may need to use the configurable low-pass filter to roll-off responses to match existing peak-to-peak calculations. This is because the YVIBS1B has an increased input signal bandwidth of 4500 Hz.

The YVIB I/O pack is compatible with the Vibration (TVBA) terminal board.

YVIB Terminal Board Compatibility

Terminal Board	Description	I/O Pack Redundancy		
		Simplex	Dual	TMR
TVBAS1A	Does not have buffered outputs. IEC 61805 certified with YVIB.	Yes	No	Yes
TVBAS2A	Provides buffered outputs and output connections. IEC 61805 certified with YVIB.	Yes	No	Yes
TVBAS2B	Safety vibration terminal board with buffered outputs; N28 function integrated into terminal board and YVIB S-position is lined up vertically with R and T positions.	Yes	No	Yes

Note Refer to the section *TVBA Compatibility* for additional information.

I/O pack redundancy refers to the number of I/O packs used in a signal path, as follows:

- Simplex uses one I/O pack.
- TMR uses three I/O packs.

The following table provides a summary of differences between the YVIBS1A and YVIBS1B.

Summary of YVIB Version Differences

I/O Pack	Processor Board†	Application Board(s)†	Enhanced Signal Mode‡	Channels	Sensor Types
YVIBS1A	BPPB	BAFA KAPA	No	13	Refer to the table *YVIB Supported Sensor Inputs*
YVIBS1B	BPPC	BBAA	Yes	13	Refer to the table *YVIB Supported Sensor Inputs*
† These boards are internal to the I/O pack and are not replaceable. ‡ YVIBS1B supports an additional KeyPhasor* input, a CDM input, and other enhanced processing capabilities.					

The following table displays the available sensor types per channel for YVIBS1A and YVIBS1B.

YVIB Supported Sensor Inputs

Sensor Type	Typical Application	YVIB Channel	
		YVIBS1A	YVIBS1B
Accelerometer	Aero-derivative gas turbines	1 - 8	1 - 8
Dynamic pressure probe	Land-Marine (LM) and Heavy-duty gas turbines (HDGT)	N/A	1 - 8
Proximitors* (Vibration)	Radial or axial measurements of turbine-driven generators, compressors, and pumps.	1 - 8	1 - 8
Velomitor*	Structural Vibration (mounted to case)	1 - 8	1 - 8
Pedestal or slot-type Keyphasor	Rotor velocity and phase measurements	13	12, 13
Seismics	Structural Vibration (mounted to case)	1 - 8	1 - 8
Proximitors (Position)	Axial measurements	1-13	1-13

16.3.2 YVIB Specifications

Item	YVIB Specification
Orderable Part Numbers	Contact your nearest GE sales or service office, or an authorized GE sales representative.
Number of Channels	13 sensor inputs are supported. Refer to the table *YVIB Supported Sensor Inputs*
Buffered Outputs (only with TVBAS2A and TVBAS2B)	Amplitude accuracy is 0.1 % for signal to Bently Nevada* 3500 system
	A -11 V dc ±5% bias is added to output when a seismic probe used
	Sinks a minimum of 3 mA when interfacing a velomitor
Accuracy	Refer to these tables: *Accuracy Vibration Inputs*, *Accuracy Position Inputs*
Functional Safety ***Refer to the Mark VIeS Safety Control Functional Safety Instruction Guide (GEH-6723) for safety instructions.***	YVIBS1A: Vibration functions are low and high demand SIL 2 capable when deployed with HFT=1. (1oo2 and 2oo3 architectures). YVIBS1B: Vibration functions shall be low and high demand SIL 3 capable when deployed with HFT=1. (1oo2 and 2oo3 architectures).
Probe Power	-24 V dc from the -28 V dc bus, from the WNPS daughterboard Each probe supply is current limited with 12 mA load per transducer
Probe Signal Resolution	Minimum of 14-bit resolution for full scale ranges defined
Open Circuit Detection	Open circuit is defined as a gap voltage that is > 1.0 V for Proximity, Accelerometer, Keyphasor, and CDM BN at terminals > -1.0 V for Velomitor at terminals < -1.0 V for CDM PCB at terminals < -3.0 V for Seismic at terminals
Common Mode Voltage	Minimum of 5 V dc
CMRR at 50/60 Hz	-50 dB
Size	8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in x 1.65 in x 4.78 in)
Technology	Surface-mount
† Ambient rating for enclosure design	YVIBS1A and YVIBS1B are rated from -30 to 65°C (-22 to 149 °F)

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

16.3.3 YVIB Installation

➢ **To install a new YVIB module into an existing Mark VIeS panel**

1. Securely mount the desired terminal board.
2. Directly plug the YVIB I/O pack into the terminal board connectors.
3. Mechanically secure the I/O packs using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right-angle force applied to the DC-37 pin connector between the I/O pack and the terminal board. The adjustment should only be required once in the service life of the product.

Note The I/O pack mounts directly to a TVBA terminal board. This TMR-capable terminal board has three DC-37 pin connectors and can also be used in simplex mode if only one YVIB is installed to JR1.

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4. Plug in one or two Ethernet cables depending on the system configuration. The I/O pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
5. For the TVBAS#A, verify that the WNPS daughterboard(s) (one per I/O pack) are seated properly in the connector. (TVBAS2B does not have a WNPS daughterboard; the N28 function is integrated into the terminal board.)
6. Apply power to the I/O pack by plugging in the connector on the side of the I/O pack. It is not necessary to remove power from the cable before plugging it in because the I/O pack has inherent soft-start capability that controls current inrush on power application.
7. Use the ToolboxST* application to configure the I/O pack. The following table provides links to some typical configurations examples based on application (not necessarily any site-specific configuration).

Application	Configuration Example
In Heavy Duty turbine applications, Proximitors are used to monitor the position of a rotating shaft.	*Position Application Example*
In Heavy Duty turbine applications, a Keyphasor is used to calculate the position and rotating speed of a rotating shaft.	*Keyphasor Application Example*
In Heavy Duty turbine applications, Vibration Displacement algorithms report a filtered air gap value, and peak-to-peak displacement value, and an optional vibration phasor relative to a specified Keyphasor channel.	*Vibration Displacement Application Example*
In LM turbine applications, Velocity sensors are mounted on bearing housings or machine casing to provide measurements of vibration.	*Velocity Application Example*
In Heavy Duty turbine applications, Combustion Dynamics Monitoring is used.	*CDM Application Example*

16.3.4 Operation

The following features are common to the distributed I/O modules:

- *BPPx Processor*
- *Processor LEDs*
- *Power Management*
- *ID Line*
- *I/O Module Common Diagnostic Alarms*

16.3.5 YVIB I/O Pack Replacement

➢ **To replace a YVIB I/O pack**

1. Follow all site safety procedures.
2. Remove the power plug located in the connector on the side of the failed I/O pack.
3. Unplug the Ethernet cable(s) from the failed I/O pack, and mark the positions of the removed cable(s).
4. Loosen the two mounting nuts on the I/O pack threaded shafts.
5. Unplug the I/O pack.
6. Plug in the replacement I/O pack. Make sure the I/O pack connector is fully seated on all sides, then properly tighten mounting nuts.
7. Plug the Ethernet and power cables back into the I/O pack.

Use the following table to determine the correct replacement procedures for the I/O pack firmware.

YVIB I/O Pack Replacement Use Cases

Module Redundancy	Failed Hardware Form	New Hardware Form
Simplex	YVIBS1A	YVIBS1A YVIBS1B
	YVIBS1B	YVIBS1B
TMR	YVIBS1A	YVIBS1A YVIBS1B (all three must be replaced with S1Bs)
	YVIBS1B	YVIBS1B

➢ **To replace a YVIB I/O pack with the same firmware/configuration:** use the ToolboxST application to download the existing configuration to the new I/O pack.

Attention

Do NOT upgrade the firmware of any YVIBS1A to a version beyond V04.06.03C. Making this mistake is extremely difficult to reverse, and would be best if the site then upgrades to YVIBS1B.

➢ To upgrade YVIB hardware forms (S1A to S1B)

Attention

Redundant Safety I/O packs mounted on the same terminal board must all be of the same hardware form, and running the same firmware version.

Do NOT attempt this replacement unless having enough I/O packs with the newer hardware form available, including spares.

It is also recommended to backup the ToolboxST .tcw file prior to upgrading the system.

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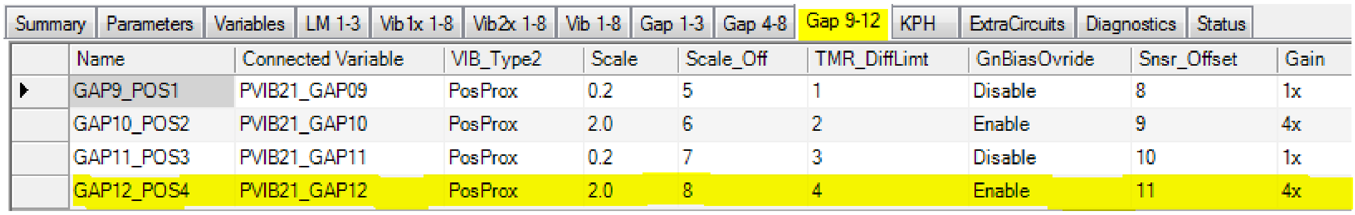
1. The site's ControlST software must be minimum V06.01. Verify the version and upgrade the system if needed.
2. Install the YVIBH1B I/O pack firmware from the ControlST V06.02 or later DVD.
3. Run an I/O report to capture the current configuration of the YVIB I/O module.
4. From the Component Editor, modify the hardware form of the YVIB I/O pack.
5. From the ToolboxST Component Editor, perform a YVIB firmware Upgrade.
6. From the Component Editor, make the changes to the YVIB configuration.
7. Refer to the I/O report generated prior to Upgrade and the Gap 9–12 configuration.

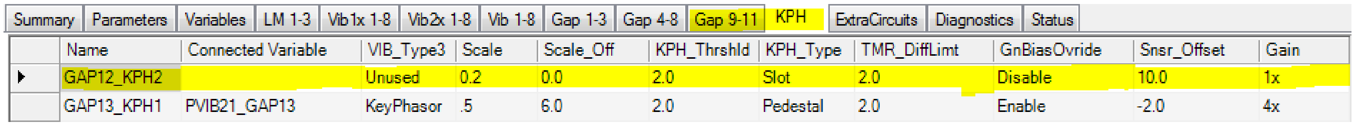
Gap 9–12 Before Upgrade (example)



	Name	Connected Variable	VIB_Type2	Scale	Scale_Off	TMR_DiffLimt	GnBiasOvride	Snsr_Offset	Gain
▶	GAP9_POS1	PVIB21_GAP09	PosProx	0.2	5	1	Disable	8	1x
	GAP10_POS2	PVIB21_GAP10	PosProx	2.0	6	2	Enable	9	4x
	GAP11_POS3	PVIB21_GAP11	PosProx	0.2	7	3	Disable	10	1x
	GAP12_POS4	PVIB21_GAP12	PosProx	2.0	8	4	Enable	11	4x

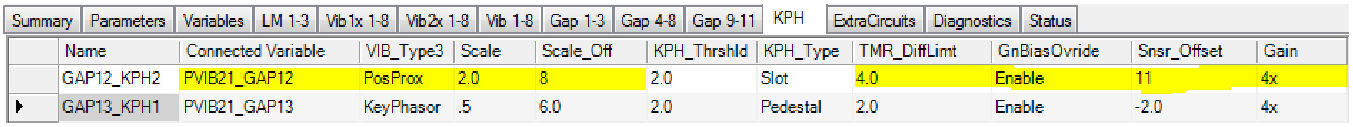
8. GAP12_POS4 configuration is reset to defaults after the upgrade and renamed GAP12_KPH2. It will need to be manually reconfigured, and have the variable reattached after the upgrade. The variable has been moved from Gap 9-12 tab to KPH tab. Use the following screens as examples for making this correction.

Gap 9–11 and KPH tabs After Upgrade Before Correction (example)



	Name	Connected Variable	VIB_Type3	Scale	Scale_Off	KPH_Thrshld	KPH_Type	TMR_DiffLimt	GnBiasOvride	Snsr_Offset	Gain
▶	GAP12_KPH2		Unused	0.2	0.0	2.0	Slot	2.0	Disable	10.0	1x
	GAP13_KPH1	PVIB21_GAP13	KeyPhasor	.5	6.0	2.0	Pedestal	2.0	Enable	-2.0	4x

KPH tab After Upgrade After Correction (example)



	Name	Connected Variable	VIB_Type3	Scale	Scale_Off	KPH_Thrshld	KPH_Type	TMR_DiffLimt	GnBiasOvride	Snsr_Offset	Gain
	GAP12_KPH2	PVIB21_GAP12	PosProx	2.0	8	2.0	Slot	4.0	Enable	11	4x
▶	GAP13_KPH1	PVIB21_GAP13	KeyPhasor	.5	6.0	2.0	Pedestal	2.0	Enable	-2.0	4x

9. Perform and build and download from the ToolboxST Component Editor. Build errors will display if invalid configurations are chosen.

16.4 PVIB or YVIB Functions

16.4.1 Vibration Monitoring Hardware

Internal to the PVIB or YVIB I/O pack is application-specific hardware that provides signal conditioning to center and amplify signals for improved analog-to-digital resolution. Each of the 13 differential amplifier inputs has a digital analog converter (DAC) bias adjustment to null the dc content of the signal to better center the signal for the analog-to-digital (A/D) input range. The DAC bias command is stored in the microprocessor to be used in the gap calculation for the Proximitor sensors.

Each input channel has a configurable gain that allows the vibration signal to be amplified. Refer to the *configuration* section for a detailed listing of available gains based on channel number and I/O pack board revision (H1B supports an additional Keyphasor on channel 12). Analog processing provides A/D conversion, digital-to-analog (D/A) conversion, and the digital pre-processing of sensor inputs. Sensor inputs are digitally filtered, and then the sampled signals and the filtering information is passed on to PVIB microprocessor memory. Channels 1 through 8 and 13 (and 12 if H1B) use a multi-pole anti-aliasing filter with a band-pass frequency range of 7 kHz.

There is a tracking filter that is used to determine the vibration content of a turbine caused by a given rotation speed. This same internal application hardware also runs the high-frequency section of the tracking filter and the 1x and 2x functions. The 1x vibration is the peak-to-peak magnitude of the radial movement in sync with the turbine shaft speed. The 1x calculation also provides the phase relationship of the vibration phasor relative to the Keyphasor. The 2x calculation provides the radial vibration component that is at twice the speed of the shaft.

The internal hardware of the PVIBH1A or YVIBS1A is different than PVIBH1B or YVIBS1B. The H1B or SIB provides an additional Keyphasor input (channel 12) and support for Combustion Dynamic Monitoring (CDM) sensors, as well as the ability to run in an Enhanced mode that offers additional input resolution and other features.

16.4.1.1 Accuracy of Vibration Inputs

Accuracy of Vibration Inputs for PVIBH1A and YVIBS1A

Vibration Inputs	Measurement	Range		Frequency	Accuracy
		V dc + V ac	V ac portion		
Proximity	Displacement	+1 to -20 V peak	0 to 4.5 V pp	10 to 200 Hz	±0.030 V pp† (1% at 3 V pp†)
				200 to 700 Hz	±0.150 V pp† (5% at 3 V pp†)
Seismic	Velocity	+1 to -1 V peak	0 to 1.00 V peak	10 to 200 Hz	Max [2% reading, ±.008 V peak]
				200 to 700 Hz	Max [5% reading, ±.008 V peak]
Velomitor	Velocity	-8.75 to 15.625 V peak	0 to 3.625 V peak	10 to 200 Hz	Max [2% reading, ±.008 V peak]
				200 to 700 Hz	Max [5% reading, ±.008 V peak]
Accelerometer	Velocity (tracking filter)	-8.75 to -11.5 V peak	0 to 1.5 V peak	10 to 350 Hz	±0.015 V peak
† V pp - V peak-peak					

Accuracy of Vibration Inputs for PVIBH1B and YVIBS1B

Vibration Inputs	Measurement	Range		Default Hardware Gain	Default Hardware Offset	Accuracy @ min & max frequency range
		(V dc + V ac)	(V ac portion)			
Eddy-Current or Proximity (channels 1 - 8)	Displacement	-20.0 to 0.0 V peak	0 to 3.0 V pp	1x	10	+/-0.020 Vpp @ 10 Hz +/-0.023 Vpp @ 200 Hz
						+/-0.023 Vpp @ 200 Hz +/-0.056 Vpp @ 700 Hz
Seismic (channels 1 - 8)	Velocity	-2.5 to +2.5 V peak	0 to 1.0 V peak	4x	0	+/-0.010 Vp @ 10 Hz +/-0.012 Vp @ 200 Hz
						+/-0.012 Vp @ 200 Hz +/-0.034 Vp @ 700 Hz
Velomitor (channels 1 - 8)	Velocity	-17.0 to -7.0 V peak	0 to 5 V peak	2x	12	+/-0.010 Vp @ 10 Hz +/-0.020 Vp @ 200 Hz
						+/-0.020 Vp @ 200 Hz +/-0.130 Vp @ 700 Hz
Accelerometer (channels 1 - 3)	Velocity	-12.5 to -7.5 V peak	0 to 2.5 V peak	4x	10	+/-0.010 Vp @ 10 Hz +/-0.025 Vp @ 350 Hz
Bently Nevada CDM	Dynamic Pressure	-15.0 to -5.0 V peak	-5.0 to 5.0 V peak	2x	10	+/-0.010 Vp @ 10 Hz +/-0.132 Vp @ 1000 Hz
PCB CDM	Dynamic Pressure	5.0 to 15.0 V peak	-5.0 to 5.0 V peak	2x	-10	+/-0.010 Vp @ 10 Hz +/-0.132 Vp @ 1000 Hz
The accuracies specified are worst case numbers, and assume the Vibration module sample frequency is in sync with the input waveform frequency, preventing the A/D sample point from moving along the waveform and reading the actual peak value. The worst case accuracy is based on missing the maximum peak V ac measurement per the table by half the sample period relative to the input fundamental frequency.						

16.4.1.2 Accuracy of Position Inputs

Accuracy of Position Inputs for PVIBH1A and YVIBS1A

Position Inputs	**Measurement**	**Range**	**Frequency**	**Accuracy**
Position	Displacement (Gap)	-0.5 to -20 V dc	N/A	±0.2 V dc (1% of full scale)
Keyphasor	Displacement (Gap)	-0.5 to -20 V dc	N/A	±0.2 V dc (1% of full scale)
	Speed	N/A	2 to 20,000 rpm	±0.1 % of full scale speed
	Phase ***Phase is only calculated when RPM is greater than approximately 250 RPM.***	N/A	Up to 333 Hz	±1 degree for 1x **
			333 to 667	±2 degrees for 2x
** 1x vibration component with respect to key slot				

Accuracy of Position Inputs for PVIBH1B and YVIBS1B

Position Inputs	**Measurement**	**Range**	**Frequency**	**Accuracy**
Position	Displacement (Gap)	-0.5 to -20 V dc	N/A	+/-0.020 Vpp @ 10 Hz
Keyphasor	Displacement (Gap)	-0.5 to -20 V dc	N/A	+/-0.020 Vpp @ 10 Hz
	Speed	N/A	2 to 20,000 RPM	+/-0.1% of full scale speed
	Phase ***Phase is only calculated when RPM is greater than approximately 250 RPM.***	N/A	Up to 333 Hz	+/-0.5 degree
			333 to 667 Hz	+/-1 degree
** 1x vibration component with respect to key slot				

16.4.1.3 Tracking Filters

The following table defines differences in the tracking filters with versions of the I/O pack.

Item	PVIBH1A / YVIBS1A	PVIBH1B / YVIBS1B
Center frequency	Prior to ControlST V06.01: The center frequency was 50% larger than configuration setting. With ControlST V06.01 or later: The H1A or SIA functions the same as H1B or S1B	-3dB bandwidth correctly matches configuration settings to meet application requirements.
Filter roll off	Prior to ControlST V06.01: Window attenuation limited to -30 dB / octave With ControlST V06.01 or later: The H1A or SIA functions the same as H1B or S1B	Window attenuation increased to -36 dB / octave to meet application requirements.
1X / 2X channels	Use channel 13 only for phase reference	Can base phase measurements off of channel 12 or 13.

16.4.1.4 Wideband Filters & Velocity Conditioning

The following table defines differences in the Wideband Filters & Velocity Conditioning with versions of the I/O pack.

Item	PVIBH1A / YVIBS1A	PVIBH1B / YVIBS1B
Supported Sensors	Velomitors and Seismics only	Velomitors, Seismics & LM Accelerometers with integrated outputs
Maximum octave attenuation	-48 dB for all filter configurations	-60 dB for all filter configurations
Output of wideband filter	Can only be mapped to Peak-to-peak algorithm.	Can either be assigned to an RMS calculation or Peak-to-peak algorithm, using *VIB_CalcSel*
Notes	Peak-to-peak algorithm uses a scan period based on the GAP13_KPH1 key-phasor speed. If there is no key-phasor input, 160 ms scan period is the default.	Peak-to-peak algorithm and RMS calculation use a Scan time of data. Update rate is equal Frame Rate. ISO for Vibration calls for RMS calculations

16.4.1.5 CDM Sensors

PVIBH1B and YVIBS1B add support for CDM sensors (not available with H1A and S1A). From the **Parameters** tab, CDM_scan_period is a selectable scan period for CDM sensor inputs.

Item	PVIBH1A / YVIBS1A	PVIBH1B / YVIBS1B
Supported sensors	None because CDM is not supported by PVIBH1A / YVIBS1A	Inputs 1-8 support the following: Bently Nevada CDM Sensor (CDM_BN_ChgAmp) PCB CDM Sensor (CDM_PCB_ChgAmp)
Maximum octave attenuation	N/A	-60 dB for all filter configurations
Output of wideband filter	N/A	Can either be assigned to an RMS calculation or Peak-to-peak algorithm, using VIB_CalcSel
Scan period selection	N/A	Peak-to-peak or RMS scan period configured by the CDM_Scan_ Period parameter.
LM 1x tracking filter support	N/A	Peak-to-peak output supported for up to 3 frequency selections (Inputs 1-3 only)

16.4.2 Vibration Monitoring Firmware

The following subsections provide details for common firmware features using in vibration monitoring applications. For application-specific firmware use cases and procedures, refer to the section, *Vibration Monitoring Application Examples*.

16.4.2.1 Signal Space Inputs for Sensor Types, with Firmware Version 5.01 or Later

Note n = input number

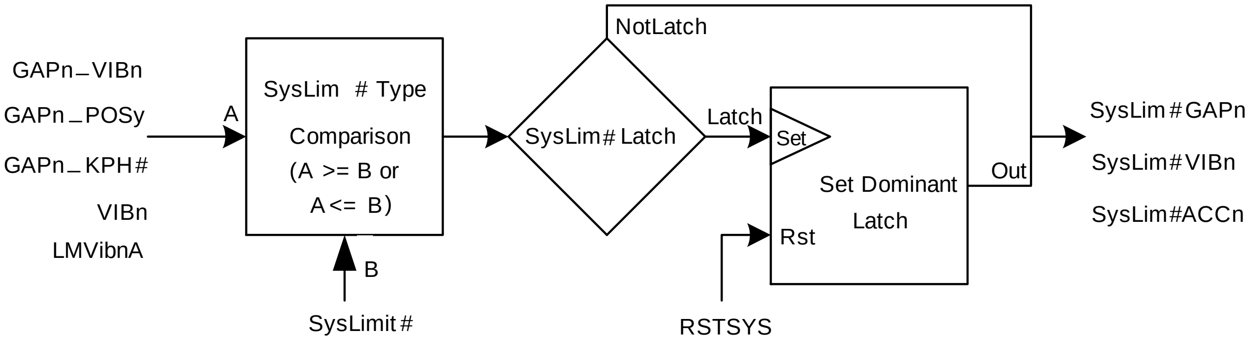
Sensor Type	GAPn_VIBn	GAPn_POSy (y = 1-3)	GAP12_KPH2 GAP13_KPH1	VIBn	VIB_1Xn Vib1xPHn VIB_2Xn Vib2xPHn	LMVibnA LMVibnB LMVibnC
PosProx	Inputs 1-8	Inputs 9-11	Inputs 12-13			
VibProx	Inputs 1-8			Inputs 1-8		
VibProx-KPHx	Inputs 1-8			Inputs 1-8	Inputs 1-8	
VibLMAccel	Inputs 1-8			Inputs 1-8		Inputs 1-3
VibSeismic	Inputs 1-8			Inputs 1-8		Unused (H1A)
						Inputs 1-3 (H1B)
VibVelomitor	Inputs 1-8			Inputs 1-8		Unused (H1A)
						Inputs 1-3 (H1B)
CDM_BN_ChgAmp (H1B Only)	Unused (H1A)			Unused (H1A)		Unused (H1A)
	Inputs 1-8 (H1B)			Inputs 1-8 (H1B)		Inputs 1-3 (H1B)
CDM_PCB_ChgAmp (H1B Only)	Unused (H1A)			Unused (H1A)		Unused (H1A)
	Inputs 1-8 (H1B)			Inputs 1-8 (H1B)		Inputs 1-3 (H1B)
KeyPhasor			Inputs 13 (H1A)			
			Inputs 12-13 (H1B)			

16.4.2.2 System Limits

GAP, VIB, and LM 1x Tracking Filters each support System Limits for configurable limit checking. This function returns a Boolean value indicating whether the limit has been exceeded, with optional latching behavior. This function is intended to simplify application logic by moving common functionality into the PVIB/YVIB configuration.

All system limits are implemented the same way, regardless of which input we are describing. System limits checks are executed at Frame Rate, on the value in signal space after it has been converted to the correct units. Based on the configuration, the system limits check will behave as greater than set point (>=) or less than set point (<=), and the result can be latching or non-latching. System Limit latches are SET dominant, so the results of the checks will be TRUE as long as the signal exceeds the set point.

Note Latching system limits are reset using the RSTSYS pin on the SYS_OUTPUTS block.



System Limits Implementation

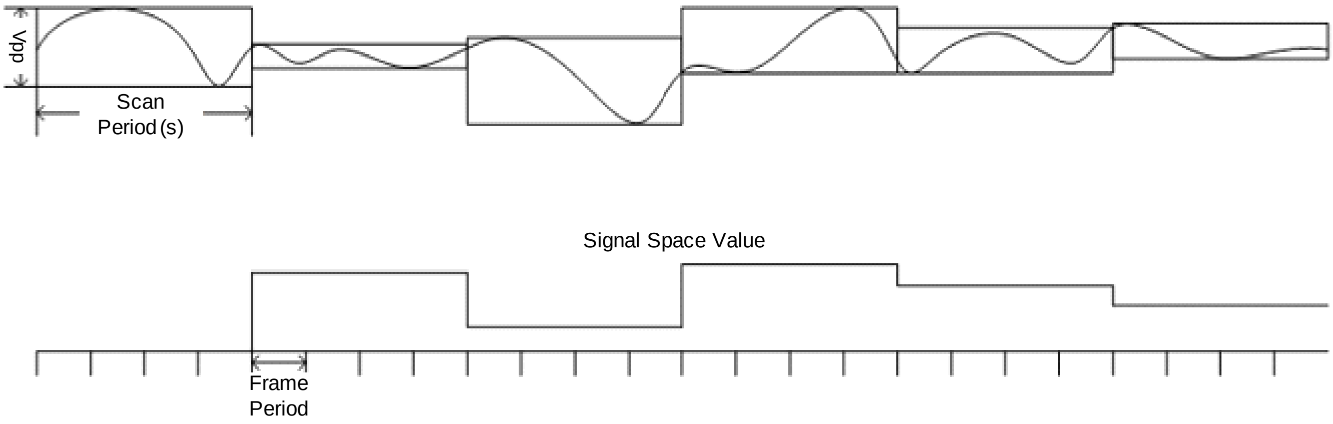
From the ToolboxST application, Component Editor, I/O pack, **Parameters** tab, there is a global System Limit disable parameter, **SystemLimits**. When this parameter is set to *Disable*, all system limits in the PVIB/YVIB are set to False, and a diagnostic alarm is generated.

Configuration of System Limits

Item	Description	Choices
SysLimit#	Set point for the System Limit check. Value is expressed in EU for that point.	Textfield
SysLim#Enabl	Enable or Disable this specific System Limit check. Value is an enumerated type.	Enable or Disable
SysLim#Latch	Configure whether system limits should latch TRUE. Value is an enumerated type.	Latch or NotLatch
SysLim#Type	Configure whether system limits checks are greater than set point or less than set point. Value is an enumerated type.	<= or >=

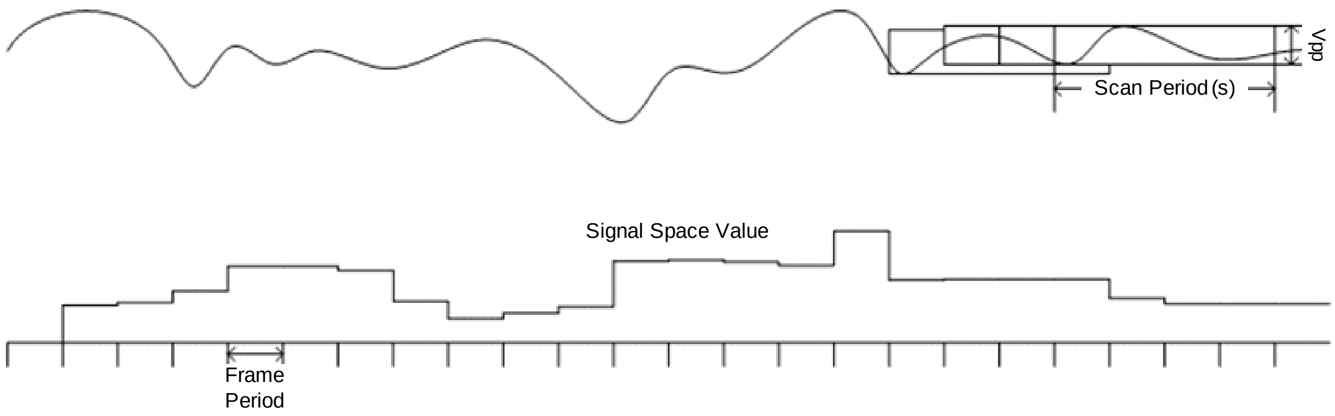
16.4.2.3 Legacy Peak-Peak Algorithm

The default vibration algorithm, which is the only vibration algorithm implemented by the PVIBH1A/YVIBS1A, is a windowed peak detection function. A window size (scan period) is determined by the current rotor speed on GAP13_KPH1. If there is no keyphasor input, 160 ms scan period is the default. As new input data is processed, it fills the window in. When the window is full, we calculate the peak-peak measurement, scale it, and send it to signal space. The window is then emptied and needs to be completely filled again before a new peak-peak value is computed. For this reason, the effective update rate is the scan period, not frame rate.



16.4.2.4 Enhanced Peak-Peak Algorithm

The enhanced peak-peak algorithm (only available with PVIBH1B or YVIBH1B) performs the same operation as the legacy peak-peak algorithm, but it executes using a sliding window, rather than a fixed window. New input data displaces old data in the windowed peak detection function. Window size (scan period) is determined by rotor speed on GAP13_KPH1. If there is no key-phasor #1 input, 160 ms scan period is the default. CDM sensors always use CDM_Scan_Period as defined in the configuration. As new data is processed, data older than the window size is displaced. At frame rate, the data within the window is used to calculate the peak-peak measurement value, which is scaled and sent to signal space. Since the window is continuously updated, the effective update rate is frame rate.



Enhanced Peak-Peak Algorithm

16.4.2.5 Enhanced RMS Algorithm

The Enhanced RMS algorithm (PVIBH1B and YVIBH1B only) uses the same sliding scan window logic as the Enhanced Peak-Peak algorithm. Data is passed through a 1-pole high-pass filter with a cutoff frequency of 0.1Hz. This removes sensor biasing voltage from the RMS value. The RMS calculation is performed on the windowed data. Window size (scan period) is determined by rotor speed on GAP13_KPH1. CDM sensors always use CDM_Scan_Period as defined in the configuration. As new data is processed, data older than the window size is displaced. At frame rate, the data within the window is used to calculate an RMS value, which is scaled and sent to signal space. Since the window is continuously updated, the effective update rate is frame rate.

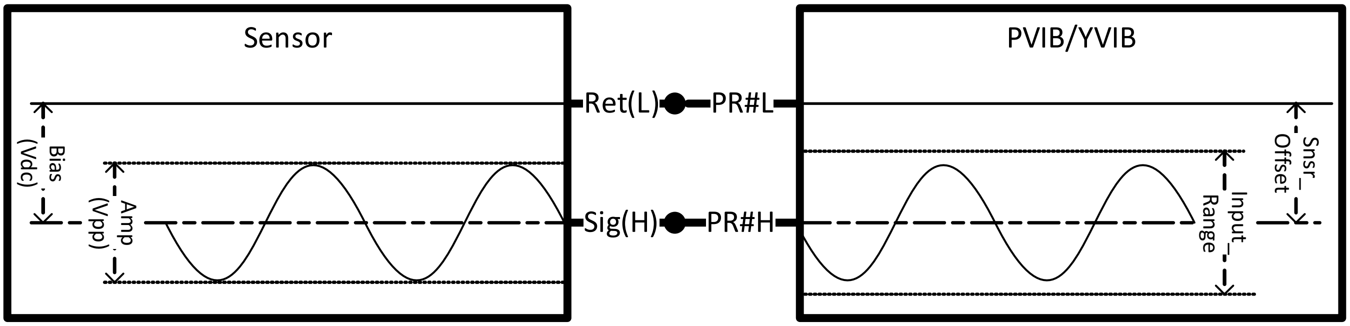
16.4.2.6 Default Sensor Gain and Bias

Each sensor has a default Gain and DC Sensor bias which is based on firmware requirements. These values are chosen based on sensor data sheets and traditional field usage.

Sensor Type	**Default Gain**	**Default Snsr_Offset**	**Vin$_{Min}$ (Volts)**	**Vin$_{Max}$ (Volts)**
PosProx	1x	9	-19	1
VibLMAccel	2x	10	-15	-5
VibProx	1x	9	-19	1
VibProx_KPH1	1x	9	-19	1
VibProx_KPH2	1x	9	-19	1
VibSeismic	4x	0	-2.5	2.5
VibVelomitor	2x	12	-17	-7
Keyphasor	1x	9	-19	1
CDM_BN_Chg_Amp	2x	10	-15	-5
CDM_PCB_Chg_Amp	2x	-12	7	17
GnBiasOvride = TRUE	G	S	((-10V/G) - S)	((10V/G) - S)

16.4.2.7 Sensor Gain and Bias Override

Depending on the specific application of a sensor, a different gain or DC bias may be needed. The PVIB/YVIB provides a configurable override for the default values for Gain and Sensor Bias through the **GnBiasOvride** parameter. Setting GnBiasOvride = Enable will replace the default Gain and Sensor Offset with the configured Gain and Snsr_Offset parameters.



Use of Gain and Snsr_Offset in PVIB/YVIB

The sensor inputs relate to the PVIB/YVIB Snsr_Offset and Input_Range values. Input_Range is a value determined by Gain through the following formula:

$$Input\_Range = \frac{20V_{pp}}{Gain}$$

Input_Range is centered on -Snsr_Offset, which allows us to define the valid input voltage range with the following formulas:

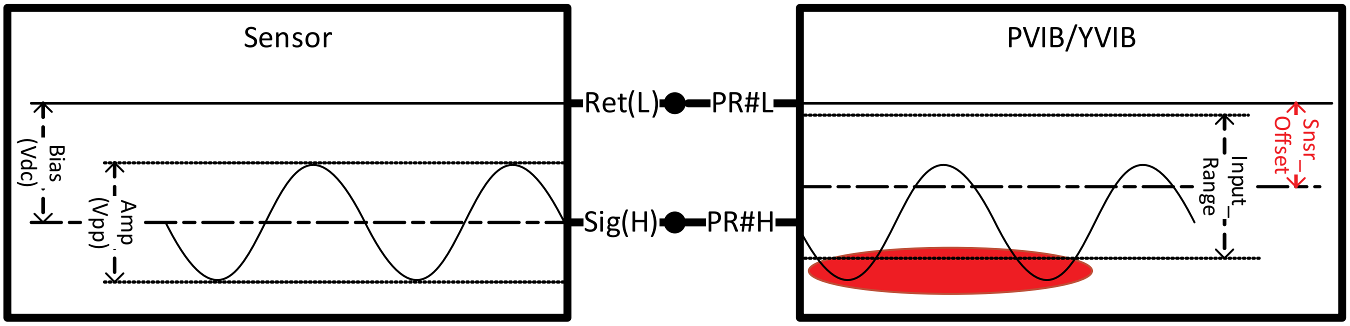
Maximum Input Voltage Definition

$$Vin_{Max} = \frac{10V}{Gain} - Snsr\_Offset$$

Minimum Input Voltage Definition

$$Vin_{Min} = \frac{-10V}{Gain} - Snsr\_Offset$$

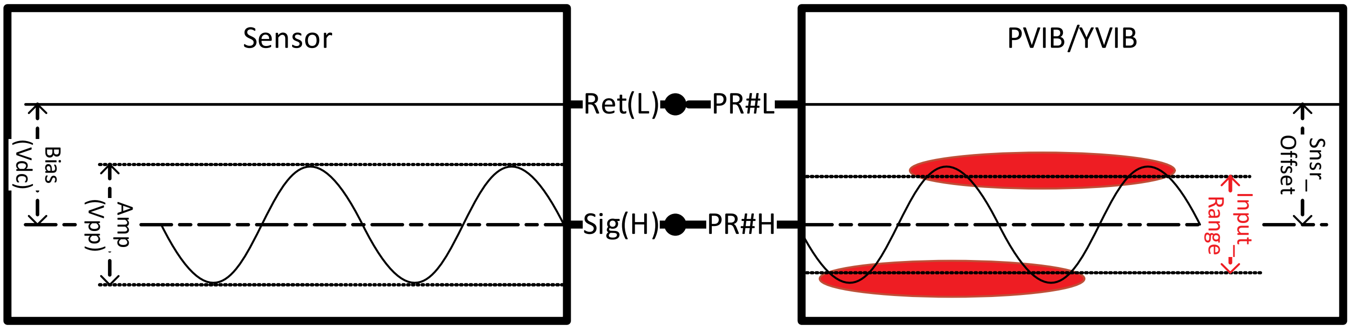
It is critical that the values of **Gain** and **Snsr_Offset** are chosen correctly to avoid saturating the A/D Converter on that input channel, which results in clipping the signal. Consider the following case, where Input Range is correctly determined, but **Snsr_Offset** is too low.



Input Clipping due to Snsr_Offset

The bottom of the Input waveform exceeds the VinMin value for this configuration. This will result in this signal being clipped off, since the A/D Converter will saturate and return only VinMin. Second, VinMax greatly exceeds the high peak of this input signal. This won’t result in an error, but it indicates that the measurement window isn’t well adapted to this input. Increasing **Snsr_Offset** will reposition the measurement window, bringing VinMax closer to the input high peak, as well as lowering VinMin below the input low peak.

Consider this case, where the selected **Gain** is too high.



Input clipping due to Gain

The **Snsr_Offset** is selected appropriately, but the Input_Range is too narrow. As a result, input signal amplitude exceeds Input_Range and we will read clipped values at both the high and low end. Verifying that Input_Range exceeds the sensor input AC amplitude is the most important factor in determining **Gain**.

In order to use the **GnBiasOvride** correctly, select a **Gain** such that Input_Range exceeds the AC amplitude of the input signal (Equation 1), and then select a **Snsr_Offset** to ensure that the measurement window defined by VinMax and VinMin contains the sensor input completely (*Max.* and *Min.* Voltage Definitions).

16.4.2.8 PVIB and YVIB Firmware Changes

The following is a list of changes made to the PVIBH1A and PVIBH1B, and YVIBS1B (not S1A) with firmware V05.01 and later.

- VibProx-KPH is renamed to VibProx-KPH1, to reflect that it uses KPH1 as source for 1x/2x tracking filters.
- LM Accelerometers are supported for Inputs 4-8, without computation of LM Tracking Filters.
- LM Tracking Filter refactored as -36 dB/oct Butterworth Filters.
- LM 1x Tracking Filters are recomputed as 6-pole filters with the correct cutoff points.
- ToolboxST Component Editor, Tab ‘Gap 9-12’ is renamed ‘Gap 9-11’ to reflect GAP12_POS4 becoming a possible Keyphasor input.
- New Parameters added to configure CDM Sensors.
- N28 Low power now affects Velomitor and CDM Bently Nevada Charge Amp health.
- Sensor out of range and Open circuit conditions hold input health low for 3 seconds after recovery.
- Default Sensor Gains and Offsets are changed, as an example: Prox biasing is -9 V dc by default, not -10 V dc. This is because the default bias value of 9 has been optimized for signal input range of +1 to -19 volts instead of optimizing for the actual BN sensor 50 ml setting.
- New Build Validation rules added to PVIB to ensure valid mixed TMR module operation with PVIBH1A and H1B packs.
- YVIB does not support mixed TMR module operation with YVIBS1A and S1Bs

16.4.2.9 PVIBH1B and YVIBS1B Firmware Enhancements

The following is a list of functional improvements made to the newer versions of PVIB and YVIB.

- LM Tracking Filters are computed for Velomitor, Seismic, and CDM sensors for Inputs 1-3 in the H1B and SIB only.
- Wideband Filters support 10-Pole Filters in the H1B and SIB only.
- Input passband increased from 1150 Hz to 4500 Hz with H1B and S1B only.

16.4.3 Vibration Monitoring Application Examples

The PVIB and YVIB modules support a variety of sensor types and applications. Refer to the tables *Supported Sensor Inputs* and *Signal Space Inputs for Sensor Types* for the relevant I/O pack for valid sensor inputs and modes.

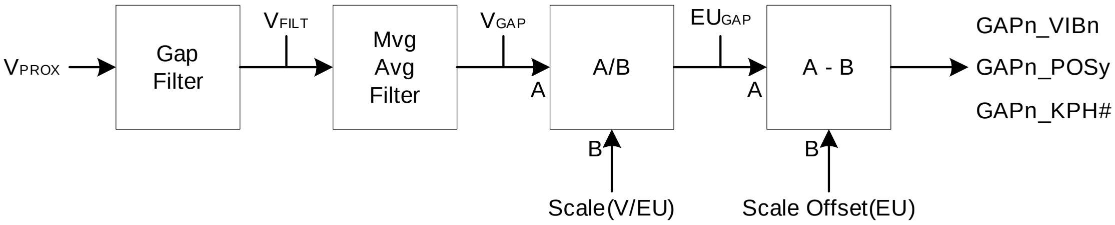
16.4.3.1 Position

Inputs 1-13 support Proximitor sensors to collect air gap value. In Heavy Duty turbine applications, Proximitors are used to monitor the position of a rotating shaft. Position algorithms report a filtered air gap value.

Input Processing

The signal space values GAPn_VIBn, GAPn_POSy, GAPn_KPH# are the filtered engineering units (EU) values.

Gap values are filtered through a 2-pole, low-pass filter with a fixed cutoff frequency of 8 Hz. The output of the gap filter is passed through a rolling average filter prior to scaling. Gap Values are converted from Volts to EU. For Position applications, Gap values have a Scale Offset parameter **Scale_Off** applied after scaling.



In this application example, SysLim1GAPn, SysLim2GAPn provide System Limit status for GAPn_VIBn value as True/False.

Position Configuration

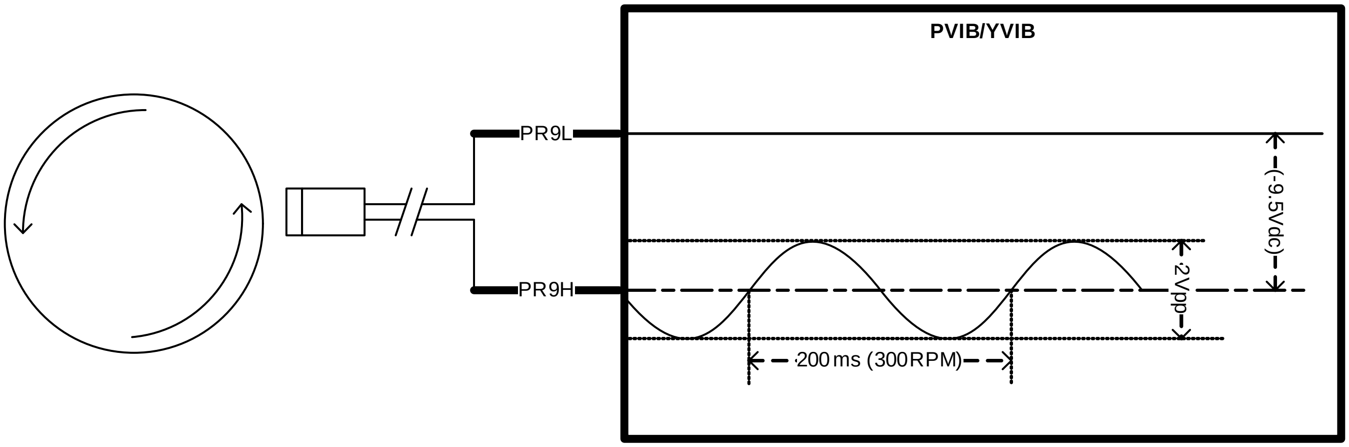
GAPn_VIBn, GAPn_POSy, GAPn_KPH#:
VibType - PosProx is used for Position applications.
Scale – Conversion from Volts to engineering units (EU). Typically, units are Volts/mils.

Scale_Off is a scale offset parameter used to remove the nominal Gap value from the measured Gap value. Units are engineering units (EU).

TMR_DiffLimt is a TMR voter disagreement detection diagnostic alarm threshold for GAPn_VIBn, GAPn_POSy, or GAPn_KPH# value. The keyphasor value is expressed as absolute difference in EU. Refer to the *Keyphasor* section for an explanation of how this value is calculated.

GnBiasOvride, Gain, Snsr_Offset – See *Gain/Bias Override*
SysLimit#, SysLim#Enabl, SysLim#Latch, SysLim#Type – See *System Limits feature*

Position Application Example



Proximitor voltage inputs to a PVIB/YVIB application are measured at the terminal board screws. Assume this sensor is connected to Channel 9 as a PosProx input.

Example Proximitor Specifications

Scale Factor	200mV/mil
Nominal Gap Setting	50 mils

Channel 9 is configured for the following behaviors:

- Return GAP9_POS1 as mils.
- Remove the nominal Gap value from GAP9_POS1.
- Set SysLim1GAP9 to LATCH True if GAP9_POS1 ≥ 5 mils.
- Set SysLim2GAP9 to LATCH True if GAP9_POS1 ≤ -5 mils.

➢ To configure GAP9_POS1

1. From the ToolboxST Component Editor, navigate to the **Gap 9-11** tab.
2. Select GAP9_POS1, and click the *Show Advanced Parameters* icon.

Note the Advanced Parameters are used if setting up system limits.

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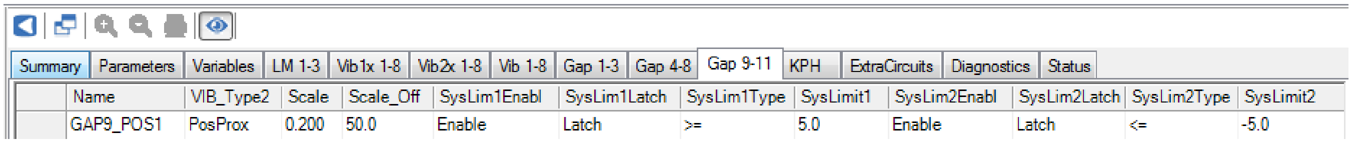
3. Configure it to match the following example.



Name	VIB_Type2	Scale	Scale_Off	SysLim1Enabl	SysLim1Latch	SysLim1Type	SysLimit1	SysLim2Enabl	SysLim2Latch	SysLim2Type	SysLimit2
GAP9_POS1	PosProx	0.200	50.0	Enable	Latch	>=	5.0	Enable	Latch	<=	-5.0

If the PVIB firmware is receiving valid sensor data, then this is expected:

- Gap values are passed through a 2-pole, low-pass filter with a cutoff frequency of 8 Hz. This will not affect either the 5Hz, 2Vpp vibration or the DC component of 9.5Vdc. The DC portion of the wave will be converted to 47.5 mils, and the AC portion of the wave will be converted to ±5.0 mils. We will remove 50.0 mils from the scaled wave, so the GAP9_POS1 value will be -2.5 ± 5.0 mils.
- SysLim1GAP9 is false and SysLim2GAP9 is true. Since SysLim2GAP9 is latching, it will remain true until the GAP9_POS1 signal is ≥ -5.0 and system limits are commanded to reset.

16.4.3.2 Keyphasor

Inputs 12-13 support Keyphasor sensors to collect air gap value and shaft rotation speed. In Heavy Duty turbine applications, a Keyphasor is used to calculate the position and rotating speed of a rotating shaft. Keyphasor algorithms report a conditioned air gap value and shaft rotation speed.

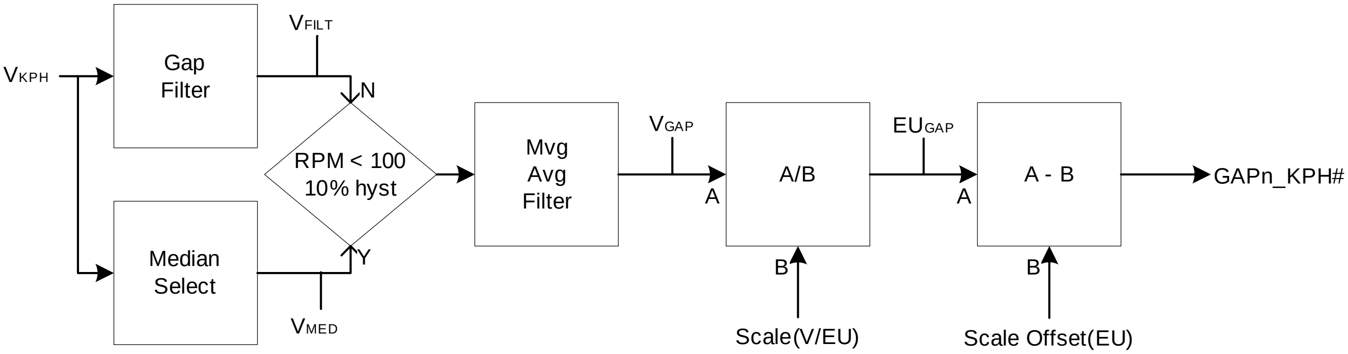
Attention

PVIBH1A only supports 1 Keyphasor on Input 13. PVIBH1B/YVIBS1B support 2 Keyphasors on Inputs 12 and 13.

Keyphasor Input Processing

GAPn_KPH# – The conditioned Position or Gap value in engineering units (EU).

Gap values are filtered through a 2-pole, low-pass filter with a fixed cutoff frequency of 8 Hz. At low speeds (100 RPM with 10% hysteresis), the Gap values bypass the filter, instead using a median selection. This allows for visual inspection of the Gap signal to show the Keyphasor edge more clearly at low speeds, removing the time delay and distortion associated with the filter. The output of the gap filter is passed through a rolling average filter prior to scaling. Gap Values are converted from Volts to EU.



GAPn_KPH# Signal Path (Keyphasor)

Scale_Off is the Scale Offset parameter used to remove the nominal Gap value from the measured Gap value. Units are engineering units (EU).

SysLim1GAPn, SysLim2GAPn – System Limit status for GAPn_KPH# value as True/False.
RPM_KPH# - The calculated shaft rotation speed in RPM.

Shaft rotation speed is calculated by detecting the time between Keyphasor transitions. Since there is only a single transition per shaft rotation, shaft rotation speed is computed once per rotation, however this requires two rotations of data for the computation. This value requires at least two full rotations before it can be computed.

At rotating speeds above 1000 RPM, RPM_KPH# is computed as the average of the speed over 4 rotations. This impacts the rate at which the RPM_KPH# signal will respond to changes in speed.

Note Only RPM_KPH1 is used by the Wideband Vibration to perform Scan Filtering.

Keyphasor Configuration

GAPn_KPH#:

VibType - KeyPhasor is used for Keyphasor applications.
Scale – Conversion from Volts to engineering units (EU). Typically, units are Volts/mils.

Scale_Off – Scale Offset to remove from measured Gap value. Units are engineering units (EU).

KPH_Thrshld – Keyphasor detection threshold for GAPn_KPH#. Value is expressed as absolute difference in Volts.

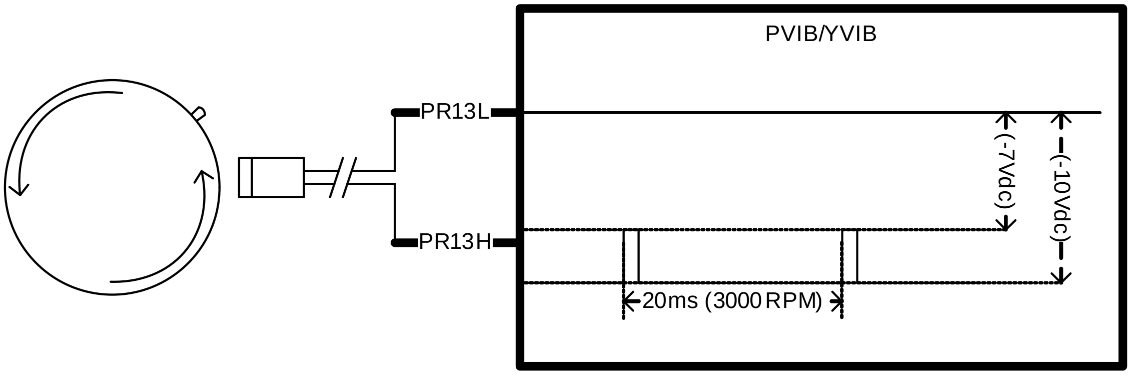
KPH_Type – Keyphasor type selection. Values are Slot, indicating the shaft has a slot or trough, or Pedestal, indicating the shaft has a key above the shaft surface. Slot detection looks for a sharply increasing distance for the key. Pedestal looks for a sharply decreasing distance for the key.

TMR_DiffLimt – TMR Voter Disagreement Detection Diagnostic alarm threshold for GAPn_KPH# value. Value is expressed as absolute difference in EU.

GnBiasOvride, Gain, Snsr_Offset – see *Gain/Bias Override*

SysLimit#, SysLim#Enabl, SysLim#Latch, SysLim#Type – See *System Limits feature*

Keyphasor Application Example



Keyphasor Sensor Monitoring Pedestal key

Keyphasor voltage inputs to a PVIB/YVIB application are measured at the terminal board screws. Assume this sensor is connected to Channel 13 as a KeyPhasor input. The shaft has a pedestal type key with a height of 15 mils above the shaft surface, so we will detect a lower air gap when the key passes by the sensor.

Example Keyphasor Specifications

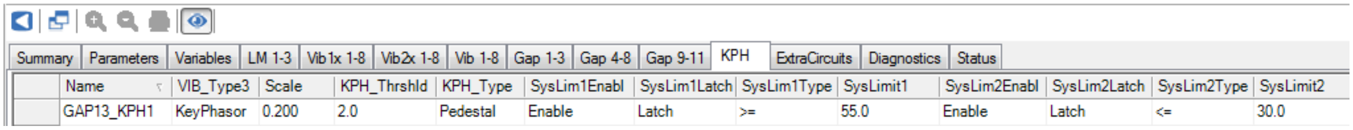
Scale Factor	200mV/mil
Nominal Gap Setting	50 mils

We will configure Channel 13 for the following behaviors:

- Return GAP13_KPH1 as mils.
- Configure the sensor as a Pedestal type Keyphasor with a threshold of 10 mils.
- Set SysLim1GAP13 to LATCH True if GAP13_KPH1 ≥ 55 mils.
- Set SysLim2GAP13 to LATCH True if GAP13_KPH1 ≤ 30 mils.

➢ To configure GAP13_KPH1

1. From the ToolboxST Component Editor, navigate to the **KPH** tab.
2. Select GAP13_KPH1, and click the *Show Advanced Parameters* icon.
3. Configure it to match the following example.



Name	VIB_Type3	Scale	KPH_Thrshld	KPH_Type	SysLim1Enabl	SysLim1Latch	SysLim1Type	SysLimit1	SysLim2Enabl	SysLim2Latch	SysLim2Type	SysLimit2
GAP13_KPH1	KeyPhasor	0.200	2.0	Pedestal	Enable	Latch	>=	55.0	Enable	Latch	<=	30.0

If the PVIB firmware is receiving the data after this configuration, we would expect:

• Gap values are passed through a 2-pole, low-pass filter with a cutoff frequency of 8 Hz, since RPM is well above the 100RPM cutoff for median values. This will cut away nearly all of the Pedestal effect on Gap value, though the average Gap value will tend to be slightly lower than the shaft Gap. The normal DC level will be converted to 50.0mils, so the GAP13_ KPH1 value will be slightly less than 50.0 mils.
• At low speeds, the Gap filter is bypassed and we can see the transition when the Pedestal clearly by monitoring the value of GAP13_KPH1. For this reason, it is important to take operating speed into account when using GAP13_KPH1 values.
• SysLim1GAP13 and SysLim2GAP13 are false, since (30.0 ≤ 50.0) and (50.0 ≤ 55.0). At low speeds, the Pedestal transitions will be much closer to the SysLim2GAP13 setpoint. For this reason, it is important to consider the operating speed when using System Limits on the Keyphasor channel. The Key will only be filtered out of the GAP13_KPH1 value when we approach running speed.
• RPM_KPH1 value is 3000 RPM. This value will be refreshed with the latest RPM measurement once every rotation, which is every 20 ms for this example.

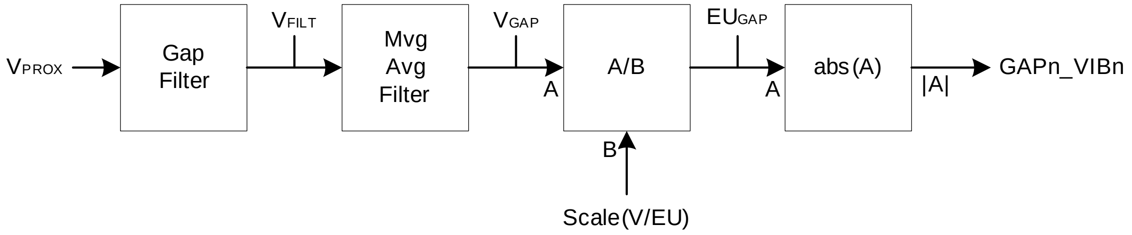
16.4.3.3 Vibration Displacement

Inputs 1-8 support Proximitor sensors to collect air gap, wideband vibration, and 1x/2x vibration vectors relative to a specified Keyphasor channel. In Heavy Duty turbine applications, Proximitors are used to monitor the position of a rotating shaft. Vibration Displacement algorithms report a filtered air gap value, and peak-to-peak displacement value, and an optional vibration phasor relative to a specified Keyphasor channel.

Vibration Displacement Input Processing

GAPn_VIBn – The filtered Position or Gap value in engineering units (EU).

Gap values are filtered through a 2-pole, low-pass filter with a fixed cutoff frequency of 8 Hz. The output of the gap filter is passed through a rolling average filter prior to scaling. Gap Values are converted from Volts to EU. For Vibration Displacement applications, Gap values are magnitude quantities, so they are always positive.



VIBn – Wideband Vibration Displacement (Peak-Peak) in engineering units (EU).

Wideband vibration information is passed through a variable scan period peak detection function. The length of the peak detection is determined by the Keyphasor 1 detected speed in RPM.

Wideband Vibration Scan Period

Shaft speed (RPM)	Scan period (ms)
0 – 60	160
60-480	2000
480-2250	250
>2250	160

Attention

Peak Detection function always uses KPH1 RPM, even when the sensor is configured to use KPH2 for 1x/2x Vibration Phasor calculations.

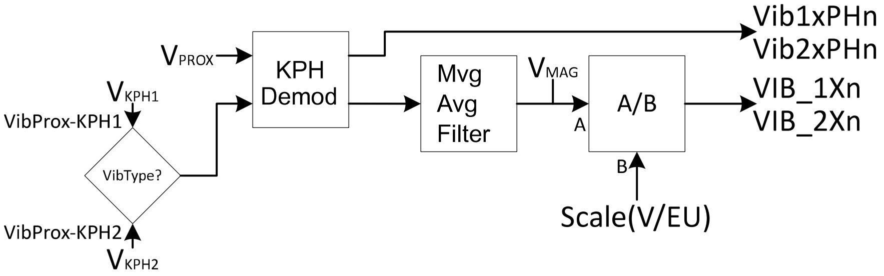
The output of the peak detection function (VPK-PK) is passed through an adjustable 1-pole, low-pass filter prior to scaling. VPK-PK is converted from Volts to EU. For PVIBH1B systems, a lower latency peak detection function can be enabled by changing the OperatingMode parameter to Enhanced. This function will update every frame, instead of every scan period. See Enhanced Vibration Algorithms for additional information.

Note Sensors monitoring position of rotating elements typically measure Peak-to-Peak. RMS calculations can be used instead if needed.

VIB_1Xn, VIB_2Xn – Vibration Phasor Magnitude (Peak-Peak) for 1st/2nd harmonic of Keyphasor frequency in engineering units (EU).

Vib1xPHn, Vib2xPHn – Phase Angle between Keyphasor and VIB_1Xn/VIB_2Xn vibration phasor in degrees.

1x/2x Vibration Phasor function measures the peak-to-peak displacement component at both the Keyphasor frequency (VIB_1Xn) and twice the frequency (VIB_2Xn). The VIB_Type selection determines which Keyphasor is used as the source for this function. Selecting VibProx will disable this function, selecting VibProx-KPH1 will enable the 1x/2x Tracking Filter operation relative to KPH1 (Channel 13), and selecting VibProx-KPH2 will enable the 1x/2x Tracking Filter relative to KPH2 (Channel 12)



SysLim1GAPn, SysLim2GAPn – System Limit status for GAPn_VIBn value as True/False.
SysLim1VIBn, SysLim2VIBn – System Limit status for VIBn value as True/False. See *System Limits feature* for more information.

Vibration Displacement Configuration

GAPn_VIBn:

VibType - VibProx, VibProx-KPH1, and VibProx-KPH2 are used for Vibration Displacement.

Note VibProx-KPH1 enables the 1x/2x Tracking Filter operation relative to KPH1 (Channel 13) and VibProx-KPH2 enables the 1x/2x Tracking Filter relative to KPH2 (Channel 12)

Attention

VibProx-KPH2 is not supported by the PVIBH1A / YVIBS1A.

Scale – Conversion from Volts to engineering units (EU). Typically, units are Volts/mils.

TMR_DiffLimt – TMR Voter Disagreement Detection Diagnostic alarm threshold for GAPn_VIBn value. Value is expressed as absolute difference in EU.
GnBiasOvride, Gain, Snsr_Offset – See Gain/Bias Override
SysLimit#, SysLim#Enabl, SysLim#Latch, SysLim#Type – See *System Limits feature*

Note Scale_Off, LMlpcutoff – Unused for this sensor type.

VIBn:

VIB_CalcSel – Select calculation method for VIBn value between Peak Displacement and RMS Displacement.

Note Sensors monitoring position of rotating elements typically measure Peak-to-Peak.

Attention

VIB_RMS is not supported by the PVIBH1A / YVIBS1A.

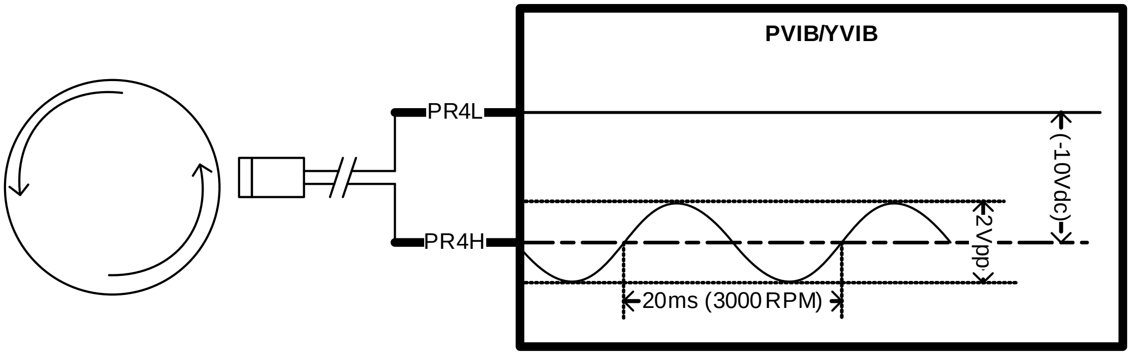
TMR_DiffLimt – TMR Voter Disagreement Detection Diagnostic alarm threshold for VIBn value. Value is expressed as absolute difference in EU.

SysLimit#, SysLim#Enabl, SysLim#Latch, SysLim#Type – See System Limits feature

Note FilterType, Fltrhpattn, Filtrhpcutoff, Fltrlpattn, Filtrlpcutoff – Unused for this sensor type.

Vibration Displacement Application Example

In the following figure (*Vibration Displacement Sensor*), Proximitor voltage inputs to a PVIB/YVIB application are measured at the terminal board screws. Assume this sensor is connected to Channel 4 as a VibProx input (no Keyphasor).



Vibration Displacement Sensor

Example Proximitor Specifications

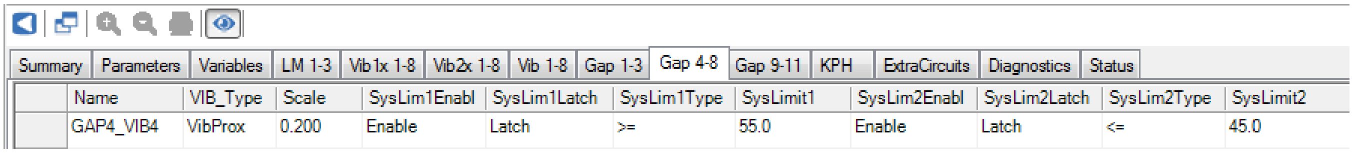
Scale Factor	200mV/mil
Nominal Gap Setting	50 mils

We will configure Channel 4 for the following behaviors:

- Return GAP4_VIB4 and VIB4 signals as mils.
- Set SysLim1GAP4 to LATCH True if GAP4_VIB4 ≥ 55 mils.
- Set SysLim2GAP4 to LATCH True if GAP4_VIB4 ≤ 45 mils.
- Set SysLim1VIB4 to True if VIB4 ≥ 8 mils
- Set SysLim2VIB4 to LATCH True if VIB4 ≥ 15 mils

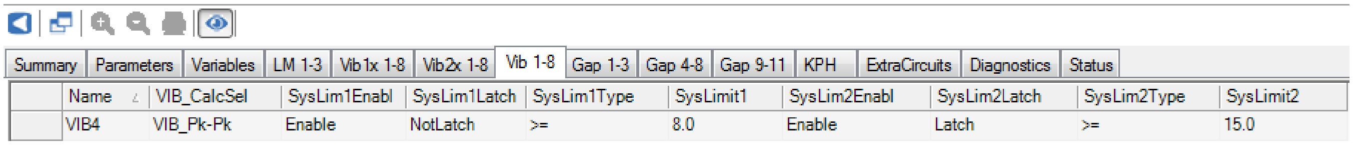
➢ To configure GAP4_VIB4

1. From the ToolboxST Component Editor, navigate to the **Gap 4-8** tab.
2. Select GAP4_VIB4, and click the *Show Advanced Parameters* icon.
3. Configure it to match the following example.



Name	VIB_Type	Scale	SysLim1Enabl	SysLim1Latch	SysLim1Type	SysLimit1	SysLim2Enabl	SysLim2Latch	SysLim2Type	SysLimit2
GAP4_VIB4	VibProx	0.200	Enable	Latch	>=	55.0	Enable	Latch	<=	45.0

4. Click the **Vib 1-8** tab.
5. Select VIB4 and click the *Show Advanced Parameters* icon.
6. Configure it to match the following example.



Name	VIB_CalcSel	SysLim1Enabl	SysLim1Latch	SysLim1Type	SysLimit1	SysLim2Enabl	SysLim2Latch	SysLim2Type	SysLimit2
VIB4	VIB_Pk-Pk	Enable	NotLatch	>=	8.0	Enable	Latch	>=	15.0

If the PVIB firmware is receiving the data successfully after competing this configuration, then the following occurs:

• Gap values are passed through a 2-pole, low-pass filter with a cutoff frequency of 8 Hz. This will attenuate the 50Hz, 2Vpp vibration by nearly 40:1, and the DC component of 10Vdc will be unaffected. The DC wave will be converted to 50mils, and the 40:1 reduced AC wave will be converted to ±0.125 mils, so the GAP4_VIB4 value will be 50 ± 0.125 mils.
• SysLim1GAP4 and SysLim2GAP4 are false, since ($45.0 \leq 49.875$) and ($50.125 \leq 55.0$).
• Vibration Displacement is unaffected by the DC component of the signal. The 50Hz, 2Vpp AC portion will be passed through a peak detection with 160 ms scan period, which will capture 8 cycles. The Peak-to-Peak value will return 2Vpp, which will be converted to 10mils, so VIB4 value will be 10mils.
• SysLim1VIB4 will be true, since VIB1 $\geq$ 8.0 mils. SysLim2VIB4 is false.

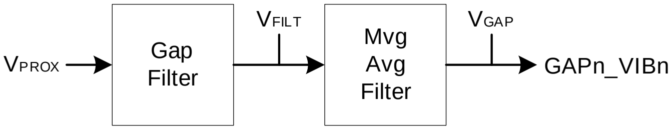
16.4.3.4 Velocity

Inputs 1-8 support Velomitors, Seismeic velocity, and Accelerometers with integrated outputs to collect wideband velocity. Inputs 1-3 also collect velocity magnitude relative to a specified rotor speed. In LM turbine applications, Velocity sensors are mounted on bearing housings or machine casing to provide measurements of vibration. Tracking filters for Inputs 1-3 can provide the magnitude of vibration at a specified frequency.

Velocity Input Processing

GAPn_VIBn – Sensor biasing voltage in Volts.

Gap values are filtered through a 2-pole, low-pass filter with a fixed cutoff frequency of 8 Hz. The output of the gap filter is passed through a rolling average filter prior to scaling. For Velocity sensors, the gap value is not scaled, and it will remain in Volts. This value can be used to monitor sensor health.



VIBn – Wideband Velocity (½*pk-pk or RMS) in engineering units (EU).

Wideband velocity information is passed through 1-pole, high-pass filter with a fixed cutoff frequency of .1Hz. This removes static information prior to wideband filtering. This data is passed through the wideband filter, which can be configured as a low-pass, high-pass, or band-pass filter. The high-pass and low-pass filters can be configured for 2, 4, 6, 8, or 10 pole Butterworth filters with a user-defined cutoff (-3dB) point.

Attention

10-pole filters are not available with PVIBH1A modules.

Wideband Filters are not executed for VibLMAccel sensors in PVIBH1A modules.

RMS Velocity is not available with PVIBH1A modules.

Depending on the value of the VIB_CalcSel for each input, the filtered data will be used to provide Peak velocity within the scan period, or RMS Velocity within the scan period.

For Peak velocity calculations, the wideband filter output is sent through a variable length peak detection function. The length of the peak detection is determined by the Keyphasor 1 detected speed in RPM.

The output of the peak detection function (VPK) is passed through an adjustable 1-pole, low-pass filter prior to scaling. VPK is converted from Volts to EU.

Note For PVIBH1B systems, a lower latency peak detection function can be enabled by changing the OperatingMode parameter to Enhanced. This function will update every frame, instead of every scan period. See Enhanced Vibration Algorithms for additional information.

Wideband vibration information is passed through a variable scan period peak detection function. The length of the peak detection is determined by the Keyphasor 1 detected speed in RPM.

Wideband Vibration Scan Period

Shaft speed (RPM)	Scan period (ms)
0 – 60	160
60-480	2000
480-2250	250
>2250	160

Attention

Peak Detection functions and Capture Buffers always uses RPM_KPH1 speed.

The data in the buffer is used to compute an RMS voltage (VRMS) over that capture length, which is passed through an adjustable 1-pole, low-pass filter prior to scaling. VRMS is converted from Volts to EU.

Note Sensors monitoring velocity typically measure RMS. Peak calculations can be used instead for legacy applications.

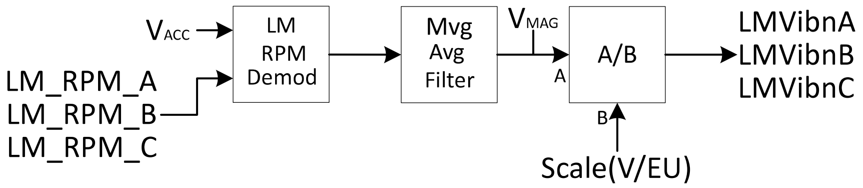
Note RMS calculations are only available with PVIBH1B / YVIBS1B systems, and can only be enabled by changing the OperatingMode parameter to Enhanced.

LMVibnA, LMVibnB, LMVibnC – Magnitude of 1X harmonic relative to specified rotor shaft in Engineering Units (EU). This function is available for Inputs 1-3 only.

1X LM Tracking Filters measure the ½*pk-pk velocity component at a specified shaft speed in RPM. The PVIB/YVIB module receives the shaft speed through the variables LM_RPM_A (for LMVib1A, LMVib2A, and LMVib3A), LM_RPM_B (for LMVib1B, LMVib2B, and LMVib3B), and LM_RPM_C (for LMVib1C, LMVib2C, and LMVib3C). The calculation is the same for all 9 inputs, with only the input channel or shaft speed source changing. Values are converted from Volts to EU.

Attention

PVIBH1A only supports the 1xLM tracking filters in VibLMAccel.



SysLim1GAPn, SysLim2GAPn – System Limit status for GAPn_VIBn value as True/False.
SysLim1VIBn, SysLim2VIBn – System Limit status for VIBn value as True/False. SysLim1ACCn, SysLim2ACCn – System Limit status for LMVibnA/B/C value as True/False.
ACC1, ACC2, and ACC3 correspond to LMVib1A, LMVib1B, and LMVib1C.
ACC4, ACC5, and ACC6 correspond to LMVib2A, LMVib2B, and LMVib2C.
ACC7, ACC8, and ACC9 correspond to LMVib3A, LMVib3B, and LMVib3C.

Velocity Input Configuration

GAPn_VIBn:

VibType - VibLmAccel, VibVelomitor, and VibSeismic are used for Velocity.

Attention

VibLmAccel does not support wideband filtering in the PVIBH1A.

VibVelomitor and VibSeismic do not support LM 1X Tracking Filters in the PVIBH1A.

Scale – Conversion from Volts to engineering units (EU). Typically, units are Volts/ips.

LMlpcutoff – LM 1X Tracking Filter low-pass cutoff. Effective LM 1X Tracking Filter bandwidth is twice the value of this field.

TMR_DiffLimt – TMR Voter Disagreement Detection Diagnostic alarm threshold for GAPn_VIBn value. Value is expressed as absolute difference in Volts.

GnBiasOvride, Gain, Snsr_Offset – See Gain/Bias Override

SysLimit#, SysLim#Enabl, SysLim#Latch, SysLim#Type – See System Limits feature

Note Scale_Off – Unused for this sensor type.

VIBn:

VIB_CalcSel – Select calculation method for VIBn value between Peak Velocity and RMS Velocity.

Note Sensors monitoring velocity typically measure RMS. Legacy PVIB applications will use Peak Velocity.

Note If OperatingMode is Legacy, this value is ignored and legacy Peak-to-Peak algorithm is used.

Attention

VIB_RMS is not supported by the PVIBH1A / YVIBS1A.

VibLMAccel does not support Wideband Filters in PVIBH1A / YVIBS1A.

10-pole filters are not supported in PVIBH1A / YVIBS1A.

FilterType – Select Wideband Filter type for Velocity data. Selections are None, Lowpass, Highpass, Bandpass.

Filtrhpcutoff, Filtrlpcutoff – Cutoff (-3dB) point for high-pass and low-pass filters, respectively.

Fltrhpattn, Fltrlpattn – Attenuation for high-pass and low-pass filters, expressed as number of poles to use in Butterworth filters. Selections are 2-pole, 4-pole, 6-pole, 8-pole, and 10-pole.

TMR_DiffLimt – TMR Voter Disagreement Detection Diagnostic alarm threshold for VIBn value. Value is expressed as absolute difference in EU.

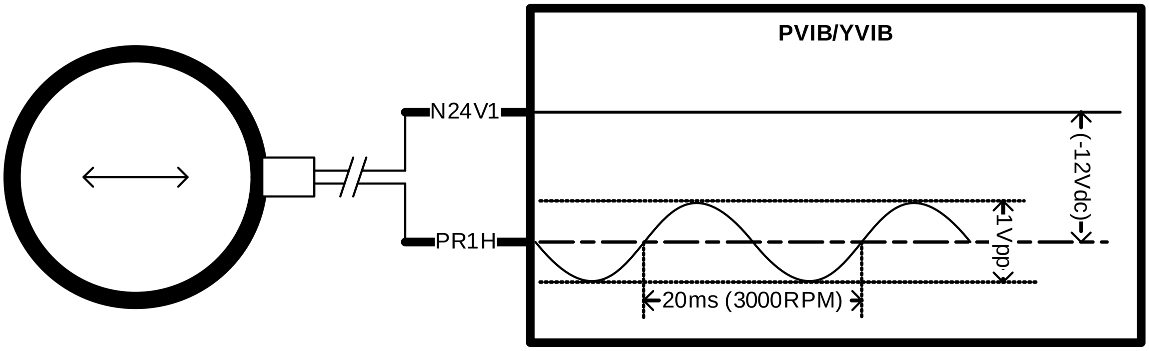
SysLimit#, SysLim#Enabl, SysLim#Latch, SysLim#Type – See System Limits feature

LMVibnA, LMVibnB, LMVibnC:

TMR_DiffLimt – TMR Voter Disagreement Detection Diagnostic alarm threshold for LMVibnA/B/C value. Value is expressed as absolute difference in EU.

SysLimit#, SysLim#Enabl, SysLim#Latch, SysLim#Type – See System Limits feature

Velocity Application Example



In this example, Velomitor voltage inputs to a PVIB/YVIB application are measured at the terminal board screws. Assume this sensor is connected to Channel 1 as a VibVelomitor input.

Example Velomitor Specifications

Scale Factor	100mV/ips
Frequency Response	6 Hz to 750 Hz

We will configure Channel 1 for the following behaviors:

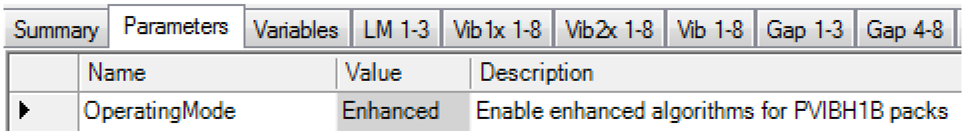
- Utilize the RMS Velocity algorithm for computing VIB1 signal.

Note RMS Computation is not available with PVIBH1A systems. Refer to Peak Velocity mode.

- Return VIB1 signal in inches/sec.
- Apply 8-pole low-pass and high-pass wideband filters to pass only inputs within Velomitor frequency response.
- Set SysLim1VIB1 to True if VIB1 $\geq$ 3 inches/sec
- Set SysLim2VIB1 to LATCH True if VIB1 $\geq$ 5 inches/sec
- Utilize LM_RPM_A to return LMVib1A as Peak Velocity at shaft speed (3000RPM) with a filter bandwidth of 5Hz.

Note LM 1X Tracking Filters will not operate with PVIBH1A for Velomitor sensors.

Navigate to “Parameters” tab. Set OperatingMode parameter to Enhanced.

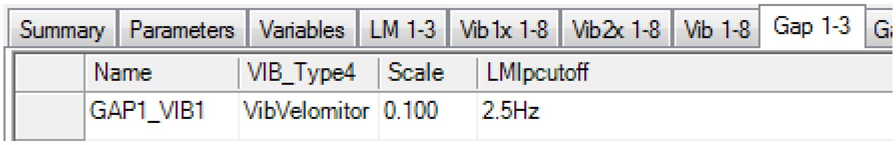


Name	Value	Description
OperatingMode	Enhanced	Enable enhanced algorithms for PVIBH1B packs

Navigate to “Gap 1-3” tab. Select GAP1_VIB1.

Set VIB_Type parameter to VibVelomitor.
Set Scale to “0.100” (Units are V/ips).

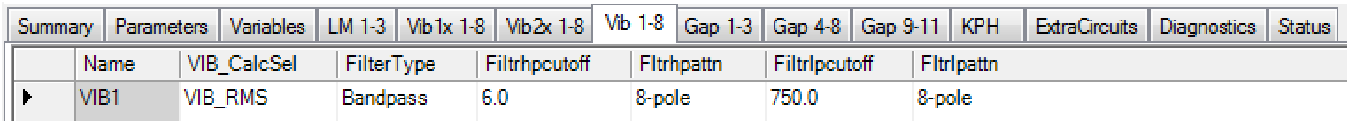
Set LMlpcutoff parameter to 2.5Hz. If the LM 1X Tracking Filter is not desired, then this setting does not matter.



Name	VIB_Type4	Scale	LMlpcutoff
GAP1_VIB1	VibVelomitor	0.100	2.5Hz

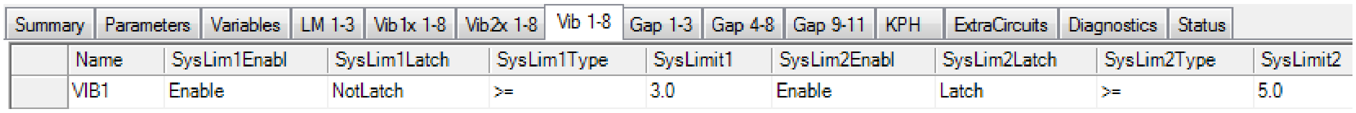
Navigate to the **Vib 1-8**tab. Select VIB1.

Set VIB_CalcSel parameter to VIB_RMS.
Set FilterType to Bandpass. Set Filtrhpcutoff to “6.0” Hz.
Set Filtrlpcutoff to “750.0” Hz.
Set Fltrhpattn and Fltrlpattn to 8-pole.



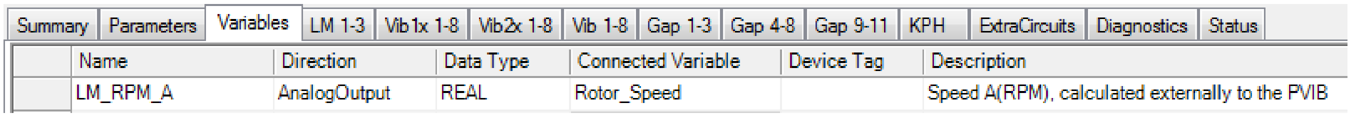
Name	VIB_CalcSel	FilterType	Filtrhpcutoff	Fltrhpattn	Filtrlpcutoff	Fltrlpattn
VIB1	VIB_RMS	Bandpass	6.0	8-pole	750.0	8-pole

Click to Show Advanced Parameters.
Set SysLim1Enabl and SysLim2Enabl parameters to Enable.
Set SysLim1Latch to NotLatch and SysLim2Latch to Latch.
Set SysLim1Type and SysLim2Type to “>=”.
Set SysLim1 to “3.0” ips and SysLimit2 to “5.0” ips.



Name	SysLim1Enabl	SysLim1Latch	SysLim1Type	SysLimit1	SysLim2Enabl	SysLim2Latch	SysLim2Type	SysLimit2
VIB1	Enable	NotLatch	>=	3.0	Enable	Latch	>=	5.0

Navigate to the **Variables** tab. Select LM_RPM_A and attach a variable containing the rotor speed of 3000 RPM to it. If the LM 1X Tracking Filter is not desired, omit this step.



Name	Direction	Data Type	Connected Variable	Device Tag	Description
LM_RPM_A	AnalogOutput	REAL	Rotor_Speed		Speed A(RPM), calculated externally to the PVIB

If the PVIB firmware is correctly receiving the data, we would expect:

- Gap values are passed through a 2-pole, low-pass filter with a cutoff frequency of 8 Hz. This will attenuate the 50Hz, 1Vpp vibration by nearly 40:1, and the DC component of -12Vdc will be unaffected. Since the units for GAP1_VIB1 are always Volts, and the 40:1 reduced AC wave will be ±0.025 volts, the GAP1_VIB1 value will be -12 ± 0.025 Volts.
- For Vib values, the DC removal filter will eliminate the DC component of -12 V. The 50Hz, 1Vpp AC portion will pass through the wideband filter unaffected and be sent to a 160ms capture window, which will capture 8 cycles. The RMS value computed for this input (ideal sine wave) will return .353VRMS, which will be converted to inches/sec, so VIB1 value will be 3.53 inches/sec. • SysLim1VIB1 will be true, since VIB1 ≥ 3.0 ips. SysLim2VIB1 is false.
- LMVib1A value is the magnitude of the 1X harmonic of the rotor speed in LM_RPM_A, which is 3000RPM. Since the input wave is an ideal sine wave with a frequency of 3000RPM, the value of LMVib1A will be 5.0 inches/sec.

16.4.3.5 Combustion Dynamics Monitoring (CDM)

Inputs 1-8 support CDM sensors to collect wideband dynamic pressure. Inputs 1-3 also collect dynamic pressure magnitude relative to a specified frequency in RPM. Combustion Dynamics applications rely on the higher bandwidth and enhanced algorithms which are only implemented in the PVIBH1B/YVIBS1B.

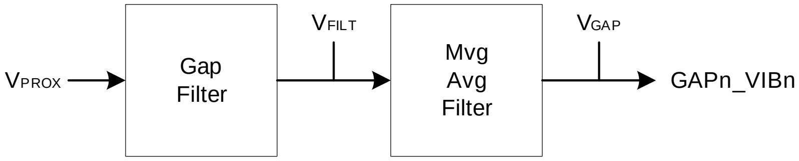
Attention

CDM Sensors are only supported on the PVIBH1B/YVIBS1B.

CDM Input Processing

GAPn_VIBn – Sensor biasing voltage in Volts.

Gap values are filtered through a 2-pole, low-pass filter with a fixed cutoff frequency of 8 Hz. The output of the gap filter is passed through a rolling average filter prior to scaling. For CDM sensors, the gap value is not scaled, and it will remain in Volts. This value can be used to monitor sensor health.



VIBn – Wideband Dynamic Pressure (pk-pk or RMS) in engineering units (EU).

Wideband dynamic pressure information is passed through 1-pole, high-pass filter with a fixed cutoff frequency of .1Hz. This removes static pressure prior to wideband filtering. This data is passed through the wideband filter, which can be configured as a low-pass, high-pass, or band-pass filter. The high-pass and low-pass filters can be configured for 2, 4, 6, 8, or 10 pole Butterworth filters with a user-defined cutoff (-3dB) point.

Depending on the value of the VIB_CalcSel for each input, the filtered data will be used to provide pk-pk dynamic pressure within the scan period, or RMS dynamic pressure within the scan period.

For pk-pk dynamic pressure calculations, the wideband filter output is sent through a variable length pk-pk detection function. The length of the pk-pk detection is determined by the CDM_Scan_Period value in configuration.

The output of the pk-pk detection function (VPK-pk) is passed through an adjustable 1-pole, low-pass filter prior to scaling. VPK-pk is converted from Volts to EU.

Note A lower latency pk-pk detection function can be enabled by changing the **OperatingMode** parameter to Enhanced. This function will update every frame, instead of every scan period.

For RMS dynamic pressure calculations, the wideband filter output is captured into a variable length buffer. The length of the RMS calculation is determined by the CDM_Scan_Period value in configuration.

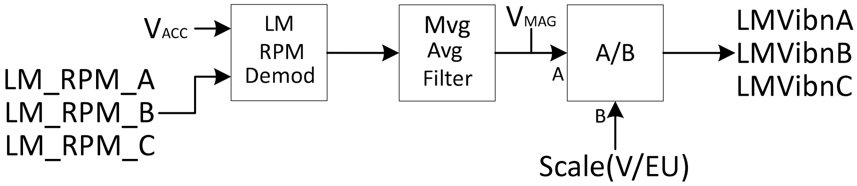
The data in the buffer is used to compute an RMS voltage (VRMS) over that capture length, which is passed through an adjustable 1-pole, low-pass filter prior to scaling (this filter cannot be disabled). VRMS is converted from Volts to EU.

Note Sensors monitoring dynamic pressure typically measure RMS. Peak calculations can be used instead for legacy applications.

Note RMS calculations are only available with PVIBH1B systems, and can only be enabled by changing the OperatingMode parameter to Enhanced. See Enhanced Vibration Algorithms for additional information.

LMVibnA, LMVibnB, LMVibnC – Magnitude of 1X harmonic relative to specified frequency (RPM) in Engineering Units (EU). This function is available for Inputs 1-3 only.

1X LM Tracking Filters measure the peak velocity component at a specified frequency in RPM. The PVIB module receives the frequency through the variables LM_RPM_A (for LMVib1A, LMVib2A, and LMVib3A), LM_RPM_B (for LMVib1B, LMVib2B, and LMVib3B), and LM_RPM_C (for LMVib1C, LMVib2C, and LMVib3C). The calculation is the same for all 9 inputs, with only the input channel or shaft speed source changing. Values are converted from Volts to EU.



SysLim1GAPn, SysLim2GAPn – System Limit status for GAPn_VIBn value as True/False.
SysLim1VIBn, SysLim2VIBn – System Limit status for VIBn value as True/False.
SysLim1ACCn, SysLim2ACCn – System Limit status for LMVibnA/B/C value as True/False.
ACC1, ACC2, and ACC3 correspond to LMVib1A, LMVib1B, and LMVib1C.
ACC4, ACC5, and ACC6 correspond to LMVib2A, LMVib2B, and LMVib2C.
ACC7, ACC8, and ACC9 correspond to LMVib3A, LMVib3B, and LMVib3C.

CDM Configuration

GAPn_VIBn:

VibType – CDM_BN_ChgAmp, CDM_PCB_ChgAmp are used for CDM applications.

Note CDM_PCB_ChgAmp expects a positively biased sensor and will use a pull-down to N28 for open circuit detection. CDM_BN_ChgAmp expects a negatively biased sensor, and will use a pull-up to P28. There is a TVBA jumper to select pull-up or pull-down voltage that must be in the correct position.

CDM_Probe_Gain – CDM Probe gain, typically expressed in pico-coulombs/PSI.
CDM_Amp_Gain – CDM Charge Amplifier gain, typically expressed in mV/ pico-coulomb.

Note CDM_Probe_Gain and CDM_Amp_Gain are hidden from view until a CDM Sensor is added.

LMlpcutoff – LM 1X Tracking Filter low-pass cutoff. Effective LM 1X Tracking Filter bandwidth is twice the value of this field.
TMR_DiffLimt – TMR Voter Disagreement Detection Diagnostic alarm threshold for GAPn_VIBn value. Value is expressed as absolute difference in Volts.
GnBiasOvride, Gain, Snsr_Offset – See Gain/Bias Override
SysLimit#, SysLim#Enabl, SysLim#Latch, SysLim#Type – See System Limits feature

Note Scale, Scale_Off – Unused for this sensor type.

VIBn:

VIB_CalcSel – Select calculation method for VIBn value between Peak Dynamic Pressure and RMS Dynamic Pressure.

Note Sensors monitoring dynamic pressure typically measure RMS.

If OperatingMode is Legacy, this value is ignored and legacy Peak algorithm is used.

FilterType – Select Wideband Filter type for Dynamic Pressure data. Selections are None, Lowpass, Highpass, Bandpass.

Filtrhpcutoff, Filtrlpcutoff – Cutoff (-3dB) point for high-pass and low-pass filters, respectively.

Fltrhpattn, Fltrlpattn – Attenuation for high-pass and low-pass filters, expressed as number of poles to use in Butterworth filters. Selections are 2-pole, 4-pole, 6-pole, 8-pole, and 10-pole.

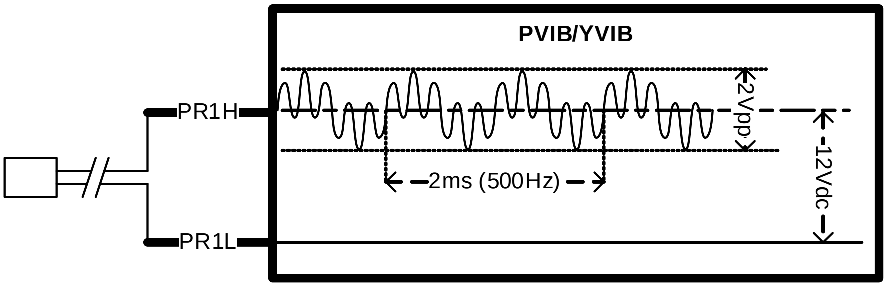
TMR_DiffLimt – TMR Voter Disagreement Detection Diagnostic alarm threshold for VIBn value. Value is expressed as absolute difference in EU.

SysLimit#, SysLim#Enabl, SysLim#Latch, SysLim#Type – See System Limits feature

LMVibnA, LMVibnB, LMVibnC:

TMR_DiffLimt – TMR Voter Disagreement Detection Diagnostic alarm threshold for LMVibnA/B/C value. Value is expressed as absolute difference in EU. SysLimit#, SysLim#Enabl, SysLim#Latch, SysLim#Type – See System Limits feature

CDM Application Example



In this example, PCB CDM voltage inputs to a PVIB/YVIB application are measured at the terminal board screws. Assume this sensor is connected to Channel 1 as a CDM_PCB_ChgAmp input.

For this example, the input waveform is two 1 VPK-PK pure tones (500Hz sine wave and 2500Hz sine wave) summed together. This is for illustrative purposes only, and is not indicative of true sensor inputs.

Example PCB Sensor Specifications

PCB Probe Gain	5.0 pC/PSI
PCB Amp Gain	20.0 mV/pC
Frequency Response	200 Hz – 4 kHz

We will configure Channel 1 for the following behaviors:

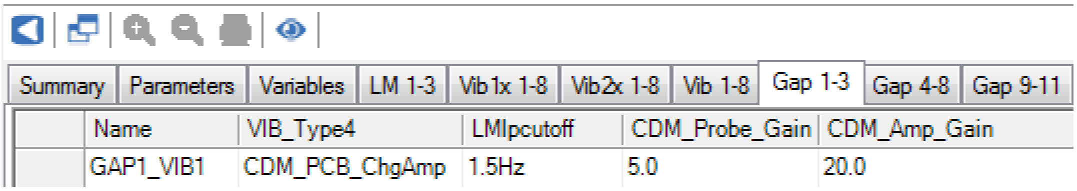
- Utilize the RMS Dynamic Pressure algorithm for computing VIB1 signal.
- Return VIB1 signal in PSI.
- Apply 10-pole low-pass and high-pass wideband filters to pass only inputs within PCB Sensor frequency response.
- Utilize LM_RPM_A to return LMVib1A as Peak Dynamic Pressure at 2500 Hz (150000 RPM = 2500 Hz * 60 RPM / Hz) with a filter bandwidth of 3Hz.

- Set CDM_Scan_Period to 640 ms

➢ To configure Channel 1

1. From the **Parameters** tab, set **OperatingMode** to Enhanced and set **CDM_Scan_Period** to 640 ms.

2. From the **Gap 1-3** tab, select GAP1_VIB1 and make the following configuration changes as displayed in the following screen.



Name	VIB_Type4	LMIpcutoff	CDM_Probe_Gain	CDM_Amp_Gain
GAP1_VIB1	CDM_PCB_ChgAmp	1.5Hz	5.0	20.0

Note These parameters will appear when a CDM sensor is selected in the VIB_Type parameter.

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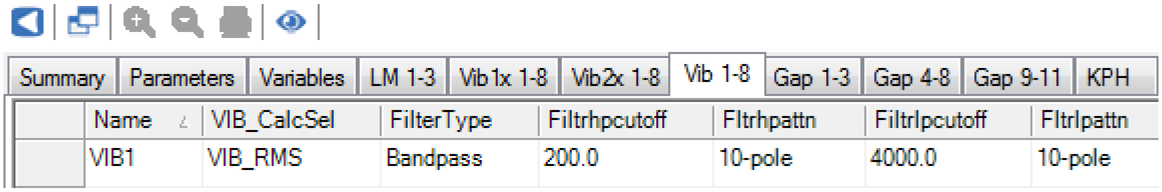
3. Navigate to the **Vib 1-8** tab. Select VIB1. Click to Show Advanced Parameters.

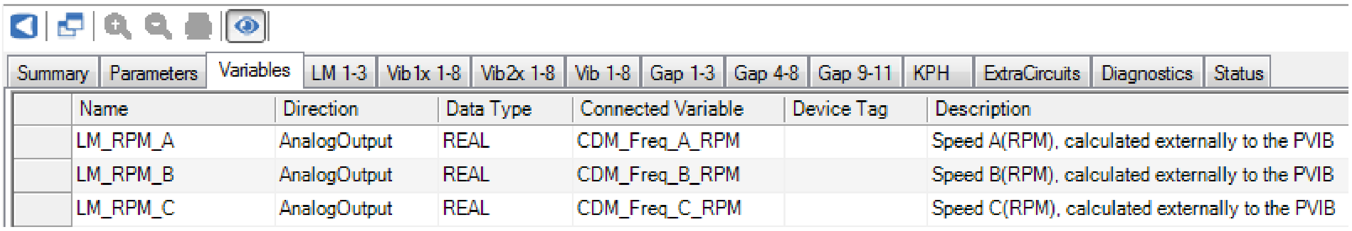
4. To set the Wideband filter, make the configuration changes as displayed in the following screen.



Name	VIB_CalcSel	FilterType	Filtrhpcutoff	Fltrhpattn	Filtrlpcutoff	Fltrlpattn
VIB1	VIB_RMS	Bandpass	200.0	10-pole	4000.0	10-pole

5. If the LM 1X Tracking Filter is desired, then navigate to the **Variables** tab. Select LM_RPM_A and attach a variable containing the 1x Harmonic frequency of 150000 RPM to it.

Note LM 1x Tracking Filter frequency input is always RPM, even for CDM applications. Be sure to convert the target frequency from Hertz to RPM.



Name	Direction	Data Type	Connected Variable	Device Tag	Description
LM_RPM_A	AnalogOutput	REAL	CDM_Freq_A_RPM		Speed A(RPM), calculated externally to the PVIB
LM_RPM_B	AnalogOutput	REAL	CDM_Freq_B_RPM		Speed B(RPM), calculated externally to the PVIB
LM_RPM_C	AnalogOutput	REAL	CDM_Freq_C_RPM		Speed C(RPM), calculated externally to the PVIB

If the PVIB firmware is receiving the data correctly after this configuration, then the following is expected:

• Gap values are passed through a 2-pole, low-pass filter with a cutoff frequency of 8 Hz. This will attenuate the AC waveform by at least 4000:1, and the DC component of 12VDC will be unaffected. Since the units for GAP1_VIB1 are always Volts, and the 4000:1 reduced AC wave will be ±0.0005 volts, the GAP1_VIB1 value will be -12 ± 0.0005 Volts.
• The DC removal filter will eliminate the DC component of -12V. The 500Hz, 1 VPK-PK and 2500Hz, 1 VPK-PK AC waves will pass through the wideband filter unaffected and be sent to a 160ms capture window, which will capture 80 cycles (scan period * frequency of the lowest principle). The RMS value computed for this input (sum of ideal sine waves) will return 0.5 V RMS, which will be converted to PSI. Therefore the VIB1 value will be 5.0 PSI RMS.
• LMVib1A value is the magnitude of the 1X harmonic of the rotor speed in LM_RPM_A, which is 2500Hz (150000 RPM). Since the input wave is the sum of two ideal sine waves, one of which is at 2500 Hz with a magnitude of 1 VPK-PK , the value of LMVib1A will be 10 PSIPK-PK.

16.4.4 Component Editor

16.4.4.1 Parameters

Parameter	Description	Choices
SystemLimits	Allows user to temporarily disable all system limit checks for testing purposes. Setting this parameter to Disable will cause a diagnostic alarm to occur.	Enable (default) Disable
OperatingMode	Legacy is the backwards compatibility mode for PVIBH1A Enhanced enables enhanced algorithms for PVIBH1B and YVIBS1B that are not compatible with PVIBH1A, including Low Latency Peak-Peak Algorithm and Vibration RMS Algorithm	Legacy (default) Enhanced
Vib_PP_Fltr	First order filter time constant (sec) — cannot be disabled	0.01 to 2 (default is 0.10)
MaxVolt_Prox	Maximum Input Volts (pk-neg), healthy Input, Prox	-4 to 0 (default is -1.5)
MinVolt_Prox	Minimum Input Volts (pk-neg), healthy Input, Prox	-24 to -16 (default is -18.5)
MaxVolt_KP	Maximum Input Volts (pk-neg), healthy Input, Keyphasor	-4 to 0 (default is -1.5)
MinVolt_KP	Minimum Input Volts (pk-neg), healthy Input, Keyphasor	-24 to -16 (default is -22.0)
MaxVolt_Seis	Maximum Input Volts (pk-pos),healthy Input,Seismic:Values > 1.25 require use of GnBiasOvride	0 to 2.75 (default is 1.0)
MinVolt_Seis	Minimum Input Volts (pk-neg),healthy Input,Seismic:Values < -1.25 require use of GnBiasOvride	-2.75 to 0 (default is -1.0)
MaxVolt_Acc	Maximum Input Volts (pk),healthy Input,Accel	-12 to 1.5 (default is -8.5)
MinVolt_Acc	Minimum Input Volts (pk-neg),healthy Input,Accel	-24 to -1 (default is -11.5)
MaxVolt_Vel	Maximum Input Volts (pk),healthy Input,Velomitor	-12 to 1.5
MinVolt_Vel	Minimum Input Volts (pk-neg),healthy Input,Velomitor	-24 to -1
MaxVolt_CDM_BN	Maximum Input Volts (pk),healthy Input,CDM Bently Nevada	-12 to 24
MinVolt_CDM_BN	Minimum Input Volts (pk-neg),healthy Input,CDM Bently Nevada	-24 to 12
MaxVolt_CDM_PCB	Maximum Input Volts (pk),healthy Input,CDM PCB	-12 to 24
MinVolt_CDM_PCB	Minimum Input Volts (pk-neg),healthy Input,CDM PCB	-24 to 12
CDM_Scan_Period	The scan period for CDM sensor inputs in seconds Only assign as 0.01 increments	0.01 to 2.0

16.4.4.2 Variables

Variables	Description	Direction and Datatype
L3DIAG_xxxx_x	I/O Pack Diagnostic Indicator where Pxxx or Yxxx is the name of the I/O pack and R, S, or T is the redundancy of pack	Input BOOL
LINK_OK_xxxx_x	IONet Link Okay Indicator where Pxxx or Yxxx is the name of the I/O pack and R, S, or T is the redundancy	Input BOOL
ATTN_xxxx_x	I/O Pack Status Indicator where Pxxx or Yxxx is the name of the I/O pack and R, S, or T is the redundancy	Input BOOL
PS18V_xxxx_x	I/O Pack 18 V Power Supply Indication where Pxxx or Yxxx is the name of the I/O pack and R, S, or T is the redundancy	Input BOOL
PS28V_xxxx_x	I/O Pack 28 V Power Supply Indication where Pxxx or Yxxx is the name of the I/O pack and R, S, or T is the redundancy	Input BOOL
IOPackTmpr_	I/O Pack Temperature at the processor where R, S, or T is the redundancy	Input BOOL
RPM_KPH1	Speed (RPM)of KP#1,calculated from input#13	Analog Input REAL
RPM_KPH2	Speed (RPM)of KP#2,calculated from input#12 (PVIBH1B only)	Analog Input REAL
LM_RPM_A	Speed A(RPM), calculated externally to the I/O Pack	Analog Output REAL
LM_RPM_B	Speed B(RPM), calculated externally to the I/O Pack	Analog Output REAL
LM_RPM_C	Speed C(RPM), calculated externally to the I/O Pack	Analog Output REAL
SysLim1GAPx where x = 1 to 13	Boolean set TRUE if System Limit 1 exceeded for Gap x input	Input BOOL
SysLim2GAPx where x = 1 to 13	Boolean set TRUE if System Limit 2 exceeded for Gap x input	Input BOOL
SysLim1VIBx where x = 1 to 8	Boolean set TRUE if System Limit 1 exceeded for Vib x input	Input BOOL
SysLim2VIBx where x = 1 to 8	Boolean set TRUE if System Limit 2 exceeded for Vib x input	Input BOOL
SysLim1ACCx where x = 1 to 9	Boolean set TRUE if System Limit 1 exceeded for Accelerometer x input	Input BOOL
SysLim2ACCx where x = 1 to 9	Boolean set TRUE if System Limit 2 exceeded for Accelerometer x input	Input BOOL

16.4.4.3 Probe Nominal Settings

Probe Type	Gain †	Snsr_Offset (Vdc)	Scale (typical value)
Proximity	1x	9	200 mv/mil
Seismic	4x	0	150 mv/ips
Velomitor	2x	12	100 mv/ips
Accelerometer	2x	10	150 mv/ips
Keyphasor	1x	9	200 mv/mil
Bently Nevada CDM	2x	10	170 mv/psi
PCB CDM	2x	-12	170 mv/psi
†These are the default settings used if GnBiasOvride=Disable.			

16.4.4.4 LM 1–3

[ ] = defaults

Name	Direction	Data Type	Description	TMR_DiffLimit	SysLim1Enabl	SysLim1Latch	SysLimit1Type	SysLimit1
LMVib#A ↓ LMVib#C	AnalogInput	REAL	Magnitude of 1X harmonic relative to LM_RPM_A, B, or C calculated from input#1, 2, or 3 (9 total inputs)	Difference Limit for Voted TMR Inputs in Volts or Mils [2] -100 to 100	Enable System Limit 1 [Disable], Enable	Latch the alarm [Latch], NotLatch	System Limit 1 Check Type [>=] , <=	System Limit 1 – Vibration in mils (prox) or Inch/sec (seismic,acel) [50] -100 to 100

SysLim2Enabl	SysLim2Latch	SysLim2Type	SysLimit2
Enable System Limit 2 [Disable], Enable	Latch the alarm [Latch], NotLatch	System Limit 2 Check Type [>=] , <=	System Limit 2 – Vibration in mils (prox) or Inch/sec (seismic,acel) [0] -100 to 100

16.4.4.5 Vib1x 1-8

Name	Direction	Data Type	Description
VIB_1X1	AnalogInput	REAL	Magnitude of 1X harmonic relative to key phasor speed calculated from input#1
↓	↓	↓	↓
VIB_1X8	AnalogInput	REAL	Magnitude of 1X harmonic relative to key phasor speed calculated from input#8
Vib1xPH1	AnalogInput	REAL	Angle of 1X harmonic relative to key phasor calculated from input#1
↓	↓	↓	↓
Vib1xPH8	AnalogInput	REAL	Angle of 1X harmonic relative to key phasor calculated from input#8

16.4.4.6 Vib2x 1-8

Name	Direction	Data Type	Description
VIB_2X1	AnalogInput	REAL	Magnitude of 2X harmonic relative to key phasor speed calculated from input#1
↓	↓	↓	↓
VIB_2X8	AnalogInput	REAL	Magnitude of 2X harmonic relative to key phasor speed calculated from input#8
Vib2xPH1	AnalogInput	REAL	Angle of 2X harmonic relative to key phasor calculated from input#1
↓	↓	↓	↓
Vib2xPH8	AnalogInput	REAL	Angle of 2X harmonic relative to key phasor calculated from input#8

16.4.4.7 Vib 1-8

[ ] = defaults

Name	Direction	Data Type	Description	VIB_CalcSel	TMR_DiffLimt	Filter Type	Filtrhpcutoff
VIB1	AnalogInput	REAL	Vibration displacement (pk-pk) or velocity (pk), AC component of input#1	[VIB_Pk-Pk] Vib_RMS ‡	Difference Limit for Voted TMR Inputs in Volts or Mils [2] -100 to 100	Filter used for Velomitor and Seismic only [None], Low Pass, High Pass, Band Pass	High Pass 3db point (cutoff in Hz) [6] 4 to 300
↓	↓	↓	↓				
VIB8	AnalogInput	REAL	Vibration displacement (pk-pk) or velocity (pk), AC component of input#8				
‡Vib_RMS is only valid when OperatingMode is Enhanced and when using a PVIBH1B or YVIBS1B							

fltrlpattn	Filtrlpcutoff	fltrlppattn	SysLim1Enabl	SysLim1Latch	SysLim1Type	SysLimit1
Slope or attenuation of high pass filter after cutoff [2-pole], 4-pole, 6-pole, 8-pole, 10-pole	Low Pass 3db point (cutoff in Hz) [500] 15 to 4300	Slope or attenuation of low pass filter after cutoff [2-pole] 4-pole, 6-pole, 8-pole, 10-pole	Enable System Limit 1 [Disable], Enable	Latch the alarm [Latch], NotLatch	System Limit 1 Check Type [>=], <=	System Limit 1 – GAP in negative volts (Velomitor) or positive mils (Prox) [50] -100 to 100

SysLim2Enabl	SysLim2Latch	SysLim2Type	SysLimit2
Enable System Limit 2 [Disable], Enable	Latch the alarm [Latch], NotLatch	System Limit 2 Check Type [>=], <=	System Limit 2 – GAP in negative volts (Velomitor) or positive mils (Prox) [0] -100 to 100

16.4.4.8 Gap 1-3

[ ] = defaults

†is only valid with PVIBH1B or YVIBS1B

‡ LM Tracking Filter magnitude value may be inaccurate at 160, 320 ms frame periods.

Name	Direction	Data Type	Description	VIB_Type4	Scale	Scale_Off	TMR_ DiffLimit
GAP1_VIB1	AnalogIn-put	REAL	Average Air Gap (for Prox) or DC volts(for others),DC component of input#1	Type of vibration probe, group 4 †CDM_BN_ChgAmp, †CDM_PCB_ ChgAmp, PosProx, [Unused], ‡VibLMAccel, VibProx, VibProx-KPH1, VibProx-KPH2, VibSeismic, VibVelomitor	Volts/-mil or Volt-s/ips [0.2] 0 to 2	Scale offset for Prox position only, in mils [0] 0 to 90	Difference Limit for Voted TMR Inputs in Volts or Mils [2] -100 to 100
GAP2_VIB2	AnalogIn-put	REAL	Average Air Gap (for Prox) or DC volts(for others),DC component of input#2				
GAP3_VIB3	AnalogIn-put	REAL	Average Air Gap (for Prox) or DC volts(for others),DC component of input#3				

GnBiasOvride	Snsr_Offset	Gain	LMIpcutoff	SysLim1Enabl	SysLim1Latch	SysLim1Type	SysLimit1
Gain Bias Override [Disable], Enable	Amount of bias voltage (dc) to remove from input signal used to max. A/Ds signal range used only when GnBiasOvride is enabled [10] ±13.5	Resolution of input signal (net gain unchanged), select based on expected range, use only if GnBiasOvride is enabled [1x], 2x, 4x, 8x	Low pass 3dB point (cutoff Hz) for LM tracking filters 1.5Hz, 2.0Hz, [2.5Hz], 3.0Hz, 3.5Hz, 4.0Hz, 4.5Hz, 5.0Hz	Enable System Limit 1 [Disable], Enable	Latch the alarm [Latch], NotLatch	System Limit 1 Check Type [>=] , <=	System Limit 1 – GAP in negative volts (Velomitor) or positive mils (Prox) [90] -100 to 100

SysLim2Enabl	SysLim2Latch	SysLim2Type	SysLimit2	CDM_Probe_Gain	CDM_Amp_Gain
Enable System Limit 2 [Disable], Enable	Latch the alarm [Latch], NotLatch	System Limit 2 Check Type [>=] , <=	System Limit 2 – GAP in negative volts (Velomitor) or positive mils (Prox) [10] -100 to 100	PCB Probe Gain, pico-coulombs per psi [17] 1 to 100	PCB Charge amplifier Gain, millivolts per pico-coulomb [10] 1 to 100

16.4.4.9 Gap 4-8

[ ] = defaults
†is only valid with PVIBH1B or YVIBS1B

Name	Direction	Data Type	Description	VIB_Type	Scale	Scale_Off	TMR_ DiffLimit
GAP4_VIB4	AnalogInput	REAL	Average Air Gap (for Prox) or DC volts(for others),DC component of input#4	Type of vibration probe, group 1 †CDM_BN_ChgAmp, †CDM_PCB_ ChgAmp, PosProx, [Unused], VibLMAccel, VibProx, VibProx-KPH1, VibProx-KPH2, VibSeismic, VibVelomitor	Volts/-mil or Volt-s/ips [0.2] 0 to 2	Scale offset for Prox position only, in mils [0] 0 to 90	Difference Limit for Voted TMR Inputs in Volts or Mils [2] -100 to 100
↓	↓	↓	↓				
GAP8_VIB8	AnalogInput	REAL	Average Air Gap (for Prox) or DC volts(for others),DC component of input#8				

GnBiasOvride	Snsr_Offset	Gain	SysLim1Enabl	SysLim1-Latch	SysLim1Type	SysLimit1
Gain Bias Override [Disable], Enable	Amount of bias voltage (dc) to remove from input signal used to max. A/Ds signal range used only when GnBiasOvride is enabled [10] ±13.5	Resolution of input signal (net gain unchanged), select based on expected range, use only if GnBiasOvride is enabled [1x], 2x, 4x, 8x	Enable System Limit 1 [Disable], Enable	Latch the alarm [Latch], NotLatch	System Limit 1 Check Type [>=] , <=	System Limit 1 – GAP in negative volts (Velomitor) or positive mils (Prox) [90] -100 to 100

SysLim2Enabl	SysLim2Latch	SysLim2Type	SysLimit2	CDM_Probe_Gain	CDM_Amp_Gain
Enable System Limit 2 [Disable], Enable	Latch the alarm [Latch], NotLatch	System Limit 2 Check Type [>=] , <=	System Limit 2 – GAP in negative volts (Velomitor) or positive mils (Prox) [10] -100 to 100	PCB Probe Gain, pico-coulombs per psi [17] 1 to 100	PCB Charge amplifier Gain, millivolts per pico-coulomb [10] 1 to 100

16.4.4.10 Gap 9-11

[ ] = defaults

Name	Direction	Data Type	Description	VIB_Type2	Scale	Scale_Off	TMR_ DiffLimit
GAP9_POS1	AnalogInput	REAL	Average Air Gap,DC component of input#9	Sensor Type, group 2 [Unused], PosProx	Volts/mil or Volts/ips [0.2] 0 to 2	Scale offset for Prox position only, in mils [0] 0 to 90	Difference Limit for Voted TMR Inputs in Volts or Mils [2] -100 to 100
GAP10_POS2	AnalogInput	REAL	Average Air Gap,DC component of input#10				
GAP11_POS3	AnalogInput	REAL	Average Air Gap,DC component of input#11				

GnBiasOvride	Snsr_Offset	Gain	SysLim1Enabl	SysLim1Latch	SysLim1Type	SysLimit1
Gain Bias Override [Disable], Enable	Amount of bias voltage (dc) to remove from input signal used to max. A/Ds signal range used only when GnBiasOvride is enabled [10] ±13.5	Resolution of input signal (net gain unchanged), select based on expected range, use only if GnBiasOvride is enabled [1x], 2x, 4x, 8x	Enable System Limit 1 [Disable], Enable	Latch the alarm [Latch], NotLatch	System Limit 1 Check Type [>=] , <=	System Limit 1 – GAP in negative volts (Velomitor) or positive mils (Prox) [90] -100 to 100

SysLim2Enabl	SysLim2Latch	SysLim2Type	SysLimit2
Enable System Limit 2 [Disable], Enable	Latch the alarm [Latch], NotLatch	System Limit 2 Check Type [>=] , <=	System Limit 2 – GAP in negative volts (Velomitor) or positive mils (Prox) [10] -100 to 100

16.4.4.11 KPH

[ ] = defaults
† is only valid with PVIBH1B or YVIBS1B

Name	Direction	Data Type	Description	VIB_Type3	Scale	Scale_Off	TMR_ DiffLimit	KPH_Thrshld
GAP12_KPH2	AnalogInput	REAL	Average Air Gap,DC component of input#9	Sensor Type, group 3 [Unused], PosProx, † KeyPhasor	Volts/mil or Volts/ips [0.2] 0 to 2	Scale offset for Prox position only, in mils [0] 0 to 90	Difference Limit for Voted TMR Inputs in Volts or Mils [2] -100 to 100	Voltage difference from gap voltage where keyphasor triggers [2.0] 1.0 to 5.0
GAP13_KPH1	AnalogInput	REAL	Average Air Gap,DC component of input#10	Sensor Type, group 3 [Unused], PosProx, KeyPhasor				

KPH_Type	GnBiasOvride	Snsr_Offset	Gain	SysLim1Enabl	SysLim1Latch	SysLim1Type	SysLimit1
[Slot], Pedestal	Gain Bias Override [Disable], Enable	Amount of bias voltage (dc) to remove from input signal used to max. A/Ds signal range used only when GnBiasOvride is enabled [10] ±13.5	Resolution of input signal (net gain unchanged), select based on expected range, use only if GnBiasOvride is enabled [1x], ‡ 2x, 4x, ‡ 8x	Enable System Limit 1 [Disable], Enable	Latch the alarm [Latch], NotLatch	System Limit 1 Check Type [>=] , <=	System Limit 1 – GAP in negative volts (Velomitor) or positive mils (Prox) [90] -100 to 100

‡Gain 2x and Gain 8x are **Never** valid on GAP12_KPH2.

SysLim2Enabl	SysLim2Latch	SysLim2Type	SysLimit2
Enable System Limit 2 [Disable], Enable	Latch the alarm [Latch], NotLatch	System Limit 2 Check Type [>=] , <=	System Limit 2 – GAP in negative volts (Velomitor) or positive mils (Prox) [10] -100 to 100

16.4.5 PVIB or YVIB Diagnostics

Note Details of the individual diagnostics are available from the ToolboxST application. The diagnostic signals can be individually latched and then cleared from the ToolboxST Component Editor, or by using the RSTDIAG signal on SYS_ OUTPUTS block, or through the WorkstationST Alarm Viewer.

The I/O pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set
- Each vibration input has hardware limit checking based on preset (configurable) high and low levels near the end of the operating range. If this limit is exceeded, a logic signal is set. The logic signal, L3DIAG_xxxx, refers to the entire board. There are diagnostic alarms for this (Alarm 33-45).
- Each input has system limit checking based on configurable high and low levels. The Sys_Outputs block can be used to reset any latched system limits. System limits can be used to drive process alarms through users application code.

16.5 PVIB or YVIB Specific Diagnostic Alarms

The following alarms are specific to the PVIB or YVIB I/O pack.

32

Description Channel [ ] A/D Converter Calibration Failure

Possible Cause The I/O pack failed to auto-calibrate when powered on.

Solution Replace the I/O pack.

33-45

Description TVBA Analog Input [ ] exceeded limits

Possible Cause

- The terminal point voltage is outside of limits for the sensor type.
- The Bias level (DC offset), Gain, or sensor limits are improperly set for the sensor/channel.
- Open connection between sensor and terminal board

Solution

- Verify that the sensor configuration is correct.
- Check for the proper voltage at the terminal board point on the sensor.
- Check the electrical continuity between sensor and terminal board.
- Replace the I/O pack or terminal board.

46

Description Channel [ ] D/A Converter Calibration Failure

Possible Cause The board failed to auto-calibrate when powered on.

Solution Replace the I/O pack.

47

Description Initialization Error Detected

Possible Cause An I/O pack has failed.

Solution Replace the I/O pack.

48

Description Internal data transfer error - Expected ID [ ] Read ErrCntr/ID [ ]

Possible Cause There is an I/O pack failure or software process conflict that may be cleared by a hard reset.

Solution

- Cycle power on the I/O pack.
- Replace the I/O pack.

49

Description Internal hardware failure - Status [ ]

Possible Cause An I/O pack has failed.

Solution Replace the I/O pack.

50

Description Channel [ ] DC Isolation Test Failure

Possible Cause The I/O pack failed to auto-calibrate when powered on.

Solution Replace the I/O pack.

51

Description I/O pack processor failure - Status [ ]

Possible Cause The I/O pack failed.

Solution Replace the I/O pack.

52-64

Description TVBA Analog Input [ ] Open Circuit ([ ] Volts)

Possible Cause An open circuit has been detected on the terminal board based on the sensor type.

Solution

- Check the wiring between the terminal board and the sensor.
- Check the sensor for proper operation.
- Replace the terminal board.

65

Description Negative 28 Volt Power Low ([ ] Counts)

Possible Cause

- WNPS daughterboard failure (for TVBAH#A or S#A)
- Failure of N28 power supply on TVBAS2B or TVBAH#B
- I/O pack P28 voltage is low
- The terminal board has failed

Solution

- Check the power to the I/O pack.
- Replace the WNPS daughterboard.
- Replace the terminal board.
- Replace the I/O pack.

66

Description Dual Ethernets not supported with 10 ms frame rate

Possible Cause The second Ethernet port is connected, but not supported for a 10 ms frame rate with PVIBH1A.

Solution

- Remove the second Ethernet connection to the PVIBH1A.
- Increase the frame rate to 20ms.
- Upgrade to PVIBH1B.

67

Description Pack internal reference voltage out of limits

Possible Cause The I/O pack failed to auto-calibrate when powered on.

Solution Replace the I/O pack.

68

Description Internal daughterboard temperature limit exceeded ([ ] °F)

Possible Cause

- The cabinet temperature is too high.
- The I/O pack overheated.
- If the cabinet temperature is within the specified temperature limits, the I/O pack internal daughterboard temperature sensor may have failed.

Solution

- Check the environmental controls applied to the cabinet containing the I/O pack. Operation will continue correctly beyond these temperature limits, but long-term operation at elevated temperatures may reduce equipment life.
- If the I/O pack internal daughterboard temperature sensor failed, then replace the I/O pack.

69

Description Channels 1, 5, 9, 13 ADC Failure. Status [ ]

Possible Cause The I/O pack failed.

Solution Replace the I/O pack.

70

Description Channels 2,6,10 ADC Failure. Status [ ]

Possible Cause The I/O pack failed.

Solution Replace the I/O pack.

71

Description Channels 3,7,11 ADC Failure. Status [ ]

Possible Cause The I/O pack failed.

Solution Replace the I/O pack.

72

Description Channels 4,8,12 ADC Failure. Status [ ]

Possible Cause The I/O pack failed.

Solution Replace the I/O pack.

73

Description 1x2x Phase Calibration Level [ ] Failure on Channel [ ]

Possible Cause The I/O pack failed to auto-calibrate when powered on.

Solution Replace the I/O pack.

74

Description Current Operating Mode is incompatible with this hardware

Possible Cause The selected Operating Mode is not supported by this module. This is likely caused by installing a PVIBH1A to replace a PVIBH1B without updating ToolboxST. This alarm may be accompanied by Voter Disagreement diagnostics.

Solution

- Change the Operating Mode parameter to Legacy.
- Replace this module with a PVIBH1B.

75-87

Description Channel [ ] Sensor type is not supported with this hardware

Possible Cause The selected sensor type (VIB_Type) is unsupported by this module. This is likely caused by installing a PVIBH1A to replace a PVIBH1B without updating ToolboxST. This channel will default to Unused behavior.

Solution

- Change the VIB_Type for the indicated channel to a value supported by all hardware forms being used. Review the documentation to see which sensor types can be used for each hardware form.
- Replace this module with a PVIBH1B.

88-95

Description Channel [ ] Wideband Filters do not support [ ]-pole filter attenuation. Falling back to [ ]-pole filter attenuation.

Possible Cause The filter attenuation selection for Fltrhpattn and/or Fltrlpattn is not supported by this module. This is likely caused by installing a PVIBH1A to replace a PVIBH1B without updating ToolboxST. This channel will run with the closest match it can support, rather than disable the filter.

Solution

- Change the Fltrhpattn and/or Fltrlpattn for the indicated channel to a value supported by all the hardware forms being used. Review the documentation to see which attenuation values can be used for each hardware form.
- Replace this module with a PVIBH1B.

192-221

Description Input Signal [ ] Voting Mismatch, Local=[ ], Voted=[ ]

Possible Cause

- There is a voter disagreement between the R, S, and T I/O packs.
- The I/O pack is not seated on the terminal board correctly.
- The I/O pack has failed.

Solution

- Adjust the parameter **TMR_DiffLimt** or correct the cause of the difference.
- Re-seat the I/O pack to the terminal board.
- Replace the I/O pack.

16.6 TVBA Vibration Input

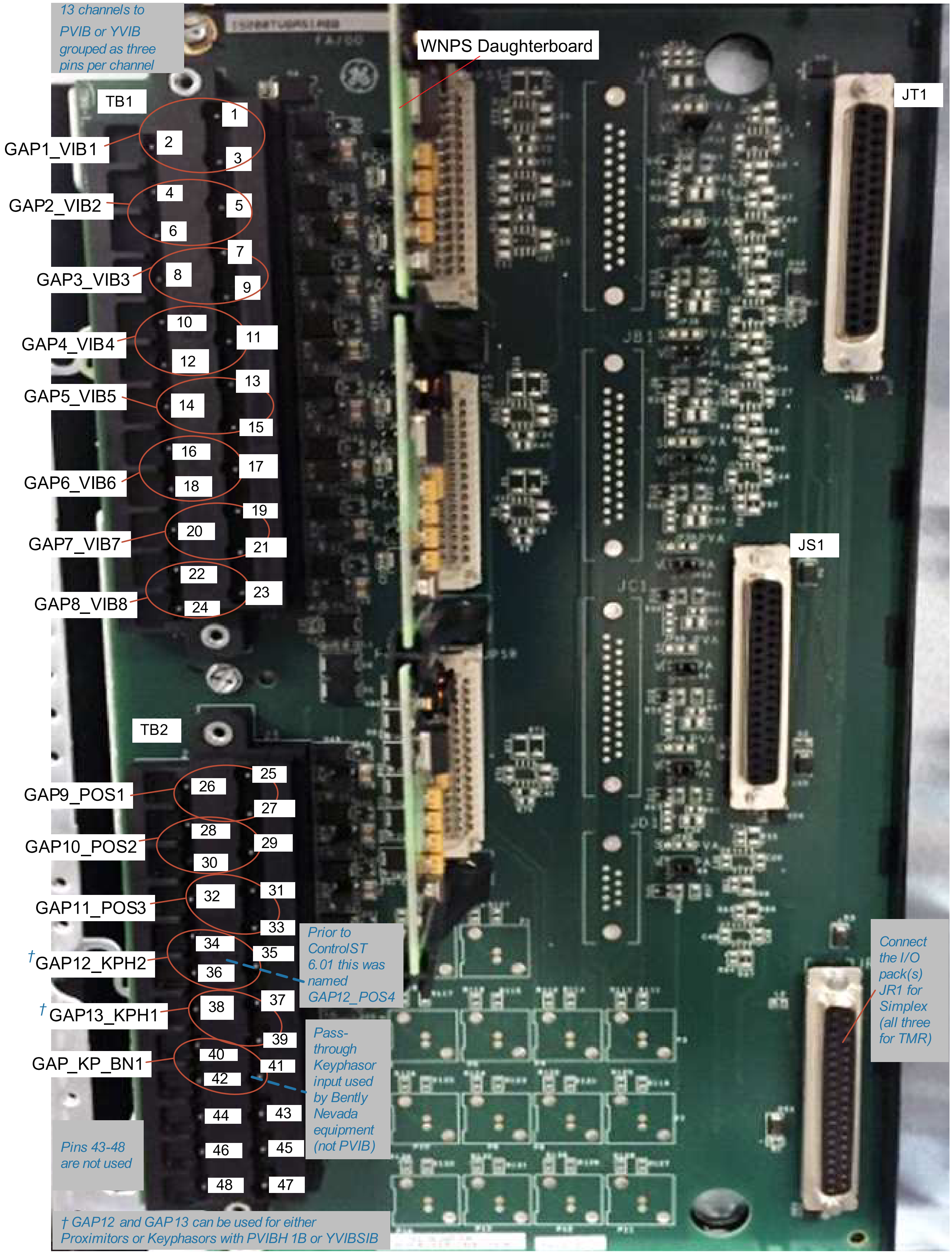
The Vibration Input (TVBA) terminal board acts as a signal interface board for the Mark VIe PVIB or Mark VIeS YVIB I/O packs. The TVBA provides a direct vibration interface to Eddy-current (position & velocity), seismic (velocity), Velomitors (velocity) and accelerometers with integrated outputs (velocity) sensors. The TVBA also provides a dynamic pressure interface to charge amplifiers.

The terminal board input signals entering through the two 24-point screw terminals are protected against high voltages due to electrical disturbances via transient suppression. Powering the different sensors and detecting open circuits is accomplished by jumpers JPxA located to the left of the 37-pin I/O pack connectors and JPxC located to the right of the 24-point screw terminals.

The input signals are passed on to the I/O packs through 37-pin connectors located on the right side of the TVBA. The TVBA can be used for either simplex or TMR applications. TMR applications fan the signal to three I/O packs.

Buffered outputs of the input signals are provided to 9 and 25 pin DIN connectors to feed the Bently Nevada***** 3xxx monitoring system. A bayonet nut connection (BNC) connection for each buffered output is also included to feed third party monitoring equipment. To configure the output buffers for the proper sensor, use the JPxB jumpers that are located to the left of the 37-pin I/O pack connectors. The I/O pack inputs channels 1 through 13 and channels 1 through 14 are routed to buffered outputs for external use. These BNC and DIN connectors, and the jumper are only available on TVBAH2A, TVBAH2B, TVBAS2A, and TVBAS2B.

Power is obtained from customer supplied +28 V through the I/O pack. The -28 V power needed to supply the Bently Nevada sensors is from the WNPS daughter board for the TVBAH#A terminal boards only, one used for simplex and three used for TMR configurations. The removable daughterboard(s) convert the sourced +28 V power to -28 V power.



13 channels to PVIB or YVIB grouped as three pins per channel

Prior to ControlST 6.01 this was named GAP12_POS4

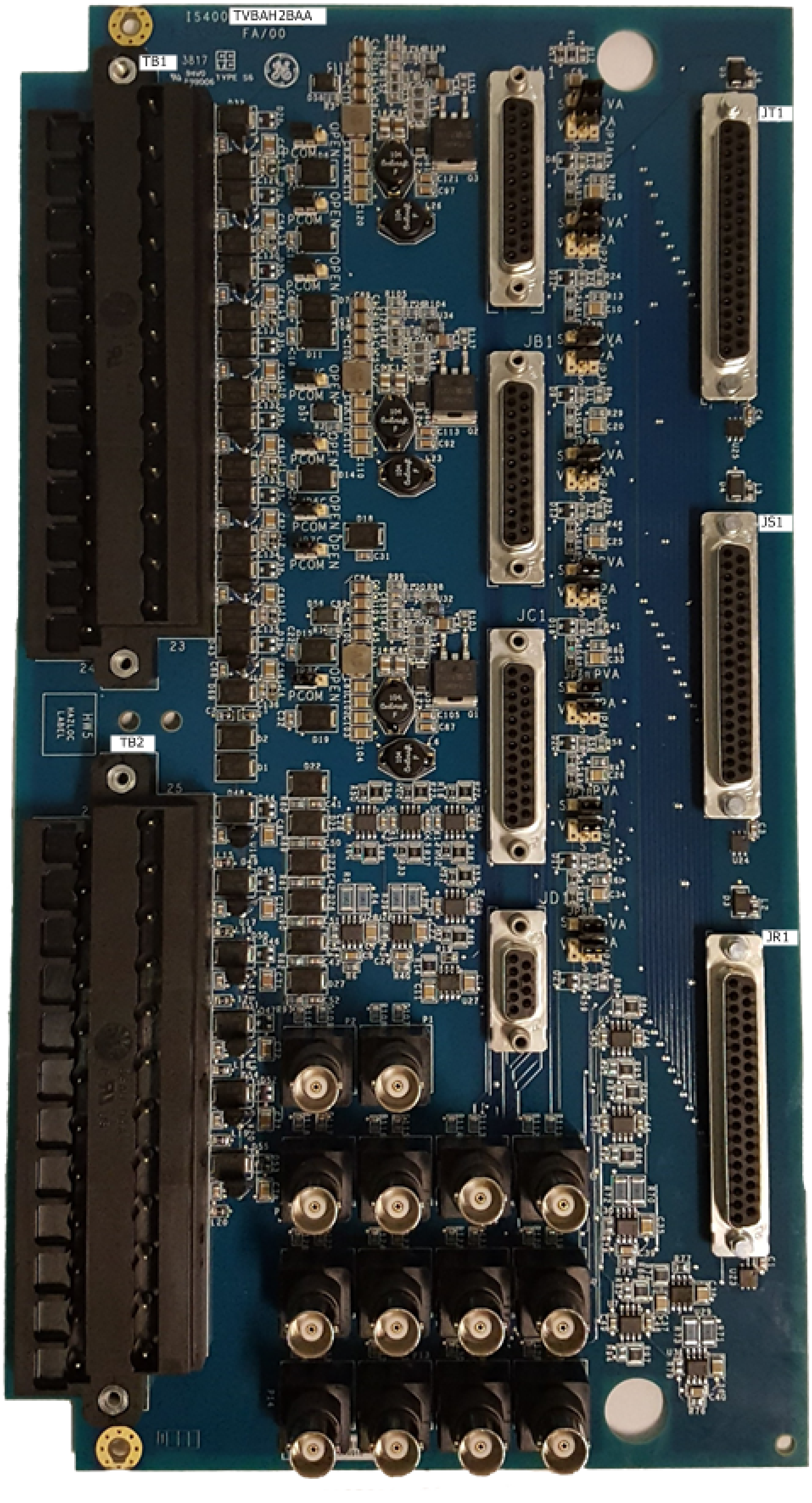
Pass-through Keyphasor input used by Bently Nevada equipment (not PVIB)

Connect the I/O pack(s) JR1 for Simplex (all three for TMR)

Pins 43-48 are not used

† GAP12 and GAP13 can be used for either Proximitors or Keyphasors with PVIBH1B or YVIBSIB

TVBAH1A Terminal Board



TVBAH2B Terminal Board

16.6.1 TVBA Compatibility and Attributes

The I/O pack and the negative power supply daughterboard (WNPS) work with the TVBA terminal boards to provide all sensor input checks. The following terminal board revisions work with the I/O pack.

Terminal Board	Compatibility	Buffered Output Circuits, DIN, and BNC Connectors	WNPS Connectors	IEC61508 Safety Certified	Allows Mixing of I/O Pack Revisions†
TVBAH1A	PVIBH1A and PVIBH1B	No	Yes	No	Yes
TVBAH2A	PVIBH1A and PVIBH1B	Yes	Yes	No	Yes
TVBAH1B‡	PVIBH1A and PVIBH1B	No	No	No	Yes
TVBAH2B‡	PVIBH1A and PVIBH1B	Yes	No	No	Yes
TVBAS1A	YVIBS1A and YVIBS1B	No	Yes	Yes	No
TVBAS2A	YVIBS1A and YVIBS1B	Yes	Yes	Yes	No
TVBAS2B‡	YVIBS1A and YVIBS1B	Yes	No	Yes	No

†Mixing I/O pack revisions on a TMR module does not allow for Enhanced mode of operation.

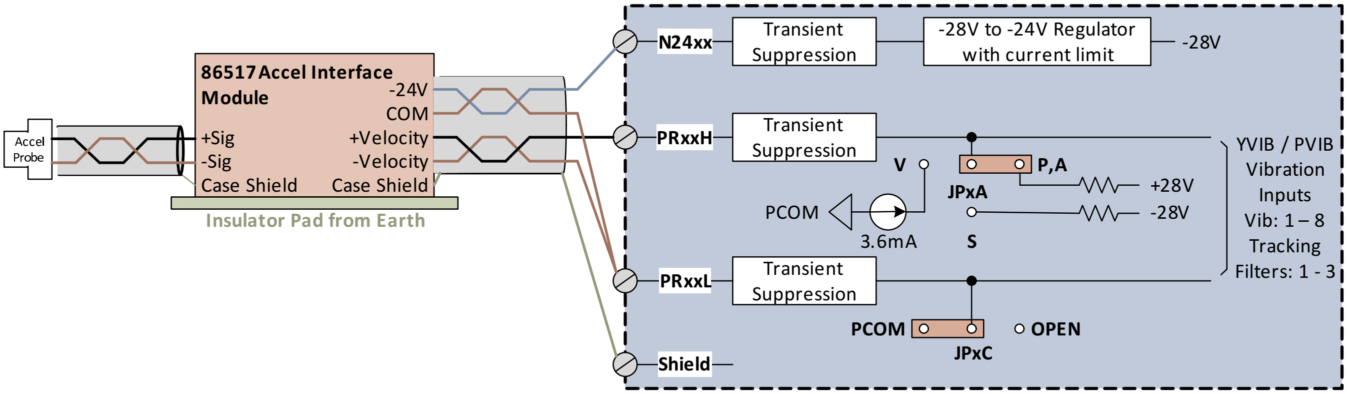
‡N28 power is generated internally to TVBAH#B and TVBAS2B.

16.6.2 TVBA Installation, Operation, and Jumper Configuration

The TVBA accepts 14 sensor inputs that are wired directly to two 24-point I/O terminal blocks. Each block is held down with two screws accepting up to #12 AWG wires. A shield termination attachment point is located adjacent to each terminal block. The I/O pack can only process 13 of the 14 channels. The 14th channel is forwarded to the buffered output stage for use by the Bently Nevada equipment (with TVBAH2A, H2B, S2A, or S2B).

16.6.2.1 Accelerometers with Integrated Outputs

The TVBA supports accelerometers with integrated outputs on channels 1, 2 and 3 only when the Tracking filters are required. If broadband rms vibration is all that is required, then all eight channels are available to use. For example, Oil & Gas LM1600, LM2500 or LM6000 gas turbine applications use the Bently Nevada 86517 sensor. The 86517 is powered by -24 V and the velocity output is connected to the vibration inputs: PRxxH and PRxxL. Tie the shield on the Mark VIe end and leave the shield open on the sensor side preventing ground loops.

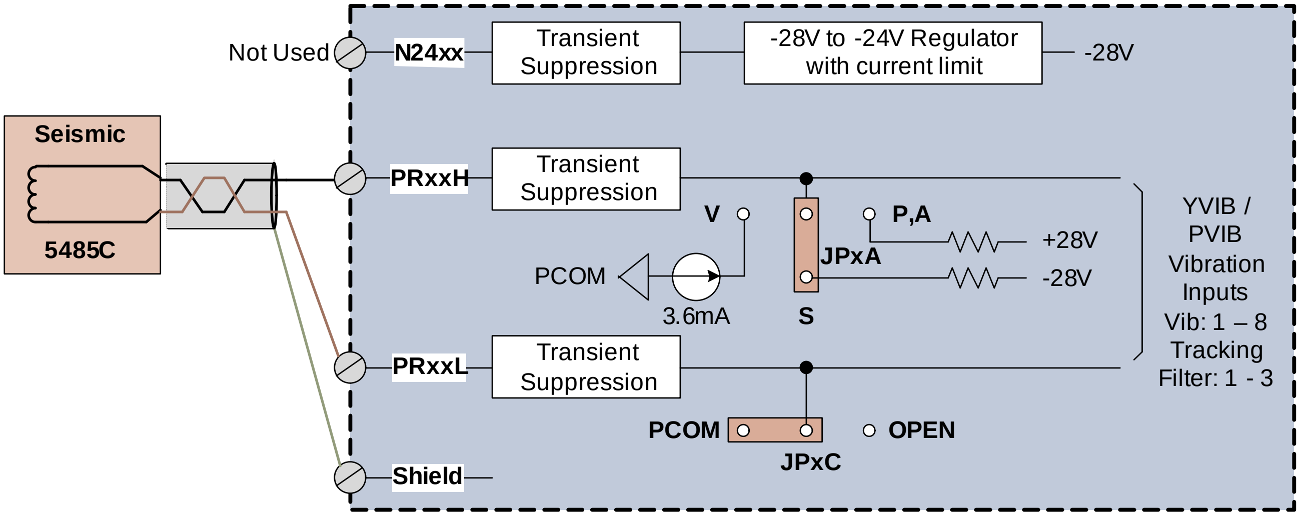


The IO variable name, VIBx

JPxA jumper is in the “P,A” position providing a +28 V weak pull-up for sensor failure detection and the JPxC jumper is in the “PCOM” position to provide a closed circuit for the -28 V power applied to the sensor through the WNPS -28 V daughterboard for TVBAH#A or TVBAS#A terminal boards only. JPxB is set in the 'PVA' position (for H2A, H2B / S2A, S2B boards).

16.6.2.2 Seismic Sensors

The TVBA can input a maximum of eight seismic sensor inputs on channels 1 through 8. Seismic sensors are usually moving-coil type probes that require no power. The heavy-duty gas turbines (HDGTs) use the Metrix 5235B, 5475C or 5485C sensors on the bearing housings to measure the non-rotating vibration. The Metrix 5485C or similar sensor's output is connected directly to the PRxxH and PRxxL inputs. The seismic output is centered at 0 V dc. With a sensitivity range of 100 to 200 mV/in/sec. Tie the shield on the Mark VIe end and leave the shield open on the sensor side.

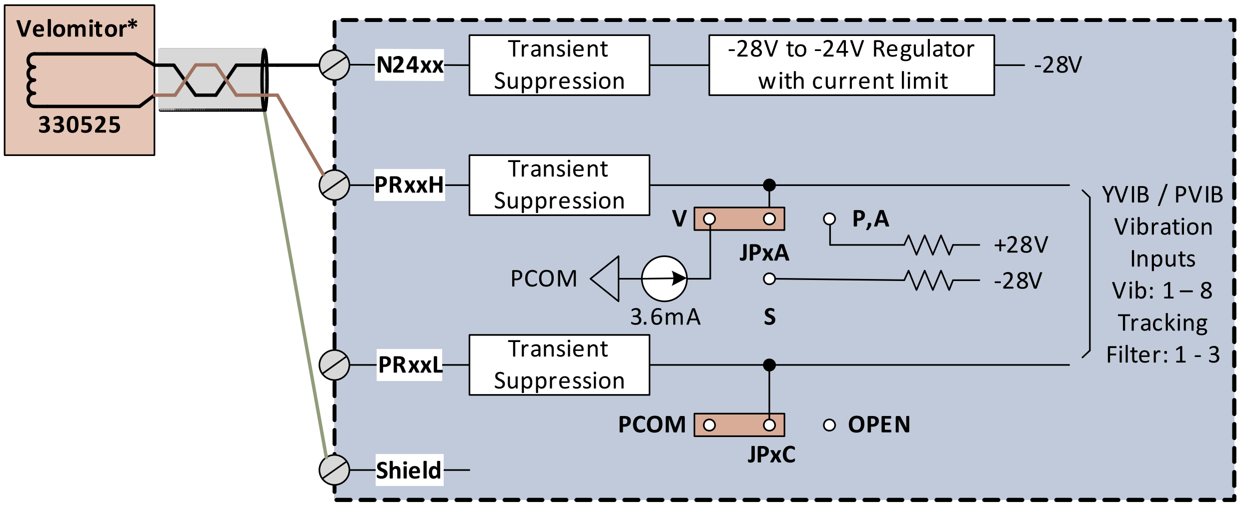


JPxA jumper is in the 'S' position providing a -28 V weak pull-down for sensor failure detection and the JPxC jumper is in the 'PCOM' position to allow the corresponding buffered output to be scaled the same as the signal input.

JPxB is set in the 'S' position (for H2A, H2B / S2A, S2B boards).

16.6.2.3 Velomitor Sensors

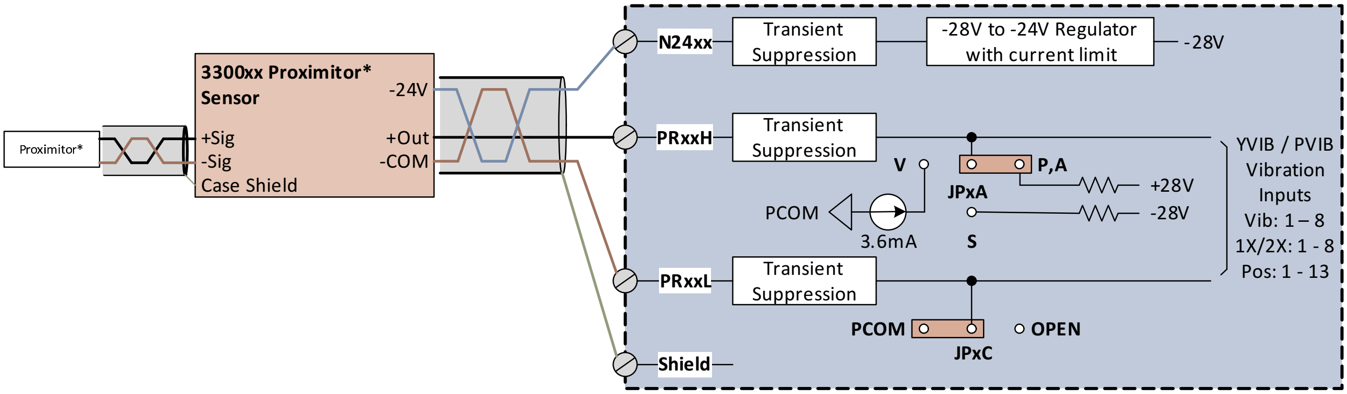
The TVBA accepts a maximum of eight Velomitor sensors on channels 1 through 8. The Bently Nevada 190501 and 3305xx product line are a constant-current device requiring a -24 V power sourced from the WNPS power supply daughterboard(s) for TVBAH#A and TVBAS#A terminal boards only to drive the current. The two-wire termination of this sensor uses the N24xx and PRxxH screw points. The velocity or AC content of the Velomitor is riding on top of a negative DC bias in the -8 to -12 V dc range generated by the sensor. The shield is tied to chassis at the control end and left open on the sensor side to prevent circulating ground currents. The sensor device usually has a sensitivity of 100 mV/in/sec.



JPxA jumper is in the 'V' position providing a 3.6 mA current diode driven by a -24 V source, N24xx. The JPxC jumper is in the 'PCOM' position providing a return for the -24 V power source. JPxB is set in the 'PVA' position (for H2A, H2B / S2A, S2B boards).

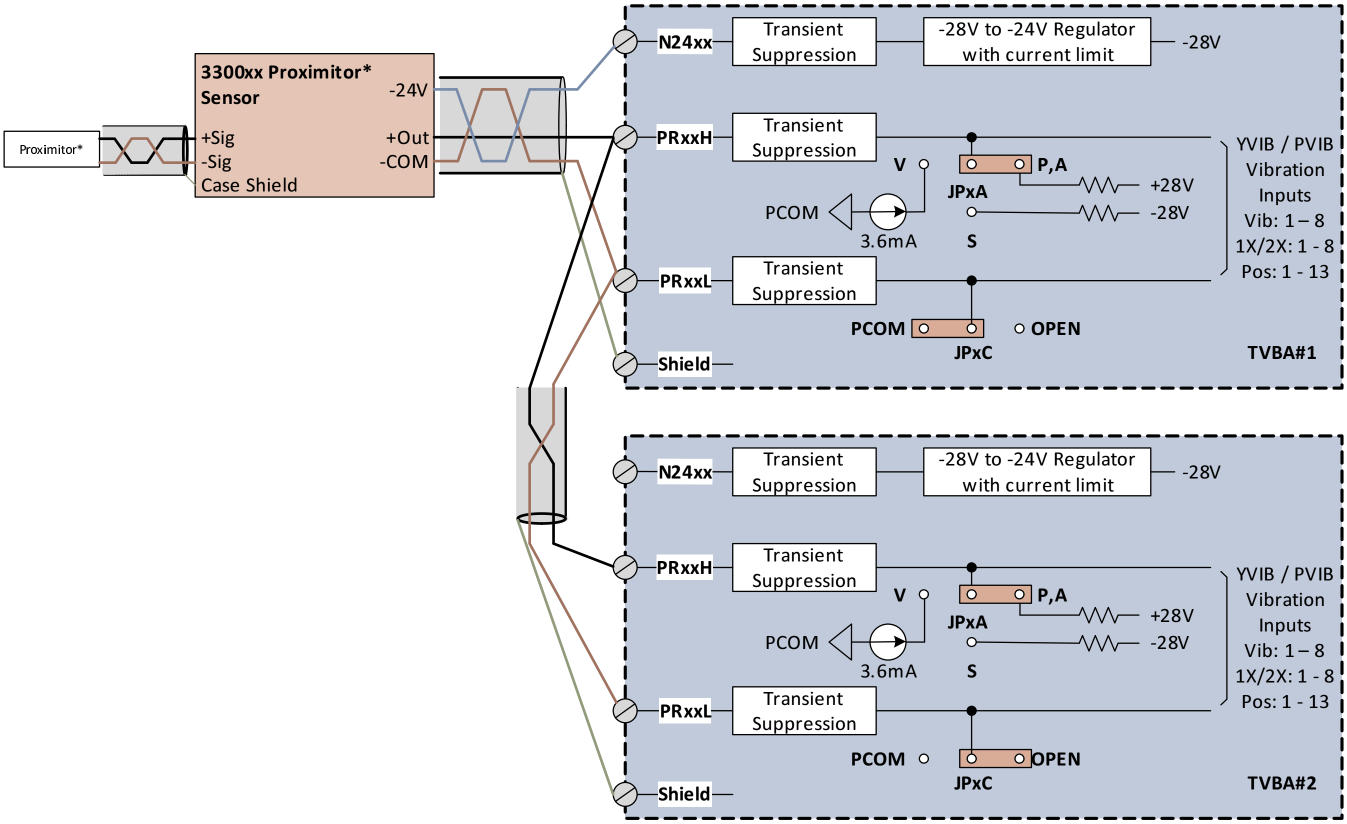
16.6.2.4 Eddy-current or Proximitor Sensors for Position and Velocity

The TVBA provides a maximum of 13 channels to connect an Eddy-current sensor to the terminal blocks. Channels 1 through 8 can condition both position and velocity information from the sensor and channels 9 through 13 can input only position information between the terminal screws PRxxH and PRxxL. The Bently Nevada Proximitor 3300 family and Metrix Model 5533 are -24 V powered devices with the output signal proportional to the gap between the rotating shaft and the head of the probe. Velocity information is extracted from the AC content riding on top of the DC gap signal. The shield is tied to chassis at the control end and left open on the sensor end to prevent circulating ground currents.



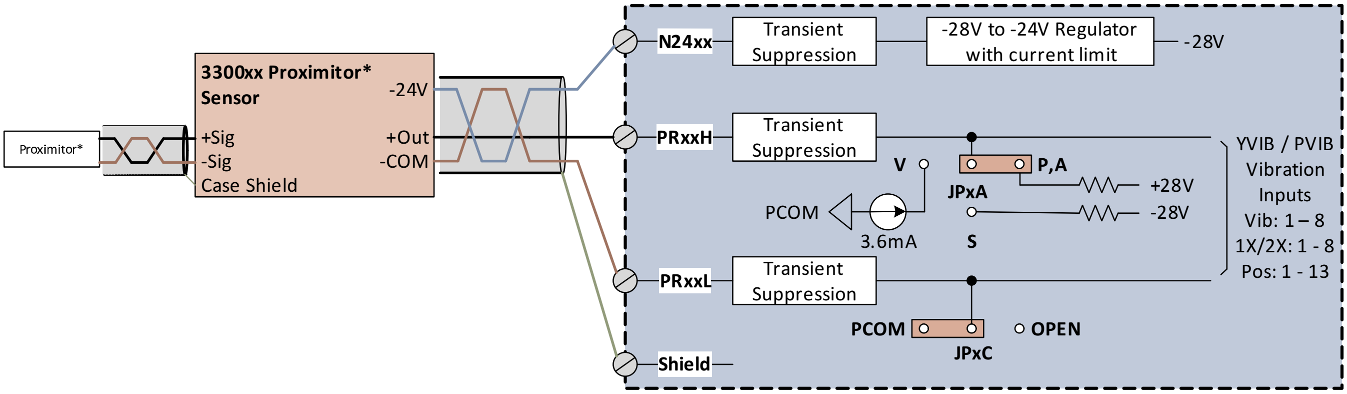
JPxA jumper is in the 'P,A' position providing a +28 V weak pull-up for sensor failure detection and the JPxC jumper is in the 'PCOM' position to provide a return for the -24 V power supply sourced from the -28 V WNPS daughter-boards on the TVBAH#A and TVBAS#A terminal boards only, and a low-side for the signal output of the sensor. JPxB is set in the 'PVA' position (for H2A, H2B / S2A, S2B boards).

The user can parallel the eddy-current signal to a second TVBA, but the N24xx power output would not be used from the second TVBA and JPxC would be in the "OPEN" position.



16.6.2.5 Eddy-current or Proximitor Sensors for Keyphasor

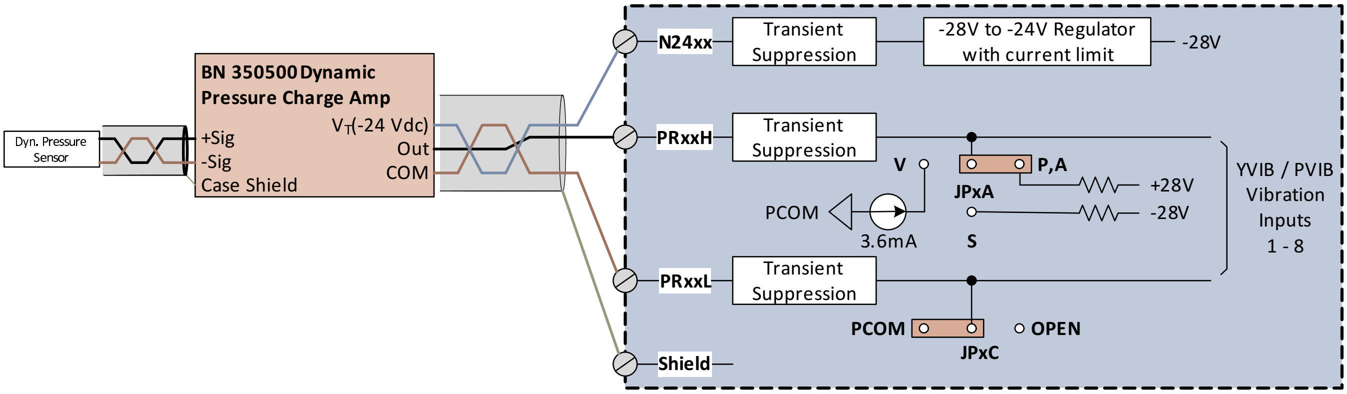
The TVBA provides channels 12 and 13 to connect an Eddy-current or Proximitor sensor used for a Keyphasor function. The Bently Nevada Proximitor 3300 family or Metrix Model 5533 are -24 V powered devices with the output signal proportional to the gap between the rotating shaft and the head of the probe. Velocity information is extracted from the AC content riding on top of the DC gap signal. The shield is tied to chassis at the control end and left open on the sensor end to prevent circulating ground currents.



JPxA jumper is in the ‘P,A’ position providing a +28 V weak pull-up for sensor failure detection and the JPxC jumper is in the ‘PCOM’ position to provide a return for the -24 V power supply sourced from the -28 V WNPS daughter-boards for the TVBAH#A and TVBAS#A terminal boards only, and a low-side for the signal output of the sensor. JPxB is set in the 'PVA' position (for H2A, H2B / S2A, S2B boards).

16.6.2.6 Bently Nevada 350500 Charge Amplifier

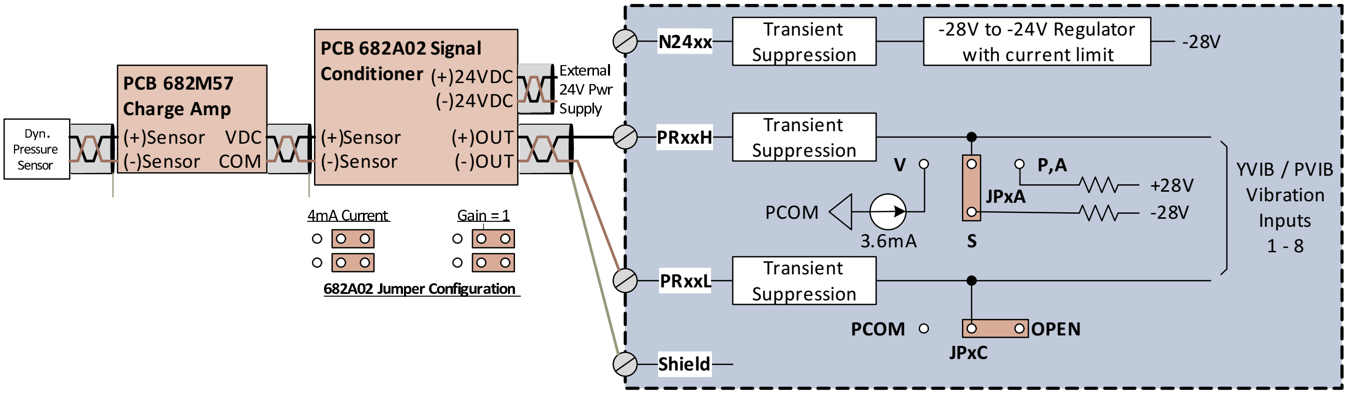
The TVBA vibration terminal board also supports the Bently Nevada 350500 charge amplifier used with dynamic-pressure sensors examining the combustion dynamics of the LM2500 DLE gas turbines. The TVBA can input combustion dynamics information on channels 1 through 8 where the I/O pack can provide band-passed, root-mean-squared (r.m.s.) dynamic-pressure data for the LM2500 DLE combustion. The charge amplifier is powered with -24 V and the AC dynamics output is riding on top of a negative DC bias signal that is used by the I/O module for signal health. The shield is tied to chassis at the control end and left open on the sensor end to prevent circulating ground currents.



JPxA jumper is in the ‘P,A’ position providing a +28 V weak pull-up. The JPxC jumper is in the ‘PCOM’ position to provide a return for the -24 V power supply sourced from the -28 V WNPS daughter-boards on the TVBAH#A and TVBAS#A terminal boards only, and a low-side for the signal output of the charge amplifier. JPxB is set in the 'PVA' position (for H2A, H2B / S2A, S2B boards).

16.6.2.7 PCB Piezotronics 682A02 Signal Conditioner

The PCB 682A02 signal conditioner can be connected to the TVBA terminal board for channels 1 through 8. The PCB system which is used with the Mark VIe PAMC combustion dynamics monitoring I/O is powered with +24 V instead of -24 V as applied to the Bently Nevada systems. The 682A02 signal conditioner is powered externally by a +24 V source. The 682A02 converts the 24 V power to a 4mA constant-current source to power the PCB 682M57 charge amplifier. The 682A02 ‘Out’ connects to the TVBA PRxxH/L terminal block screws. The AC dynamic pressure signal is riding on top of a 10 – 13 V dc bias voltage used to determine the health of the combustion sensing system. The shield is tied to chassis at the control end and left open on the sensor end to prevent circulating ground currents.



JPxA jumper is in the ‘S’ position providing a -28 V weak pull-down. The JPxC jumper is in the ‘OPEN’ position to provide a true differential input eliminating ground current loops with the external power supply. JPxB is set in the 'S' position (for H2A, H2B / S2A, S2B boards).

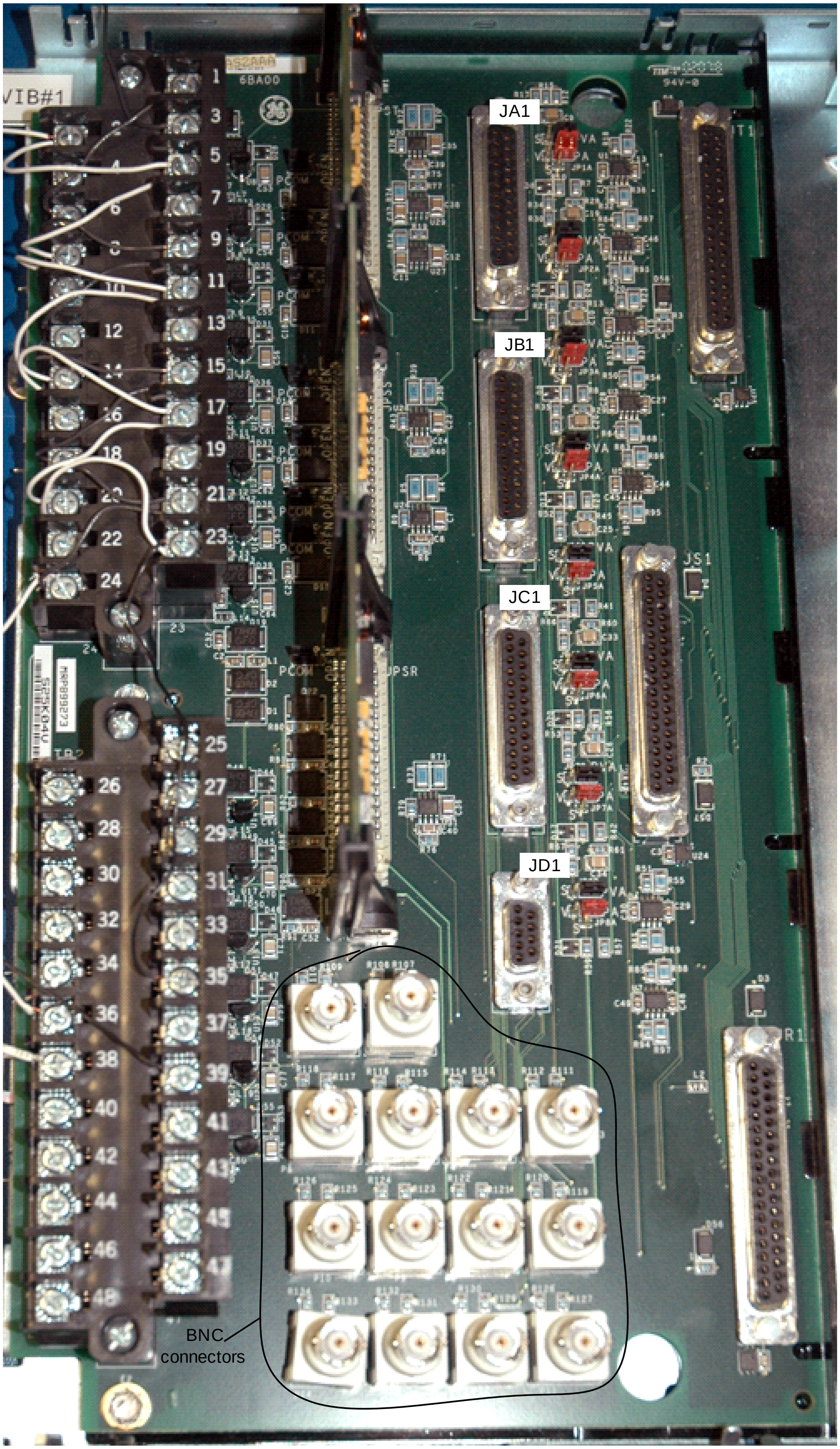
16.6.2.8 Customer Terminal Points

Channel	Signal Name	Pin #	Description
GAP1_VIB1	N24V01	1	-24 V power supply output for channel #1
	PR01H	2	Input #1 signal high side to I/O pack and buffered output
	PR01L	3	Input #1 signal low side to I/O pack and buffered output
GAP2_VIB2	N24V02	4	-24 V power supply output for channel #2
	PR02H	5	Input #2 signal high side to I/O pack and buffered output
	PR03L	6	Input #2 signal low side to I/O pack and buffered output
GAP3_VIB3	N24V03	7	-24 V power supply output for channel #3
	PR03H	8	Input #3 signal high side to I/O pack and buffered output
	PR03L	9	Input #3 signal low side to I/O pack and buffered output
GAP4_VIB4	N24V04	10	-24 V power supply output for channel #4
	PR04H	11	Input #4 signal high side to I/O pack and buffered output
	PR04L	12	Input #4 signal low side to I/O pack and buffered output
GAP5_VIB5	N24V05	13	-24 V power supply output for channel #5
	PR05H	14	Input #5 signal high side to I/O pack and buffered output
	PR05L	15	Input #5 signal low side to I/O pack and buffered output
GAP6_VIB6	N24V06	16	-24 V power supply output for channel #6
	PR06H	17	Input #6 signal high side to I/O pack and buffered output
	PR06L	18	Input #6 signal low side to I/O pack and buffered output
GAP7_VIB7	N24V07	19	-24 V power supply output for channel #7
	PR07H	20	Input #7 signal high side to I/O pack and buffered output
	PR07L	21	Input #7 signal low side to I/O pack and buffered output
GAP8_VIB8	N24V08	22	-24 V power supply output for channel #8
	PR08H	23	Input #8 signal high side to I/O pack and buffered output
	PR08L	24	Input #8 signal low side to I/O pack and buffered output
GAP9_POS1	N24V09	25	-24 V power supply output for channel #9
	PR09H	26	Input #9 signal high side to I/O pack and buffered output
	PR09L	27	Input #9 signal low side to I/O pack and buffered output
GAP10_POS2	N24V10	28	-24 V power supply output for channel #10
	PR10H	29	Input #10 signal high side to I/O pack and buffered output
	PR10L	30	Input #10 signal low side to I/O pack and buffered output
GAP11_POS3	N24V11	31	-24 V power supply output for channel #11
	PR11H	32	Input #11 signal high side to I/O pack and buffered output
	PR11L	33	Input #11 signal low side to I/O pack and buffered output
GAP12_KPH2	N24V12	34	-24 V power supply output for channel #12
	PR12H	35	Input #12 signal high side to I/O pack and buffered output
	PR12L	36	Input #12 signal low side to I/O pack and buffered output
GAP13_KPH1	N24V13	37	-24 V power supply output for channel #13
	PR13H	38	Input #13 signal high side to I/O pack and buffered output
	PR13L	39	Input #13 signal low side to I/O pack and buffered output
GAP_KP_BN1	N24V14	40	-24 V power supply output for channel #14
	PR14H	41	Input #14 signal high side to buffered output ONLY
	PR14L	42	Input #14 signal low side to buffered output ONLY
		43 - 48	No connections

16.6.2.9 TVBAH2A or S2A Buffered Outputs

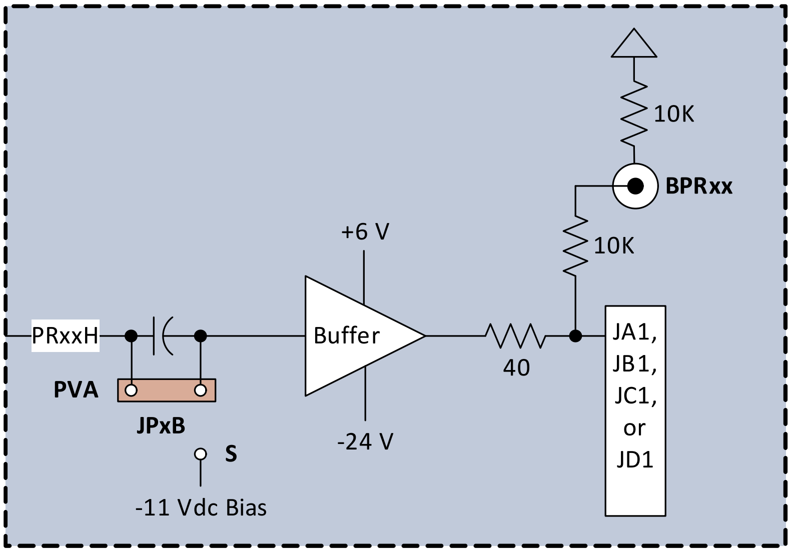
With the TVBAH2A or S2A, each channel provides additional outputs other than the standard 37-pin connection. The signal output is buffered from the signal used by the I/O module to prevent any corruption caused by third-party hardware connected to the output.

Each channel is output on a BNC connector with 10 kilo-ohms between the buffer out and BNC signal pin and 10 kilo-ohms isolation between signal low and the Mark VIe control power common, PCOM.



TVBA_2A Terminal Board

Each channel is also output through a 25-pin or 9-pin connectors JA1, JB1, JC1 and JD1 designed to interface with the Bently Nevada 3500 monitoring system. The TVBA buffered source impedance is approximately 40 ohms.



Jumper, JPxB

The jumper, JPxB where x = 1 through 14 is used to configure the output for either seismic outputs with a -11 V dc bias voltage added to the velocity signal or positioned to output Proximitor, Velomitor or accelerometer with integrated output signals.

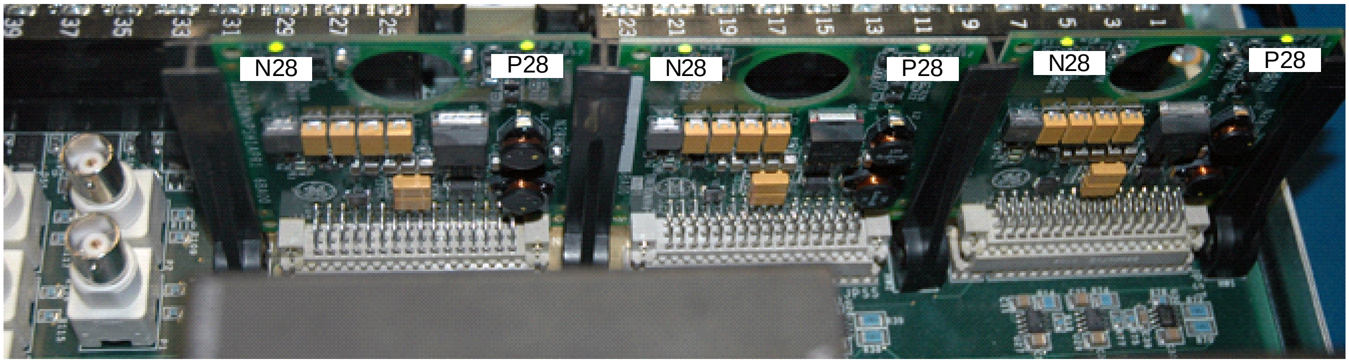
16.6.2.10 Bently Nevada Buffered DB Connector Points

Signal Name	Connector	Pin #
BPR01	JA1	3
PCOM	JA1	2
BPR02	JA1	7
PCOM	JA1	6
BPR03	JA1	11
PCOM	JA1	10
BPR04	JA1	23
PCOM	JA1	24
BPR05	JB1	3
PCOM	JB1	2
BPR06	JB1	7
PCOM	JB1	6
BPR07	JB1	11
PCOM	JB1	10
BPR08	JB1	23
PCOM	JB1	24
BPR09	JC1	3
PCOM	JC1	2
BPR10	JC1	7
PCOM	JC1	6
BPR11	JC1	11
PCOM	JC1	10
BPR12	JC1	23
PCOM	JC1	24
BPR13	JD1	1
PCOM	JD1	3

Signal Name	Connector	Pin #
BPR14	JD1	5
PCOM	JD1	9

16.6.2.11 WNPS Power Supply Daughterboard

Three redundant external power supplies provide the power for the TVBAH#A and TVBAS#A only. The WNPS function is integrated into the TVBAH#B and TVBAS2B terminal boards. If one power supply goes down, the offline power supply can be replaced without bringing down the terminal board and sensor power. To maintain this feature, the TVBA has three removable daughterboards to provide the +28 Vdc to -28 V dc power conversion. The daughterboards can be removed while the TVBA is online by disconnecting the I/O pack power (R, S or T), and removing the WNPS. Indicator LEDs display the status of the P28 power in and the N28 power out.



The WNPS uses the corresponding channel (R, S, or T) 28 V bus to manufacture the required power for the vibration probes and on any board chips requiring power. A monitor feed for each -28 V supply should be fed back to the I/O pack for monitoring. The TVBA combines three -28 sources using diodes from the daughterboards to create the TVBA N28 bus. A TVBA configured with the TMR daughterboards provide enough current to supply 14 Proximitors at 18 mA, 14 buffered outputs at 12 mA, with one channel shorted at approximately 200 mA for a total of 540 mA without failure. Current sharing by the supplies make this condition possible. A TVBA with a single WNPS is not expected to handle this condition.

16.6.3 TVBA Specifications

Requirement	Limits
Input Options	
Number of channels supporting position or gap inputs	13
Number of channels supporting velocity or dynamic pressure sensor inputs	8
Number of channels supporting Key Phasor inputs	2
Sensors Supported	1) Eddy-current or Proximitor
	2) Accelerometer with integrated output
	3) Seismic
	4) Velomitor
	5) Charge Amplifier
Sensor Power Options	
Number of negative 24 V dc, N24 outputs to power sensors	14
N24 Nominal Voltage	-24.5 V dc
	(-23 to -26) V dc
N24 maximum current	12 mA
Buffered Outputs	
Number of buffered outputs	14
Buffer Gain Accuracy	+/-0.1%
DB9 and DB25 Connector Output Load requirements to achieve less than 10% overshoot	1500 ohms minimum
	1000 pF maximum
BNC Connector Load requirements to achieve less than 10% overshoot	2 Mohm minimum
	1000 pF maximum
WNPS Negative Power Supply Daughter Board	
Number of WNPS boards used on TVBA to providing N24 power from redundant P28 power sources R, S & T.	3
Nominal Output Voltage	-28 V dc
	(-26.6 to -29.4) V dc
Output Voltage Ripple	280 mV pk
Maximum Output Current	400 mA
Terminal Screws	
Wiring Sizes	22 to 12 AWG
Torque	9.6 in-lb (1.085 N-m)

16.6.4 Diagnostics

The TVBA terminal board provides weak pull-up and pull-down circuits configured based on the jumper position to allow the Vibration I/O Pack (PVIB or YVIB) to detect an open circuit. The I/O pack creates the diagnostic alarm (fault) if any one of the inputs has an out-of-range voltage.

Each connector between the TVBA and the I/O pack has its own ID device that is interrogated by the Vibration pack. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the R, S and T connector location. When this chip is read by the I/O pack and a mismatch is encountered, a hardware incompatibility fault is created.

Notes

17 PUAA, YUAA Universal I/O Modules

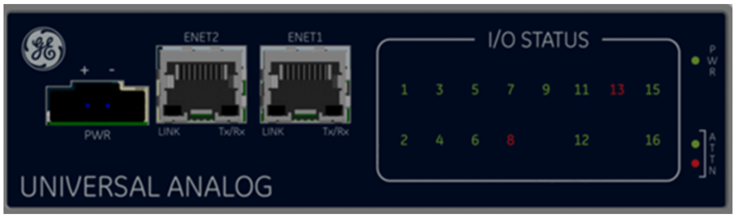
The Mark* VIe and Mark VIeS control systems are used in a wide range of process control and turbo-machinery applications. The PUAA and YUAA modules are enhanced I/O devices designed for distributed control systems (DCS) and balance of plant (BoP) control systems (where there are typically up to tens of thousands of I/O points, requiring high availability). These modules offer a reduction of cost per I/O point as compared to traditional analog I/O modules (while maintaining high availability). A three-wire channel is located on a single terminal block section that fits onto a row of the header. Each block section can be independently wired and then inserted, allowing channel by channel commissioning. This enables much faster and more reliable terminations and decreases time to commission / maintain the system. The PUAA module is the standard Mark VIe compatible module, while the YUAA module is the companion module that is used in the Mark VIeS Safety control system. The PUAA and YUAA modules share identical functionality.

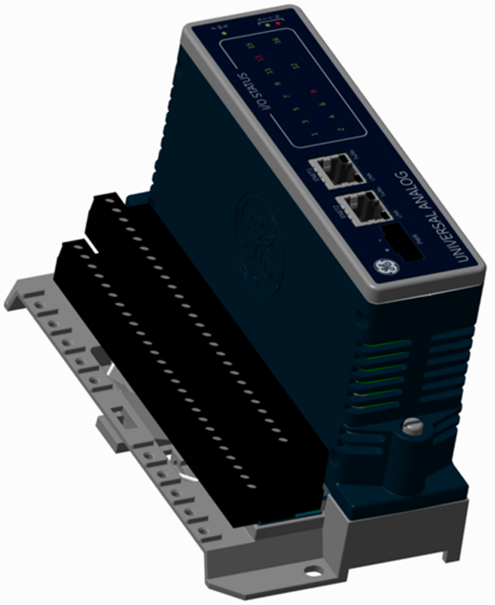
Support for Universal I/O Modules in ControlST*

Product	ControlST Version
PUAA	V07.00.00C or later
YUAA	V07.02.00C or later

17.1 Mark VIe PUAA Universal I/O Pack

The PUAA module consists of the PUAAH1A I/O pack connected to the SUAAH1A terminal board. The initial release of the module meets a variety of international regulations and standards, as detailed in GEH-6721_Vol_I system manual, including RoHs components.





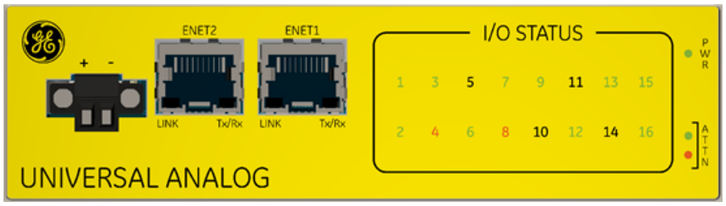
Sixteen Simplex analog channels can be configured individually as any of the following types: Thermocouple, RTD, Voltage Input (± 5 V or ± 10 V), 4–20 mA current input, 0–20 mA current output, pulse accumulator, or digital input. Configuration of I/O channels is accomplished with the ToolboxST* application.

The boards internal to the I/O pack include one BPPC processor, one BCAR carrier board, and four MIO-universal analog I/O boards. The BPPC processor is common to many Mark VIe I/O packs. The SUAA terminal board provides removable terminal blocks to reduce maintenance down times. The PUAA module operates on simplex control side power as supplied by a 28 V source. There are no internal jumpers, switches, or fuses required to configure the module.

The PUAA continues to meet the same high level of reliability/availability standards as other Mark VIe control system products. Savings to the customer include fewer panels/footprint and variations for replacement parts.

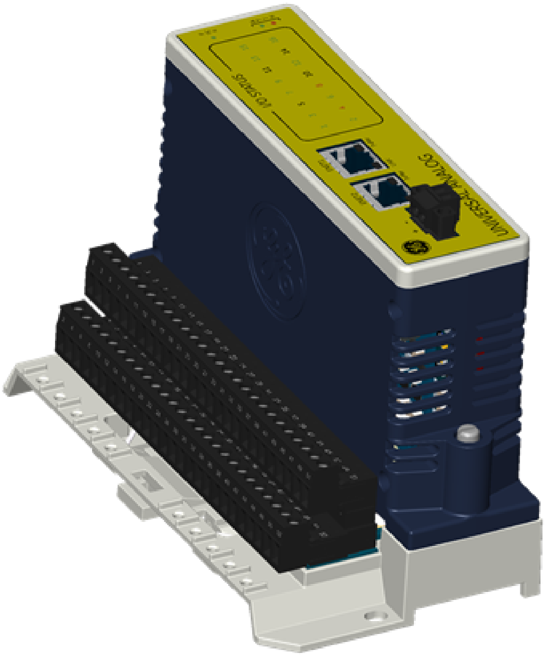
Note The operating voltage limits on the user terminals are -12 to 20 V with respect to power COM for analog modes. The digital input mode has an operating limit of 0 to 20 V for inputs with no series resistance and up to 30 V for inputs with line monitoring resistors added. Operation outside of these limits may impact operation of adjacent channels.

17.2 Mark VIeS YUAA Universal I/O Pack



The YUAA module consists of the YUAAS1A I/O pack connected to the SUAAS1A terminal board. The initial release of the module meets a variety of international regulations and standards, as detailed in GEH-6721_Vol_I system manual, including RoHs components.

Sixteen Simplex analog channels can be configured individually as any of the following types: Thermocouple, RTD, Voltage Input (± 5 V or ± 10 V), 4–20 mA current input, 0–20 mA current output, pulse accumulator, or digital input. Configuration of I/O channels is accomplished with the ToolboxST* application.



The boards internal to the I/O pack include one BPPC processor, one BCAR carrier board, and four MIO-universal analog I/O boards. The BPPC processor is common to many Mark VIeS I/O packs. The SUAA terminal board provides removable terminal blocks to reduce maintenance down times. The YUAA module operates on simplex control side power as supplied by a 28 V source. There are no internal jumpers, switches, or fuses required to configure the module.

The YUAA continues to meet the same high level of reliability/availability standards as other Mark VIe control system products. Savings to the customer include fewer panels/footprint and variations for replacement parts.

Note The operating voltage limits on the user terminals are -12 to 20 V with respect to power COM for analog modes. The digital input mode has an operating limit of 0 to 20 V for inputs with no series resistance and up to 30 V for inputs with line monitoring resistors added. Operation outside of these limits may impact operation of adjacent channels.

17.3 Specifications

17.3.1 PUAA Specifications

PUAA Specifications

Item	Specification
Number of Channels	16 channels, with groups of three terminals per channel
Supported Redundancy	Simplex
Shared IONet	Supported
Required ControlST and PUAA Versions	ControlST Software Suite V07.00.00C or later PUAA firmware V05.03.00 or later
Auto-Reconfiguration	Supported
RJ-45 Ethernet Ports	Supports dual Ethernet (IONet) networks
Fastest Frame Rate Supported	10 ms
Supported I/O Types	• Thermocouple • RTD • 4–20 mA current input with HART option • ± 5 V or ± 10 V input • 0–20 mA current output with HART option • Digital inputs and outputs • Pulse accumulators
Incoming Control Power	28 V dc source is required
Incoming Power Consumption	Power consumption is based on 8.1 watts quiescent plus power per channel modes as follows: • TC, 5V, 10V, externally wetted discrete inputs, pulse accumulator inputs, or RTD modes = 0.02 watts per channel • External fed mA input and internally wetted discrete inputs = 0.04 watts per channel • Internal fed mA input or mA output = 0.68 watts per channel or less, depending on external loop resistance
Power Output to Field Device	From SUAA screws PWR_RTN, supply is a maximum 2 V less than the incoming control power to the PUAA I/O pack.
I/O Pack Internal Current Limiter	2.5 A to limit impact to supply if a short circuit failure should occur
I/O Pack Hot Swap Replacement	Supported
28 V dc Power Connector	Phoenix® contact part number MC 1.5/S-STF-3.81
Rating for Ambient Temperature on of Module Exterior During Operation	-40 to 70 °C
Storage Temperature Rating	-40 to 85 °C
Relative Humidity Required	5% to 95% non-condensing
Lightning Strike Protection	UL61010-1
Operating Vibration	IEC/EN 60068-2-6
Flammability Rating	UL94V-2
I/O Pack Casing Protection Against Intrusion	Ingress Protection Code: IP20 per EN 60529
General Mark VIe I/O Pack Specifications	Refer to GEH-6721_Vol_I for technical regulations and standards that apply to all of the Mark VIe control system equipment
PUAA Module Dimensions	6.6 in L x 3.4 in W x 4.3 in H (with I/O pack attached) Average panel area/channel is equal to small S card footprint per group of 16 channels
Mode Miswired Tolerance	Refer to the ToolboxST Configuration Modes section for details regarding PUAA resistance to damage when incorrectly wired or configured.

PUAA Specifications (continued)

Item	Specification
Group Isolation	Exists internally between the processor and the IONet ports to break ground loops, using high resistance barriers
Channel Terminal Voltage	Operation is guaranteed only when channel terminals are connected to signal voltages between 20 to -11 volts with respect to COM. For voltages outside this range, an external resistor may be required for correct operation. Refer to the section *Digital Inputs and Outputs*. Signals above 24.5 or below -13 volts with respect to COM will affect performance across other channels and could cause long term degradation of the performance. Voltages beyond ± 28 V are clamped by transorbs for protection.

PUAA mA/HART Specifications

Item	Specification
Number of Channels	16 channels per terminal board possible as inputs or outputs
Input Span	4-20 mA dc with allowance for 0-24 mA to cover NAMUR fault conditions
Input Converter Resolution	16-bit analog-to-digital converter
HART Rx and Cx Values	250 ohms in parallel with 5000 pF for HART inputs 14 kohms with 11000 pF for HART current outputs
Scan Time	Normal scan 5 ms (200 Hz). Note that controller frame rate is 100 Hz.
Measurement Accuracy	Better than 0.1% full scale over the temperature range -40 to 70°C.
Noise Suppression on Inputs	A software filter, using a two-pole, low-pass filter, is configurable for: off (0), .75, 1.5 Hz, 3 Hz, 6 Hz, 12 Hz for mA and HART inputs
Common Mode Rejection	Ac common mode rejection 60 dB at 60 Hz, with up to ±5 V common mode voltage. Dc common mode rejection 80 dB with -5 to +7 peak V common mode voltage
Common Mode Voltage Range	±5 V
Output Converter	16-bit D/A converter with 0.5% accuracy over 0 to 24 mA possible span
Output Load	800 Ω for 0-20 mA output

PUAA Performance

Channel Configuration	Rating
mA/HART Inputs	4 to 20 mA at 0.1% accuracy over temperature range *In presence of severe conducted RF interference (IEC 61000-4-6, 10 V rms), the accuracy may degrade to 1.5%.* *In presence of severe radiated RF interference (IEC 61000-4-3, 10 V/m), internal wetted mA input accuracy may degrade to 2% and external wetted mA input accuracy may degrade to 20%.*
Voltage Inputs	± 5 V dc or ±10 V dc at 0.1% accuracy over temperature range
mA Outputs	0 to 20 mA with 0.5% accuracy, compliance up to 18 V dc with 22 V or higher field supply 0-800 ohm load with current monitoring as a variable OutxxMA with 3% accuracy *In the presence of severe radiated RF interference (IEC 61000-4-3, 10 V/m), the accuracy may degrade to 3%.*
Thermocouple Inputs	E, J, K, S, T, B, N, R thermocouples with 0.1 % measurement accuracy of full scale **Caution** **The CJC sensor accuracy varies with the amount of power dissipated in the PUAA package. For a setting of 16 thermocouples, the CJC provide 2 °F accuracy. For best accuracy with local CJC, mount the PUAA at the bottom of the cabinet far from higher power devices or PUAA using higher power modes. If combining thermocouples with high power modes such as mA outputs, the CJC may degrade in accuracy up to 4 °F. A practical limit on mixing modes is to limit up to 8 mA outputs on any PUAA with other channels set for thermocouples.** **For best accuracy it is recommended that remote cold junctions be used due to heat dissipation from analog outputs and input modes. The remote cold junction value may be from either RTD channels on the same PUAA with variables passed to application code or from other devices read by the application code such as another PUAA or PRTD.**
	RSS Accuracy of 53 uV on 45 mV span (E, J, K, S, T)
	RSS Accuracy of 115 uV on 95 mV span (B, N, R)
	Open wire detection is supported
	Wiring Resistance: round trip between channel terminals is less than 100 ohms for full accuracy
RTD Inputs	120 ohm Nickel ± 2°F at 400 °F 100 ohm Platinum ± 4°F at 400 °F 200 ohm Platinum ± 2°F at 400 °F 10 ohm Copper ± 10 °F at 400 °F Resistance up to 450 ohms Scan time: 500 ms *In the presence of severe conducted RF interference (IEC 61000-4-6, 10 V rms), the resistance accuracy may degrade to 2%. The associated temperature accuracy will similarly vary with the amount based on the type of sensor.*
Discrete Inputs	10 to 20 V external wetted switches into 12.5 Kohm internal load Sequence of Event (SOE) tagging per I/O frame for first, second, and last change with 1 msec resolution 22 to 30 V external wetted switches using a series or a series-parallel set of 8.2 Kohm resistors Line monitoring (open/short detection) is optional for external wetting using two 8.2 Kohm resistors at contact Line monitoring (open/short detection) is not supported on > 20 V external wetted switches Internal wetted switches with 10 mA contact current, 22 V open contact voltage Line monitoring (open/short detection) is optional for internal wetting using two 240 ohm resistors at contact

PUAA Performance (continued)

Channel Configuration	Rating
Discrete Outputs	Up to 24 mA at up to 22 V using mA output mode, capable of driving control circuits of many external interposing electromagnetic (Phoenix Contact 2961105 on DIN base PLC-BSP-24DC/21) or solid state (Crydom DC60S7 60Vdcc 7A) relays using under 22 mA control current with panel or DIN rail mounting near the SUAA base. SOE is not supported on analog outputs to drive external interposing circuits.
Pulse Accumulators	16-bit accumulator Voltage range: -10 to 20 V Frequency range: 0 to 500 Hz

PUAA Orderable Part Numbers

Part Numbers	Description
IS430SNUAH1A	Complete assembled Simplex module made up of one IS420PUAAH1A attached to one IS410SUAAH1A, and includes the base/mounting and hardware/cover
IS420PUAAH1A	PUAA I/O module with captive mounting screws
IS410SUAAH1A	Simplex terminal board on DIN-rail mountable base
IS400SUAAH1A	Simplex terminal board only

17.3.2 YUAA Specifications

YUAA Specifications

Item	Specification
Number of Channels	16 channels, with groups of three terminals per channel
Supported Redundancy	Simplex
Shared IONet	Supported
Required ControlST and YUAA Versions	ControlST Software Suite V07.02.00C or later YUAA firmware V05.05.00 or later
Auto-Reconfiguration	Supported
RJ-45 Ethernet Ports	Supports dual Ethernet (IONet) networks
Fastest Frame Rate Supported	10 ms
Supported I/O Types	• Thermocouple • RTD • 4–20 mA current input with HART option • ± 5 V or ± 10 V input • 0–20 mA current output with HART option • Digital inputs and outputs • Pulse accumulators
Incoming Control Power	28 V dc source is required
Incoming Power Consumption	Power consumption is based on 8.1 watts quiescent plus power per channel modes as follows: • TC, 5V, 10V, externally wetted discrete inputs, pulse accumulator inputs, or RTD modes = 0.02 watts per channel • External fed mA input and internally wetted discrete inputs = 0.04 watts per channel • Internal fed mA input or mA output = 0.68 watts per channel or less, depending on external loop resistance
Power Output to Field Device	From SUAA screws PWR_RTN, supply is a maximum 2 V less than the incoming control power to the YUAA I/O pack
I/O Pack Internal Current Limiter	2.5 A to limit impact to supply if a short circuit failure should occur
I/O Pack Hot Swap Replacement	Supported
28 V dc Power Connector	Phoenix® contact part number MC 1.5/S-STF-3.81
Rating for Ambient Temperature on Module Exterior During Operation	-40 to 70 °C
Storage Temperature Rating	-40 to 85 °C
Relative Humidity Required	5 to 95% non-condensing
Lightning Strike Protection	UL61010-1
Operating Vibration	IEC/EN 60068-2-6
Flammability Rating	UL94V-2
I/O Pack Casing Protection Against Intrusion	Ingress Protection Code: IP20 per EN 60529
General Mark VIe I/O Pack Specifications	Refer to GEH-6721_Vol_I for technical regulations and standards that apply to all of the Mark VIeS control system equipment
YUAA Module Dimensions	6.6 in L x 3.4 in W x 4.3 in H (with I/O pack attached) Average panel area/channel is equal to small S card footprint per group of 16 channels
Mode Miswired Tolerance	Refer to the ToolboxST Configuration *Modes* section for details regarding YUAA resistance to damage when incorrectly wired or configured.

YUAA Specifications (continued)

Item	Specification
Group Isolation	Exists internally between the processor and the IONet ports to break ground loops, using high resistance barriers
Channel Terminal Voltage	Operation is guaranteed only when channel terminals are connected to signal voltages between 20 to -11 volts with respect to COM. For voltages outside this range, an external resistor may be required for correct operation. Refer to the section *Digital Inputs and Outputs*. Signals above 24.5 or below -13 V with respect to COM will affect performance across other channels and could cause long term degradation of the performance. Voltages beyond ± 28 V are clamped by transorbs for protection.

YUAA mA/HART Specifications

Item	Specification
Number of Channels	16 channels per terminal board possible as inputs or outputs
Input Span	4-20 mA dc with allowance for 0-24 mA to cover NAMUR fault conditions
Input Converter Resolution	16-bit analog-to-digital converter
HART Rx and Cx Values	250 ohms in parallel with 5000 pF for HART inputs 14 kohms with 11000 pF for HART current outputs
Scan Time	Normal scan 5 ms (200 Hz). Note that controller frame rate is 100 Hz.
Measurement Accuracy	Better than 0.1% full scale over the temperature range -40 to 70°C.
Noise Suppression on Inputs	A software filter, using a two-pole, low-pass filter, is configurable for: off (0), .75, 1.5 Hz, 3 Hz, 6 Hz, 12 Hz for mA and HART inputs
Common Mode Rejection	Ac common mode rejection 60 dB at 60 Hz, with up to ±5 V common mode voltage. Dc common mode rejection 80 dB with -5 to +7 peak V common mode voltage
Common Mode Voltage Range	±5 V
Output Converter	16-bit D/A converter with 0.5% accuracy over 0 to 24 mA possible span
Output Load	800 Ω for 0-20 mA output

YUAA Performance

Channel Configuration	Rating
mA/HART Inputs	4 to 20 mA at 0.1% accuracy over temperature range *In presence of severe conducted RF interference (IEC 61000-4-6, 10 V rms), the accuracy may degrade to 1.5%.* *In presence of severe radiated RF interference (IEC 61000-4-3, 10 V/m), internal wetted mA input accuracy may degrade to 2% and external wetted mA input accuracy may degrade to 20%.*
Voltage Inputs	± 5 V dc or ±10 V dc at 0.1% accuracy over temperature range
mA Outputs	0 to 20 mA with 0.5% accuracy, compliance up to 18 V dc with 22 V or higher field supply 0-800 ohm load with current monitoring as a variable OutxxMA with 3% accuracy *In the presence of severe radiated RF interference (IEC 61000-4-3, 10 V/m), the accuracy may degrade to 3%.*
Thermocouple Inputs	E, J, K, S, T, B, N, R thermocouples with 0.1 % measurement accuracy of full scale **Caution** **The CJC sensor accuracy varies with the amount of power dissipated in the PUAA package. For a setting of 16 thermocouples, the CJC provide 2 °F accuracy. For best accuracy with local CJC, mount the PUAA at the bottom of the cabinet far from higher power devices or PUAA using higher power modes. If combining thermocouples with high power modes such as mA outputs, the CJC may degrade in accuracy up to 4 °F. A practical limit on mixing modes is to limit up to 8 mA outputs on any PUAA with other channels set for thermocouples.** **For best accuracy it is recommended that remote cold junctions be used due to heat dissipation from analog outputs and input modes. The remote cold junction value may be from either RTD channels on the same PUAA with variables passed to application code or from other devices read by the application code such as another PUAA or PRTD.**
	RSS Accuracy of 53 uV on 45 mV span (E, J, K, S, T)
	RSS Accuracy of 115 uV on 95 mV span (B, N, R)
	Open wire detection is supported
	Wiring Resistance: round trip between channel terminals is less than 100 ohms for full accuracy
RTD Inputs	120 ohm Nickel ± 2°F at 400 °F 100 ohm Platinum ± 4°F at 400 °F 200 ohm Platinum ± 2°F at 400 °F 10 ohm Copper ± 10 °F at 400 °F Resistance up to 450 ohms Scan time: 500 ms *In the presence of severe conducted RF interference (IEC 61000-4-6, 10 V rms), the resistance accuracy may degrade to 2%. The associated temperature accuracy will similarly vary with the amount based on the type of sensor.*
Discrete Inputs	10 to 20 V external wetted switches into 12.5 Kohm internal load Sequence of Event (SOE) tagging per I/O frame for first, second, and last change with 1 msec resolution 22 to 30 V external wetted switches using a series or a series-parallel set of 8.2 Kohm resistors Line monitoring (open/short detection) is optional for external wetting using two 8.2 Kohm resistors at contact Line monitoring (open/short detection) is not supported on > 20 V external wetted switches Internal wetted switches with 10 mA contact current, 22 V open contact voltage Line monitoring (open/short detection) is optional for internal wetting using two 240 ohm resistors at contact

YUAA Performance (continued)

Channel Configuration	Rating
Discrete Outputs	Up to 24 mA at up to 22 V using mA output mode, capable of driving control circuits of many external interposing electromagnetic (Phoenix Contact 2961105 on DIN base PLC-BSP-24DC/21) or solid state (Crydom DC60S7 60Vdcc 7A) relays using under 22 mA control current with panel or DIN rail mounting near the SUAA base. SOE is not supported on analog outputs to drive external interposing circuits.
Pulse Accumulators	16-bit accumulator Voltage range: -10 to 20 V Frequency range: 0 to 500 Hz

YUAA Orderable Part Numbers

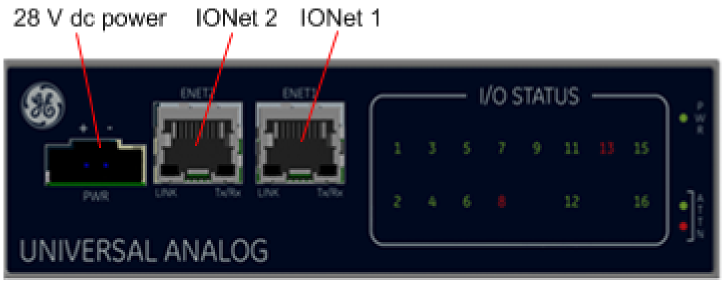
Part Numbers	Description
IS430SSUAH1A	Complete assembled Simplex module made up of one IS420YUAAS1A attached to one IS410SUAAS1A, and includes the base/mounting and hardware/cover
IS420YUAAS1A	YUAA I/O module with captive mounting screws
IS410SUAAS1A	Simplex terminal board on DIN-rail mountable base
IS400SUAAS1A	Simplex terminal board only

17.4 Module Installation and Mounting

Perform the procedures in this section to install and mount a new PUAA/YUAA module into an existing Mark VIe or Mark VIeS cabinet.

17.4.1 Installation

The 16-channel module can be mounted with terminal blocks facing either left or right direction when mounted on a vertical DIN rail, using pluggable Euro-style terminal blocks. The average panel area/channel (dimensions) is approximately the same as an existing Mark VIe or Mark VIeS small S-terminal board footprint.



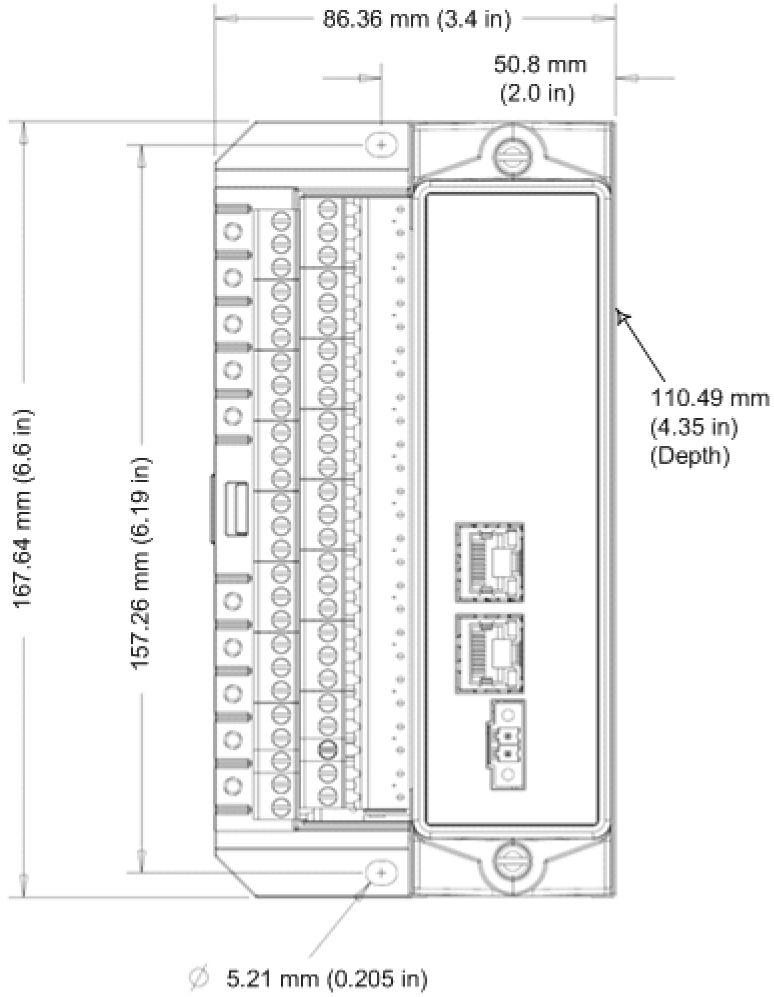
➢ To install the PUAA/YUAA module into an existing Mark VIe or Mark VIeS cabinet

1. Follow all standard safety and LOTO procedures and agency or specific area / location requirements for safety.
2. Securely mount the SUAA terminal board to the cabinet. It uses the same DIN mounting columns as existing Mark VIe or Mark VIeS terminal boards. Refer to the section *Mounting* for mechanical dimensions and thermal management requirements.
3. If not already attached, connect the PUAA/YUAA I/O pack to the terminal board using the two screws, and tighten to 2.146 Nm (19 in lb) torque.
4. Plug in one or two Ethernet cables to the RJ-45 connector(s) depending on the IONet configuration. The I/O pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
5. Attach the appropriate (24 – 12 AWG) wires to the terminal board screws depending on channels and devices being used. Tighten field wiring to 0.45 Nm (4 in lb). The terminal blocks are removable on a channel by channel basis. Field wiring shield ground connections are available on the metal frame of the module, separate from but adjacent to the removable terminal block. This requires the use of a metal shield strip similar to existing Mark VIe or Mark VIeS terminal block brackets. Be aware that there is no isolation between the control and field side analog electronics. Refer to the section *SUAA Universal Analog Terminal Board* for more information, including a diagram and complete terminal board screw definitions.
    a. For new installations, refer to the table *Wiring and Configuration for New Installs* for available modes, then refer to the appropriate wiring diagrams.
    b. For retrofit installations, refer to the instructions related to the existing terminal board being replaced by the SUAA: *STAI/SHRA Retrofits*, *STAO Retrofits*, *STTC Retrofits*, *SRTD Retrofits*, or *24 V STCI Retrofits*.
6. Apply power to the I/O pack by plugging in the 28 V dc connector. It is not necessary to remove power from the cable before plugging it in because the I/O pack has inherent soft-start capability that controls current inrush on power application.
7. Using the ToolboxST* application, configure and download to the I/O pack as necessary. Be sure that the IONet configuration matches the cable connections to the I/O pack.
    a. For new installations, refer to the table *Wiring and Configuration for New Installs*, then refer to the appropriate *ToolboxST configuration sections* in this document for those Modes.

b. For retrofit installations, from the ToolboxST application open the existing system with the I/O pack that is being replaced with the new module, then generate an I/O report and a Configuration Report for the existing I/O pack. Using these reports, configure the new PUAA/YUAA I/O pack as a replacement to the existing I/O pack.

17.4.2 Mounting

The PUAA/YUAA module can be mounted to either a standard 35 mm (1.38 in) DIN-rail or directly mounted to a panel using the two 5.2 mm (0.21 in) slotted holes on the module base.

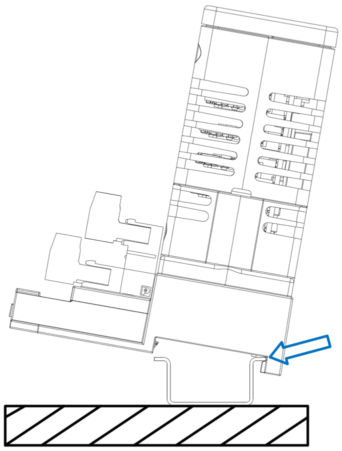
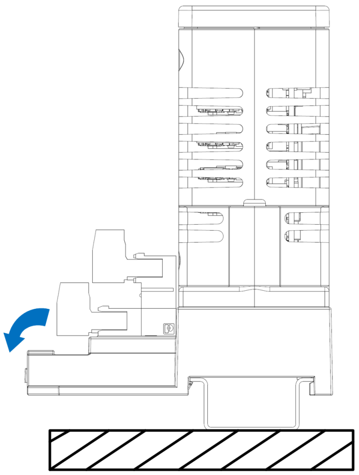
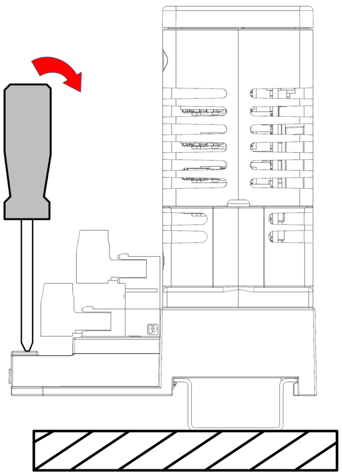
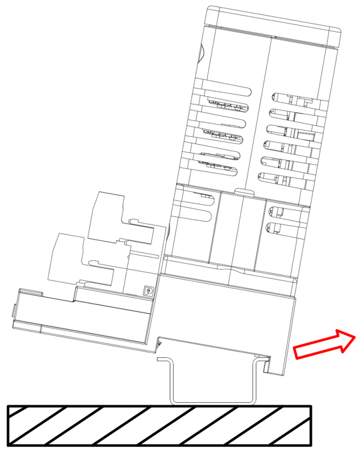


Mounting Dimensions

The module can be mounted with the terminal strips either left or right facing. It cannot be mounted with the terminals top or bottom facing as this impedes the convection flow required to ensure adequate cooling of the internal components. There are no spacing requirements to ensure adequate module cooling. Spacing the modules at the standard Mark VIe or Mark VIeS spacing of 170 mm (6.7 in) will allow for a small gap between the modules but is not required for cooling purposes.

The module can be assembled to standard 35 mm (1.38 in) DIN-rail (7.5 mm [0.30 in], and 15 mm [0.60 in] height). The module position relative to the DIN-rail center line is 23 mm (0.9 in). The module base is designed to lock onto the DIN-rail and resist sliding without the use of rail stops. Removal and reinstallation or transfer of the module from one rail to another can reduce the effectiveness of the locking features. In such cases, the addition of rail stops or base replacement may be required.

PUAA/YUAA DIN-rail Installation and Removal

For **installation**, engage the rear DIN rail guide over the edge of the module and rotate downward to snap the module onto the rail. First time installation may require extra force to engage the rail locking		
For **removal**, Use a large flat bladed screwdriver to pull the rail clip away from the rail. Rotate the module back and slide away from the rail.		

17.4.3 Wiring and Configuration

For available modes and wiring and configuration instructions for new installations, refer to the table in the section *Wiring and Configuration for New Installs*.

For wiring and configuration instructions for retrofit installations related to the existing terminal board being replaced by the SUAA, refer to the following sections:

- *Wiring and Configuration for STAI/SHRA Retrofits*
- *Wiring and Configuration for STAO Retrofits*
- *Wiring and Configuration for STTC Retrofits*
- *Wiring and Configuration for SRTD Retrofits*
- *Wiring and Configuration for 24 V STCI Retrofits*.

17.4.3.1 Wiring and Configuration for New Installs

The following table provides a complete list of available Analog modes with links to the appropriate wiring and configuration instructions.

Mode	Field Device	Wiring Diagrams	ToolboxST Configuration
CurrentInput (with HART option)	4–20 mA Input Internally and externally powered	*Analog Inputs*	*Current Inputs*
VoltageInput	± 5 V or ± 10 V input internally and externally powered		*Voltage Inputs*
CurrentOutput (with HART option)	0–20 mA Output	*Current Outputs*	*Current Outputs*
RTD	*RTD types*	*RTD Inputs*	*RTDs*
Thermocouple	*TC types* Local or Remote CJs	*Thermocouple Inputs*	*Thermocouples*
DigitalInput	External switches	*Digital Inputs*	*Digital Inputs*

Refer the section *SUAA Universal Analog Terminal Board* for more information, including a diagram and complete terminal board screw definitions.

17.4.3.2 Wiring and Configuration for STAI or SHRA Retrofits

The following table provides field wiring and channel comparisons for retrofitting an existing STAI or SHRA with a SUAA terminal board to provide current or voltage inputs, and two current outputs. The PUAA/YUAA and SUAA are not isolated as on the prior analog input module (PAIC/YAIC) or analog HART module (PHRA/YHRA).

Attention

HART inputs are always referenced to ground, however mA inputs allow either floating or grounded style.

STAI Screw	STAI Name	Channel	SUAA screw	SUAA Name	Use
1	P24V	1	1	PWR_RET	PWR Out if internally powered not used if externally powered
2	20mA	1	3	IO+	mA In (Mode set from ToolboxST for PUAA/YUAA)
3	VDC	1	3	IO+	V In (Mode set from ToolboxST for PUAA/YUAA)
4	Ret	1	5	IO-	Ground for 3 wire devices Ground for externally powered 2 wire Ground for externally powered 4 wire Not used for 2 wire internally powered 2nd AI for special-case internally powered 4-wire device
5	P24V	2	2	PWR_RET	Same as SUAA screw 1
6	20mA	2	4	IO+	Same as SUAA screw 3
7	VDC	2	4	IO+	Same as SUAA screw 3
8	Ret	2	6	IO-	Same as SUAA screw 5
9	P24V	3	7	PWR_RET	Same as SUAA screw 1
10	20mA	3	9	IO+	Same as SUAA screw 3
11	VDC	3	9	IO+	Same as SUAA screw 3
12	Ret	3	11	IO-	Same as SUAA screw 5
13	P24V	4	8	PWR_RET	Same as SUAA screw 1
14	20mA	4	10	IO+	Same as SUAA screw 3
15	VDC	4	10	IO+	Same as SUAA screw 3
16	Ret	4	12	IO-	Same as SUAA screw 5
17	P24V	5	13	PWR_RET	Same as SUAA screw 1
18	20mA	5	15	IO+	Same as SUAA screw 3
19	VDC	5	15	IO+	Same as SUAA screw 3
20	Ret	5	17	IO-	Same as SUAA screw 5
21	P24V	6	14	PWR_RET	Same as SUAA screw 1
22	20mA	6	16	IO+	Same as SUAA screw 3
23	VDC	6	16	IO+	Same as SUAA screw 3
24	Ret	6	18	IO-	Same as SUAA screw 5
25	P24V	7	19	PWR_RET	Same as SUAA screw 1
26	20mA	7	21	IO+	Same as SUAA screw 3
27	VDC	7	21	IO+	Same as SUAA screw 3
28	Ret	7	23	IO-	Same as SUAA screw 5
29	P24V	8	20	PWR_RET	Same as SUAA screw 1
30	20mA	8	22	IO+	Same as SUAA screw 3
31	VDC	8	22	IO+	Same as SUAA screw 3
32	Ret	8	24	IO-	Same as SUAA screw 5
33	P24V	9	25	PWR_RET	Same as SUAA screw 1
34	20mA	9	27	IO+	Same as SUAA screw 3
35	VDC	9	27	IO+	Same as SUAA screw 3
36	Ret	9	29	IO-	Same as SUAA screw 5
37	P24V	10	26	PWR_RET	Same as SUAA screw 1
38	20mA	10	28	IO+	Same as SUAA screw 3
39	VDC	10	28	IO+	Same as SUAA screw 3

STAI Screw	STAI Name	Channel	SUAA screw	SUAA Name	Use
40	Ret	10	30	IO-	Same as SUAA screw 5
41	PCOM		49	COM	Ground for special-use 4-wire internally powered devices
42	PCOM		50	COM	Ground for special-use 4-wire internally powered devices
43	PCOM		51	COM	Ground for special-use 4-wire internally powered devices
44	PCOM		52	COM	Ground for special-use 4-wire internally powered devices
45	OP1	11	33	IO+	current output 1
46	OR1	11	35	IO-	return for current output 1
47	OP2	12	34	IO+	current output 2
48	OR2	12	36	IO-	return for current output 2

17.4.3.3 Wiring and Configuration for STAO Retrofits

The following table provides a field wiring and channel comparison for retrofitting an existing STAO with a SUAA terminal board to provide current outputs.

STAO Screw	STAO Name	Channel	SUAA Screw	SUAA Name	Use
1	AO	1	3	IO+	AO Signal
2	Ret	1	5	IO-	Return
3	AO	2	4	IO+	AO Signal
4	Ret	2	6	IO-	Return
5	AO	3	9	IO+	AO Signal
6	Ret	3	11	IO-	Return
7	AO	4	10	IO+	AO Signal
8	Ret	4	12	IO-	Return
9	AO	5	15	IO+	AO Signal
10	Ret	5	17	IO-	Return
11	AO	6	16	IO+	AO Signal
12	Ret	6	18	IO-	Return
13	AO	7	21	IO+	AO Signal
14	Ret	7	23	IO-	Return
15	AO	8	22	IO+	AO Signal
16	Ret	8	24	IO-	Return
17	Chassis Ground		Chassis		
18	Chassis Ground		Chassis		
19-36	No connects		n/c		

17.4.3.4 Wiring and Configuration for STTC Retrofits

The following table provides a field wiring and channel comparison for retrofitting an existing STTC with a SUAA terminal board to provide thermocouple inputs. The PUAA/YUAA and SUAA are not isolated as on the prior analog modules for thermocouples (PTCC/YTCC).

STTC Screw	STTC Name	Channel	SUAA Screw	SUAA Name
1	TC_P	1	3	IO+
2	TC_N	1	5	IO-
3	Shield		Chassis	
4	Shield		Chassis	
5	TC_P	2	4	IO+
6	TC_N	2	6	IO-
7	TC_P	3	9	IO+
8	TC_N	3	11	IO-
9	Shield		Chassis	
10	Shield		Chassis	
11	TC_P	4	10	IO+
12	TC_N	4	12	IO-
13	TC_P	5	15	IO+
14	TC_N	5	17	IO-
15	Shield		Chassis	
16	Shield		Chassis	
17	TC_P	6	16	IO+
18	TC_N	6	18	IO-
19	TC_P	7	21	IO+
20	TC_N	7	23	IO-
21	Shield		Chassis	
22	Shield		Chassis	
23	TC_P	8	22	IO+
24	TC_N	8	24	IO-
25	TC_P	9	27	IO+
26	TC_N	9	29	IO-
27	Shield		Chassis	
28	Shield		Chassis	
29	TC_P	10	28	IO+
30	TC_N	10	30	IO-
31	TC_P	11	33	IO+
32	TC_N	11	35	IO-
33	Shield		Chassis	
34	Shield		Chassis	
35	TC_P	12	34	IO+
36	TC_N	12	36	IO-
37-40	No Connect		n/c	
41	Shield		Chassis	
42	Shield		Chassis	

17.4.3.5 Wiring and Configuration for SRTD Retrofits

The following table provides a field wiring and channel comparison for retrofitting an existing SRTD with a SUAA terminal board to provide RTD inputs.

SRTD Screw	SRTD Name	Channel	SUAA screw	SUAA Name	Use
1	EX01	1	5	IO-	Excitation
2	SIG01	1	3	IO+	Signal
3	RET01	1	1	PWR_RET	Return
4	EX02	2	6	IO-	Excitation
5	SIG02	2	4	IO+	Signal
6	RET02	2	2	PWR_RET	Return
7	EX03	3	11	IO-	Excitation
8	SIG03	3	9	IO+	Signal
9	RET03	3	7	PWR_RET	Return
10	EX04	4	12	IO-	Excitation
11	SIG04	4	10	IO+	Signal
12	RET04	4	8	PWR_RET	Return
13	EX05	5	17	IO-	Excitation
14	SIG05	5	15	IO+	Signal
15	RET05	5	13	PWR_RET	Return
16	EX06	6	18	IO-	Excitation
17	SIG06	6	16	IO+	Signal
18	RET06	6	14	PWR_RET	Return
19	EX07	7	23	IO-	Excitation
20	SIG07	7	21	IO+	Signal
21	RET07	7	19	PWR_RET	Return
22	EX08	8	24	IO-	Excitation
23	SIG08	8	22	IO+	Signal
24	RET08	8	20	PWR_RET	Return
25-34	No connects		n/c		
35	Chassis for shields		Chassis		
36	Chassis for shields		Chassis		

17.4.3.6 Wiring and Configuration for 24 V STCI Retrofits

The 24 channels of the STCI cannot be fully mapped to the 16 channels of the SUAA due to fewer channels in the PUAA/YUAA. The following table assumes that the first 16 channels of the STCI are mapped, where channels 17 to 24 would be wired to a second SUAA's channels 1 to 8. The STCI is internally wired for internal wetted contacts using external supplies, while the SUAA allows for internal fed switches using internal supplies. Therefore, terminals 49 to 52 are not reconnected on the SUAA.

STCI Screw	STCI Name	Channel	SUAA Screw	SUAA Name	Use
1	Input 1 (Positive)	1	SUAA #1 screw 1	PWR_RET for Channel 1	Positive feed to switch # 1
2	Input 1 (Signal)	1	SUAA #1 screw 3	I/O+ for Channel 1	Return path from switch #1
3	Input 2 (Positive)	2	SUAA #1 screw 2	PWR_RET for Channel 2	Positive feed to switch # 2
4	Input 2 (Signal)	2	SUAA #1 screw 4	I/O+ for Channel 2	Return path from switch #2
5	Input 3 (Positive)	3	SUAA #1 screw 7	PWR_RET for Channel 3	Positive feed to switch # 3
6	Input 3 (Signal)	3	SUAA #1 screw 9	I/O+ for Channel 3	Return path from switch #3
7	Input 4 (Positive)	4	SUAA #1 screw 8	PWR_RET for Channel 4	Positive feed to switch # 4
8	Input 4 (Signal)	4	SUAA #1 screw 10	I/O+ for Channel 4	Return path from switch #4
9	Input 5 (Positive)	5	SUAA #1 screw 13	PWR_RET for Channel 5	Positive feed to switch # 5
10	Input 5 (Signal)	5	SUAA #1 screw 15	I/O+ for Channel 5	Return path from switch #5
11	Input 6 (Positive)	6	SUAA #1 screw 14	PWR_RET for Channel 6	Positive feed to switch # 6
12	Input 6 (Signal)	6	SUAA #1 screw 16	I/O+ for Channel 6	Return path from switch #6
13	Input 7 (Positive)	7	SUAA #1 screw 19	PWR_RET for Channel 7	Positive feed to switch # 7
14	Input 7 (Signal)	7	SUAA #1 screw 21	I/O+ for Channel 7	Return path from switch #7
15	Input 8 (Positive)	8	SUAA #1 screw 20	PWR_RET for Channel 8	Positive feed to switch # 8
16	Input 8 (Signal)	8	SUAA #1 screw 22	I/O+ for Channel 8	Return path from switch #8
17	Input 9 (Positive)	9	SUAA #1 screw 25	PWR_RET for Channel 9	Positive feed to switch # 9
18	Input 9 (Signal)	9	SUAA #1 screw 27	I/O+ for Channel 9	Return path from switch #9
19	Input 10 (Positive)	10	SUAA #1 screw 26	PWR_RET for Channel 10	Positive feed to switch # 10
20	Input 10 (Signal)	10	SUAA #1 screw 28	I/O+ for Channel 10	Return path from switch #10
21	Input 11 (Positive)	11	SUAA #1 screw 31	PWR_RET for Channel 11	Positive feed to switch # 11
22	Input 11 (Signal)	11	SUAA #1 screw 33	I/O+ for Channel 11	Return path from switch #11
23	Input 12 (Positive)	12	SUAA #1 screw 32	PWR_RET for Channel 12	Positive feed to switch # 12
24	Input 12 (Signal)	12	SUAA #1 screw 34	I/O+ for Channel 12	Return path from switch #12
25	Input 13 (Positive)	13	SUAA #1 screw 37	PWR_RET for Channel 13	Positive feed to switch # 13
26	Input 13 (Signal)	13	SUAA #1 screw 39	I/O+ for Channel 13	Return path from switch #13
27	Input 14 (Positive)	14	SUAA #1 screw 38	PWR_RET for Channel 14	Positive feed to switch # 14
28	Input 14 (Signal)	14	SUAA #1 screw 40	I/O+ for Channel 14	Return path from switch #14
29	Input 15 (Positive)	15	SUAA #1 screw 43	PWR_RET for Channel 15	Positive feed to switch # 15
30	Input 15 (Signal)	15	SUAA #1 screw 45	I/O+ for Channel 15	Return path from switch #15
31	Input 16 (Positive)	16	SUAA #1 screw 44	PWR_RET for Channel 16	Positive feed to switch # 16
32	Input 16 (Signal)	16	SUAA #1 screw 46	I/O+ for Channel 16	Return path from switch #16
33	Input 17 (Positive)	17	SUAA #2 screw 1	PWR_RET for Channel 17	Positive feed to switch # 17
34	Input 17 (Signal)	17	SUAA #2 screw 3	I/O+ for Channel 17	Return path from switch #17
35	Input 18 (Positive)	18	SUAA #2 screw 2	PWR_RET for Channel 18	Positive feed to switch # 18
36	Input 18 (Signal)	18	SUAA #2 screw 4	I/O+ for Channel 18	Return path from switch #18
37	Input 19 (Positive)	19	SUAA #2 screw 7	PWR_RET for Channel 19	Positive feed to switch # 19
38	Input 19 (Signal)	19	SUAA #2 screw 9	I/O+ for Channel 19	Return path from switch #19
39	Input 20 (Positive)	20	SUAA #2 screw 8	PWR_RET for Channel 20	Positive feed to switch # 20
40	Input 20 (Signal)	20	SUAA #2 screw 10	I/O+ for Channel 20	Return path from switch #20
41	Input 21 (Positive)	21	SUAA #2 screw 13	PWR_RET for Channel 21	Positive feed to switch # 21
42	Input 21 (Signal)	21	SUAA #2 screw 15	I/O+ for Channel 21	Return path from switch #21
43	Input 22 (Positive)	22	SUAA #2 screw 14	PWR_RET for Channel 22	Positive feed to switch # 22

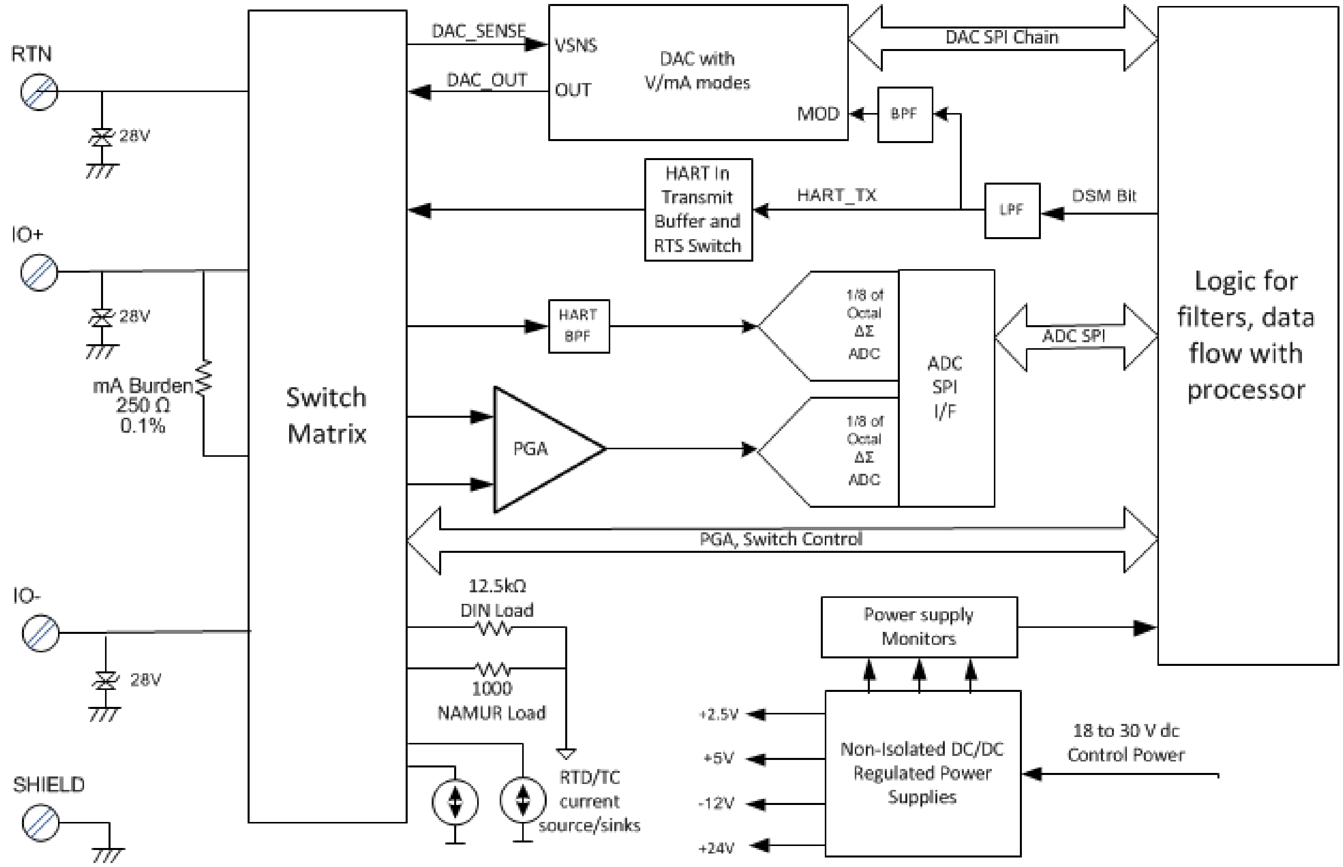
STCI Screw	STCI Name	Channel	SUAA Screw	SUAA Name	Use
44	Input 22 (Signal)	22	SUAA #2 screw 16	I/O+ for Channel 22	Return path from switch #22
45	Input 23 (Positive)	23	SUAA #2 screw 19	PWR_RET for Channel 23	Positive feed to switch # 23
46	Input 23 (Signal)	23	SUAA #2 screw 21	I/O+ for Channel 23	Return path from switch #23
47	Input 24 (Positive)	24	SUAA #2 screw 20	PWR_RET for Channel 24	Positive feed to switch # 24
48	Input 24 (Signal)	24	SUAA #2 screw 22	I/O+ for Channel 24	Return path from switch #24
49	Excitation Positive	ALL	None	None	Leave disconnected, internally supplied by PUAA
50	Excitation Positive	ALL	None	None	Leave disconnected, internally supplied by PUAA
51	Excitation Negative	ALL	None	None	Leave disconnected, internally supplied by PUAA
52	Excitation Negative	ALL	None	None	Leave disconnected, internally supplied by PUAA

17.5 Operation

The following features are common to the distributed I/O modules:

- *BPPx Processor*
- *Processor LEDs*
- *Power Management*
- *ID Line*
- *I/O Module Common Diagnostic Alarms*

The PUAA/YUAA I/O pack uses a switch block in each channel to configure signal flow to and from a DAC, a HART interface, a PGA, and current sources. The following diagram illustrates the channel organization.



PUAA/YUAA Channel Organization

Settings for the switches and circuitry vary by the selected mode of operation, as follows:

- Thermocouples and voltage inputs connect through the switch block to the PGA and A/D. The PGA is set for an appropriate gain based on the voltage span. Thermocouples are also periodically tested for burnout, where a multiplexed set of current source and sink pulses a weak 10 microamperes current through the external thermocouple. If the thermocouple has too high a resistance or has opened, the PGA senses the excessive shift in voltage. Voltage inputs do not use the burnout pulse test.
- RTD inputs use the multiplexed set of current sources to pass two equal currents to IO+ and IO-, as well as across the external resistor sensor. The third leg of the sensor is connected to RTN and ground using the switch block. The PGA senses the voltage between IO+ and IO-, where any voltage drops on the wiring are cancelled out.
- mA inputs connect a burden resistor in the current path with the PGA and A/D to sense the amount of current flow. If the input is internally fed, the DAC is set for 24 mA to drive the loop with the return path through the burden to ground, allowing the external device to regulate the current. An optional HART connects a bandpass filter to the burden resistor, sensing any tone signals sent from the external device. A switched transmit path driver also connects to the burden resistor for modulating the voltage on the burden resistor when PUAA/YUAA communicates back to the external device.

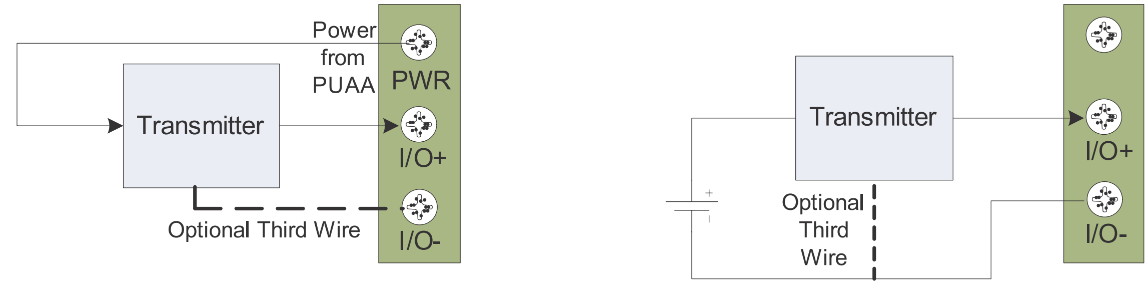
- mA outputs connect the DAC to the external actuator with the return path passed to ground. Confirmation of the current is received by the PGA sensing the voltage drop on a series resistor at the DAC output. If the HART option is enabled, the DAC may be modulated with an AC tone to communicate to the external actuator with the response sensed by connecting a bandpass filter and A/D to the output terminal.
- Digital inputs are similar to the ma input settings, with specific paths set by the options:
    - Externally-fed switch inputs are connected to IO+ and then to a 12.5K input load to ground. The PGA has a 20 V limit so a series resistor is added for higher field supplies to avoid false error alarms for excess input voltage.
    - Externally-fed switches with line monitoring (open/short detection) use two external resistors in series with and parallel to the external switch. This connects to the 12.5K input load with the PGA/ADC path used to check for voltages in correct ranges. If too high or too low the external wiring is declared to be faulty.
    - Internally-fed switches use the DAC to drive a current through the external switch and back through the mA burden resistor to ground. For a simple switch input, the DAC is set for 10 mA flow. By sensing the burden resistor voltage, the switch state is determined. An option for line monitoring (open/short detection) with two resistors allows for fault checking, where the DAC is set for 5 V to allow for the current to change.
    - NAMUR style sensors use a device connected to the PUAA/YUAA set for 8.2 V output with a 1K series resistance. By sensing the terminal voltage, the amount of current flow is derived and in turn the external device state is determined as on, off, or faulty.

All of the settings are provided through complex programmable logic device (CPLD) controlling groups of four channels, supporting commands to the switch block settings, dataflow to the DAC for output settings, dataflow from the PGA and HART ADC channels (one for low bandwidth signals covering DC to 20 Hz, and a second for bandpass energy on HART signaling), first stage of decimation and filtering, HART modulation output using a delta sigma bit output feeding a hardware low pass filter, and data transfers with the PUAA/YUAA's processor board's FPGA. The processor and FPGA provide a second level of filtering and decimation down to the frame rate along with completion of the HART demodulation and UART functions.

17.6 Analog Inputs (Voltage or mA Current)

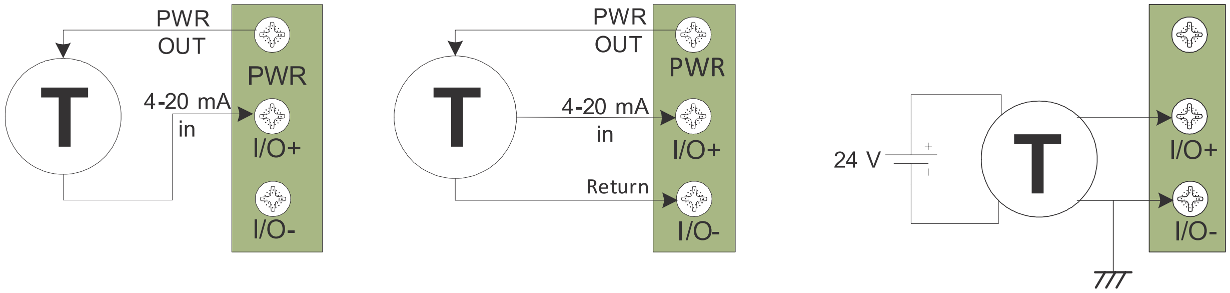
There are three connections per analog channel providing local power output with current limiting (PWR_RTN), IO+ signal, and IO- signal/return as needed for each functional mode (4–20 mA, ± 5 V dc, or ± 10 V dc). The following figures provide typical wiring options.

Note HART is optional for all internally powered mA input modes. HART is not supported for externally powered devices.



Internally powered 2 or 3 wire field device

Externally powered 2 or 3 wire field device



Two Wire Transmitter using DAC Supplied Source

Three Wire Transmitter with Return Line

External Powered Four-wire Transmitter

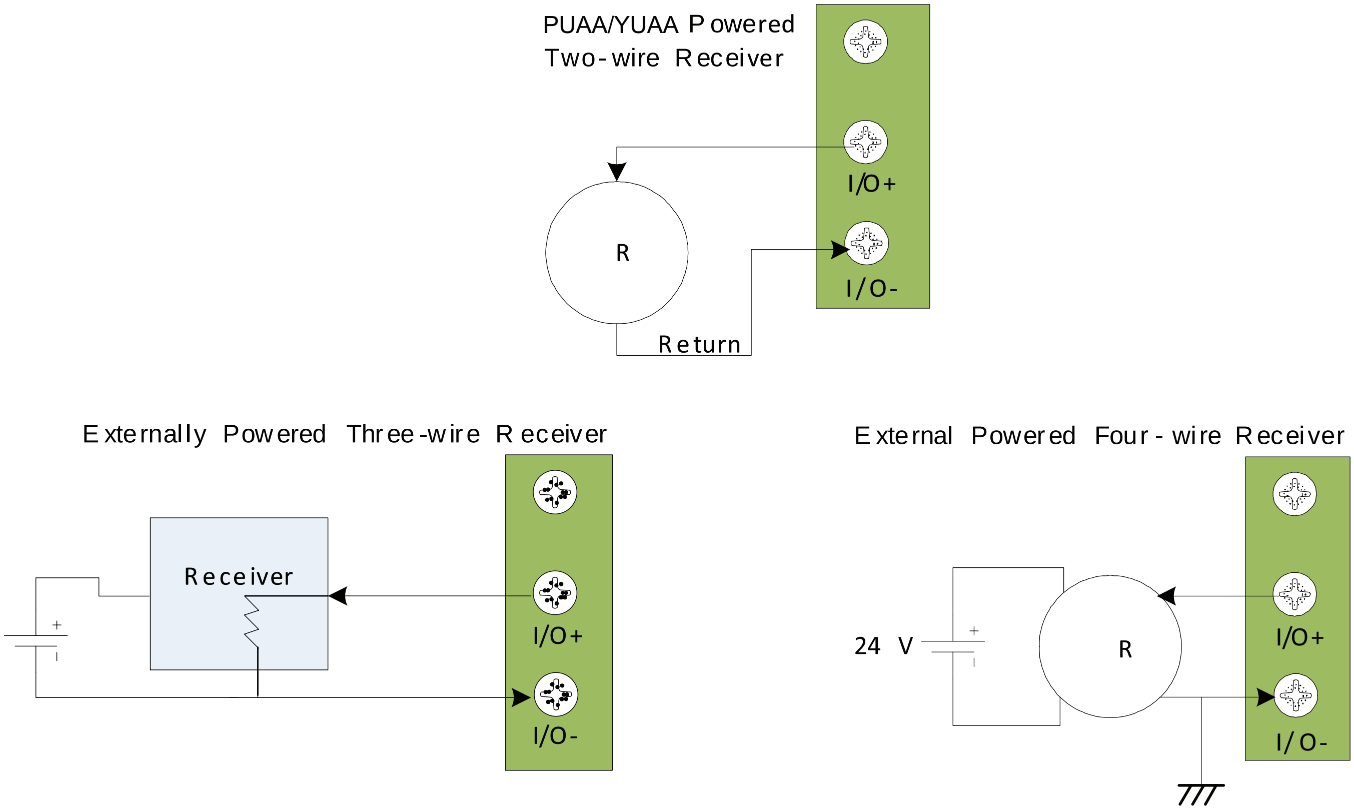
Analog Inputs Wiring Options

Caution

Internally powered 2 or 3 wire devices use the analog output DAC set at 24 mA. While there is no thermal derating for number of active analog outputs at ambients up to 158 °F) (70°C), it is possible for a fault condition with shorted leads to cause all power dissipation to be within the PUAA package. In this situation, there may be thermal alarms annunciated for the processor board.

17.7 Current Outputs

The following are typical channel wiring options for mA outputs. HART option is supported. Dithering is not supported.


PUAA/YUAA Powered Two-wire Receiver
R
Return
I/O+
I/O-
Externally Powered Three-wire Receiver
Receiver
+
I/O+
I/O-
External Powered Four-wire Receiver
24 V
+
R
I/O+
I/O-

0–20 mA Analog Current Outputs

Caution

To avoid false heat alarms, ensure that the output loads are more than 600 ohms for the loop current (moving power dissipation and heat to outside of the PUAA/YUAA package) when using more than 8 channels of Current Output at ambient temperatures above 60°C (140 °F).

It is possible to drive into shorted loads causing all power dissipation to be within the PUAA/YUAA package. In this situation, there may be thermal alarms generated from the processor board while in hot ambient conditions.

17.8 HART-Enabled mA Inputs and Outputs

All channels on the PUAA are HART capable when assigned to mA input or output. Therefore, there can be up to 16 individual HART channels, with the data delivery to the controller over IONet split into two groups of 8 points (data for IOPoints 1-8 is grouped together, and data for IOPoints 9-16 is grouped together).

From the ToolboxST Component Editor, there is no separate configuration tab for HART. Assigning channels to HART uses the same mA input or mA output configuration, where within the mA input or output tab there are additional settings for HART_Enable, HART_CtrlVars, HART_ExStatus, HART_MfgID, HART_DevType, and HART_DEVID.

In order to conserve the dataflow for the PUAA, there are three stages of deployment based on HART assignments:

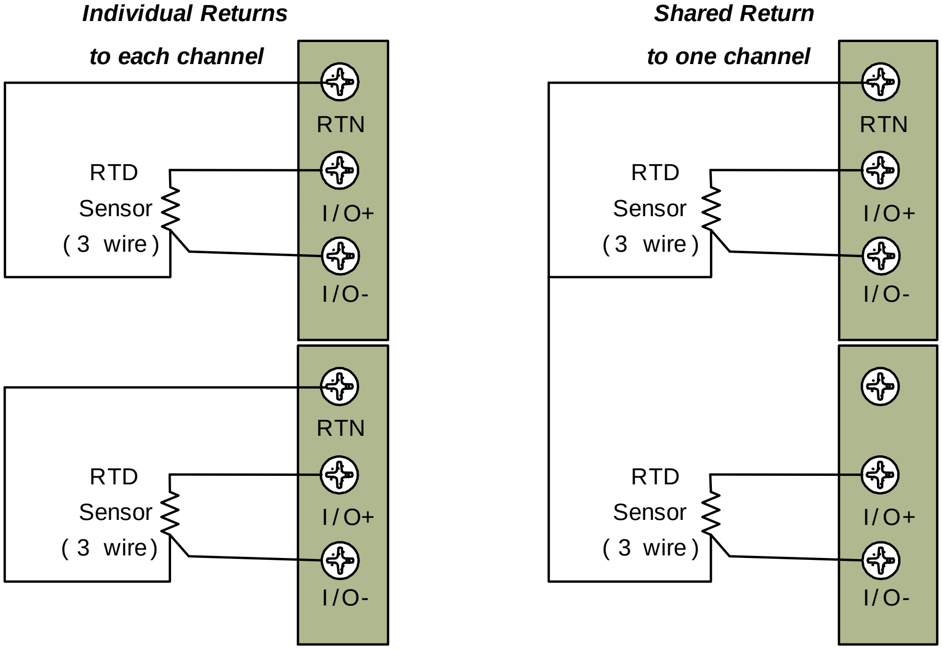
- No channels are assigned to HART with no HART transfers used on IONET for maximum available number of channels per controller
- 1 up to 8 channels assigned to HART within a single group of 8 channels (1 to 8) or (9 to 16), requiring a pack reboot when first assigned to allocate data transfers for a single HART group of channels
- Channels assigned across both HART groups, requiring a second pack reboot upon the first channel assigned to the second group to allocate a second set of data transfers for both HART groups of channels.

The reboots for HART traffic are only required when first assigning a channel within a group as part of a download to the PUAA. Once the first channel is assigned in a group, additional channels may be assigned on following downloads without a reboot of the pack. If channels being assigned in a download are within both groups of HART channels, then only a single reboot is required.

17.9 RTD Inputs

The PUAA/YUAA has an RTD input performance equivalent to the existing PRTD/SRTD for RSS accuracy covering 100 to 200 ohm sensors, with slow speed only (no fast mode). Analog channels support RTD inputs covering resistance spans matching Nickel and Platinum sensors, as compared to the existing Mark VIe PRTD/SRTD. Resistance input from RTD sensors can be from 60 to 450 ohms, using 3–wire connections, with or without a shared return line.

RTD (3–wire) processing uses a single channel, with the channel alternating between voltage and current measurements to derive the sensed resistance. The currents are provided by the dual current sources, while the DAC terminal on the SUAA is an active ground to return the current. The PUAA does not support Fast mode, as is available with PCLA and PRTD. A single Slow mode of operation is used, with an acquisition time of 500 milliseconds or faster for 16 channels.



RTD Wiring

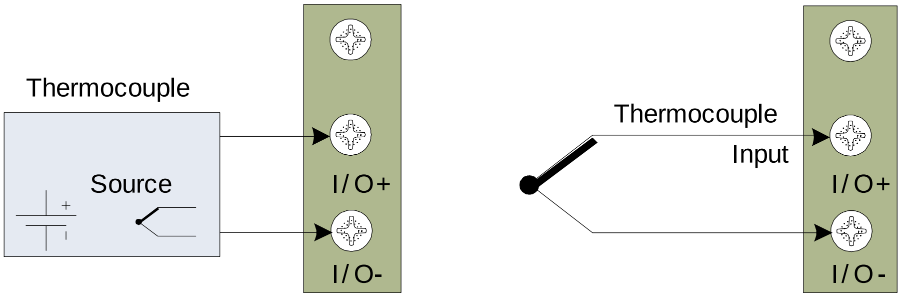
The I/O pack configuration and the final ohms value is used to lookup a temperature value based on the type of RTD selected. This final value is returned in signal space as either ohms or a temperature in degrees (Celsius or Fahrenheit set by parameter *TempUnits*). The available RTD types are displayed in the following table, using a current source of up to 1 mA with a compliance voltage range of up to 5 V.

RTD Types and Temperature Ranges

Value	RTD Type	Compatible Device Types	Min Temp (ºF)	Max Temp (ºF)
1	Minco PD	PT100 DIN	-325.893	1566.553
2	Minco PA	PT100 PURE	-323.885	1167.418
3	Minco PB	PT100 USIND Rosemount 104	-329.068	1166.875
4	Minco NA	N 120	-113.662	499.599
5	Minco PIA	None	-413.319	1765.473
6	Minco SAMA	SAMA 100	-322.438	1112.704
7	Minco PK	PT 200	-101.918	511.573
8	Minco PN	None	-101.918	511.573
10	Minco CA	CU10	-153.768	531.560
9	Ohms	Not Applicable	< 10 ohms	625 ohms

17.10 Thermocouple Inputs

PUAA/YUAA reads temperature inputs from thermocouples with E, J, K, S, T, B, N, and R styles, and has open wire detection and signal performance equivalent to a PTCC/YTCC I/O pack.



Supported TC Types and Temperature Ranges

TC Type	Min	Max
mV	-40	114
	Min Temp (ºF)	**Max Temp (ºF)**
T	-328	752
K	-328	2501.6
J	-337.38	2192
E	-328	1832
S	-40	3214.4
B	32	3308
N	-454	2372
R	-58	3214.4

Burnout detection on the input is based on a periodic pulse of current forcing the open terminal voltage outside the normal -40 to 95 mV region. Therefore, there may be a delay of up to 1 second from the time a sensor fails to when the burnout is detected. When the input goes open, the input terminal voltage typically drops close to zero. If the thermocouple sensor is hotter than the PUAA/YUAA screw temperature, the reported temperature reading will report colder (since the TC had been at a positive terminal input voltage). If the thermocouple sensor is colder than the PUAA/YUAA screw temperature, the temperature reading will momentarily report a warmer temperature, until the pulsed current source causes detection of the open circuit and the behavior specified by the **ReportOpenTC** parameter is applied.

Burnout Detection is only enabled on E, J ,K, S, T, B, N and R styles of thermocouples. When the **ReportOpenTC** parameter is set to Fail_Cold, the PUAA/YUAA will report Extrapolated values from TC tables at -40 mV (Open TC threshold). When **ReportOpenTC** is set to Fail_Hot, the PUAA/YUAA will report 2000 °C (3632 °F) depending on TempUnits selection. Burnout detection is disabled on mv selection. Therefore, ± 312.5 mV can be read with mv type selection with healthy zone limited from -40 mV to 114 mV.

Cold Junctions

Two Cold Junction temperature sensors located on the SUAA terminal board provide local cold junction temperature for Cold Junction compensation for Thermocouple inputs. The PUAA/YUAA products also supports the ability for the user to configure and use a Remote Cold Junction. The configuration between Local/Remote Cold Junction is determined by the ColdJuncType parameter on the PUAA/YUAA Parameters tab (remote or local). The Remote cold junction value is provided by the application by using the CJRemote variable in the Variables tab. From the Parameters tab, the TempUnits determines if the application is using °F or °C.

In addition, support is provided for the user to specify a Backup cold junction that gets used if either the Local or Remote Cold Junction is deemed unhealthy (out of range). The Backup Cold junction value is provided by the application by using the CJBackup variable in the Variables tab.

The temperature units for both BackupCJ and RemoteCJ will be assumed as equivalent to the setting of the TempUnits parameter on the Parameters tab.

Normal operation uses the two internal CJC sensors. Due to package heating variation for varying channel assignments, the accuracy of the CJC is best when other channels are NOT assigned to high power modes such as mA outputs or internal fed mA inputs.

Caution

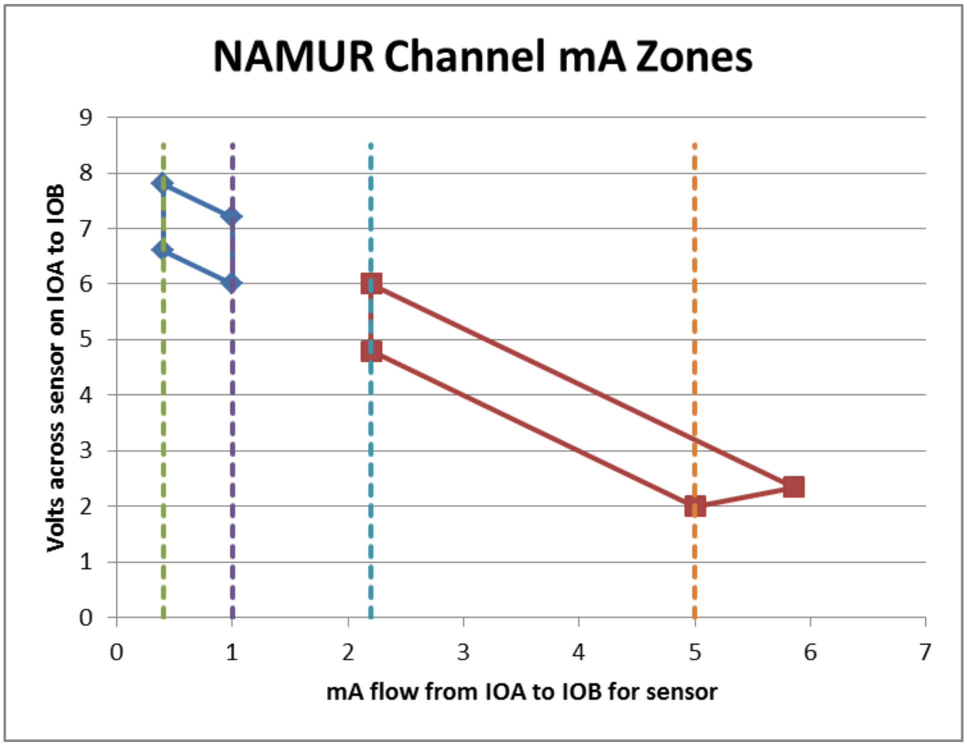
For best accuracy it is recommended that remote cold junctions be used due to heat dissipation from analog outputs and input modes. The remote cold junction value may be from either RTD channels on the same PUAA with variables passed to application code or from other devices read by the application code such as another PUAA/YUAA or PRTD.

17.11 Digital Inputs and Outputs

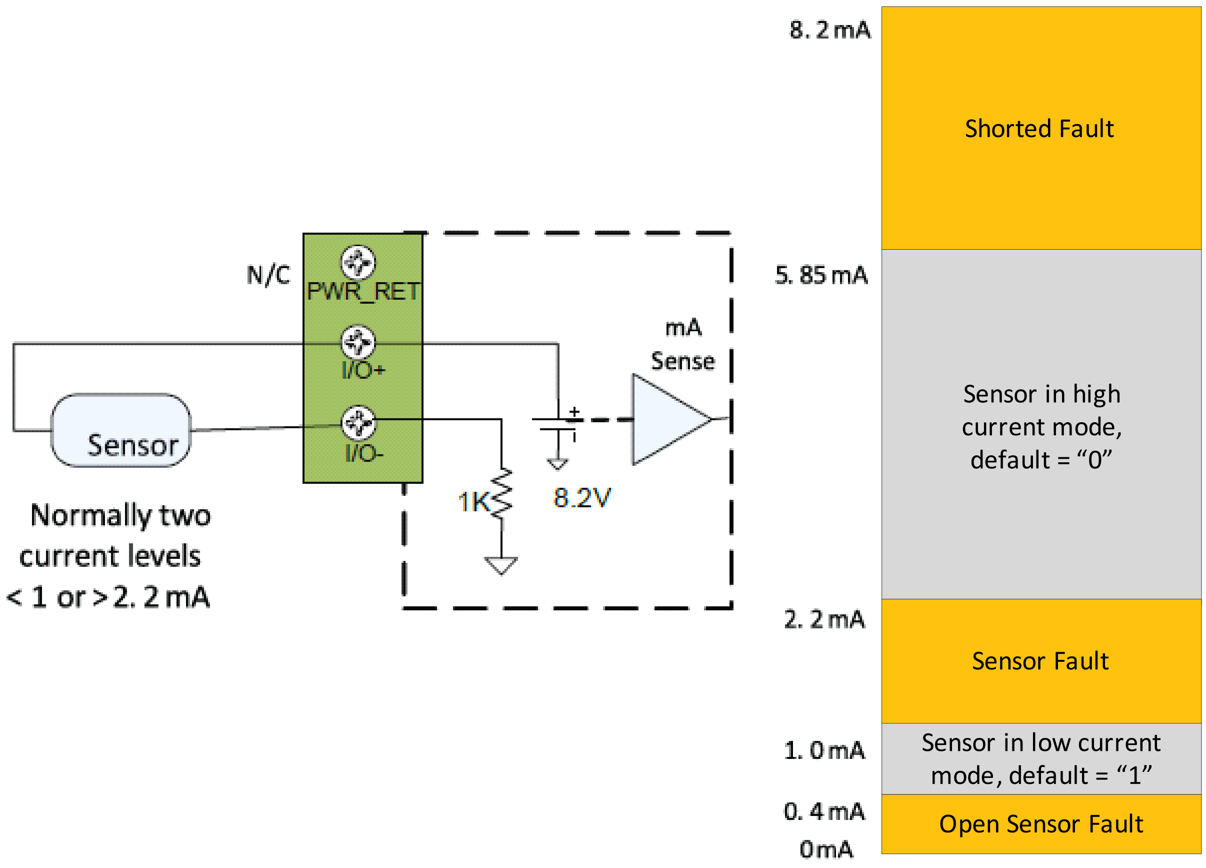
The PUAA/YUAA supports several types of digital (discrete) inputs and outputs, as enabled by configuration including: Digital input modes of NAMUR, Externally Wetted, Internally Wetted, and Digital Outputs through using mA outputs and interposing relays. Terminal voltages for the PUAA/YUAA must remain between 0 and 20 V for correct discrete input operation. To use inputs of higher than 20 V, such as for 24 V discrete inputs, the user must use a series resistor which would be part of the open wire detection. With the use of two resistors in parallel and series with the switch contact, external wetting voltages of up to 30 V are allowed.

17.11.1 NAMUR Style Sensor Inputs

The NAMUR sensor is connected between IO+ and IO-. NAMUR style implies that the sensor is designed in accordance with IEC60947-5-6 *Control circuit devices and switching elements –DC Interface for proximity sensors and switching amplifiers (NAMUR)*.



The NAMUR load 1K resistor is located on the IO- side of the connection. This prevents the use of a shared return wire for multiple sensors as done on RTD devices – each sensor shall be wired separately to its channel's two terminals.


N/C
PWR_RET
I/O+
I/O-
Sensor
Normally two current levels < 1 or > 2. 2 mA
1K
8.2V
mA Sense
8. 2 mA
Shorted Fault
5. 85 mA
Sensor in high current mode, default = “0”
2. 2 mA
Sensor Fault
1. 0 mA
Sensor in low current mode, default = “1”
0. 4 mA
Open Sensor Fault
0 mA

The decision for the sensor state is based on the current sensing on the high side with thresholds set at 0.4 mA, 1 mA, 2.2 mA, and 5.85 mA. Faults as well as normal sensor low and high current states are detected as follows:

- If the current is seen to be less than 0.4 mA then an open circuit is declared with an alarm.
- Between 0.4 and 1 mA, the sensor is in a low current state
- Between 1 and 2.2 mA, the sensor is declared as faulty
- Between 2.2 and 5.85 mA, the sensor is in a high current state
- Above 5.85 mA, the sensor is faulty with a short or IO+ is miss-wired to ground.

NAMUR sensors come in both normally open and normally closed styles. The default polarity is for the channel's contact state value to be set if current is between 0.4 and 1 mA.

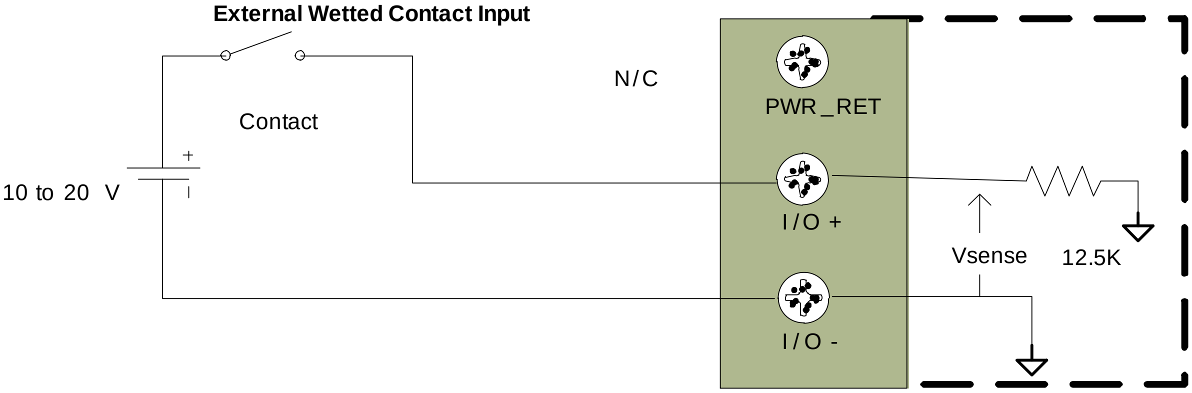
17.11.2 External Wetted Contact Inputs

The thresholds are based on the excitation voltage using optional external resistors, where the terminals are connected to an internal 12.5K load. There are three types of external wetted contact inputs, depending on source voltage and desired diagnostic support, as described in the following sections:

- External wetted contact inputs with 10–20 V field supply
- External wetted contact inputs with 20–30 V field supply requiring series resistance
- External wetted contact with line monitoring (open/short detection)

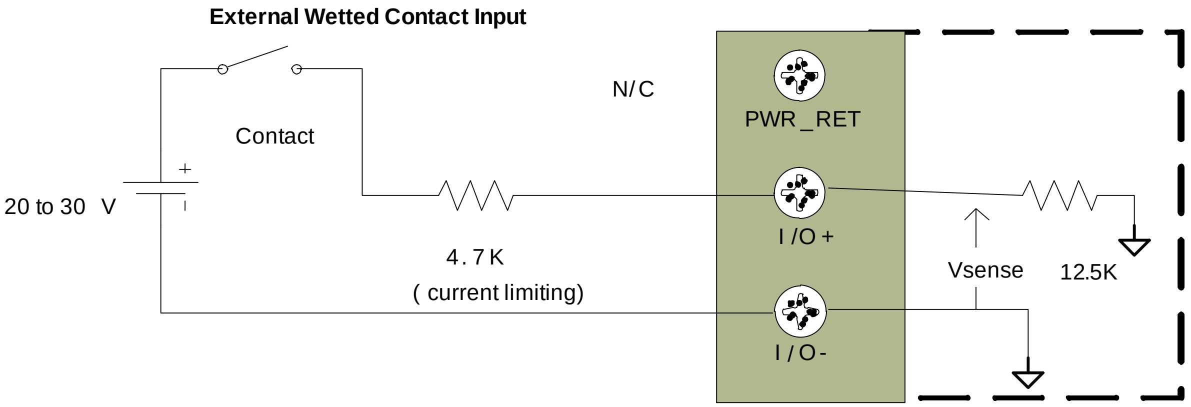
External Wetted Contact Inputs with 10 to 20 V Field Supply

For switches using a field supply of 20 V or lower, the simplest circuit to install is a switch with no resistors. There are no diagnostics for faults, just a decision at 50% of the specified field voltage for switch open or closed.



External Wetted Contact Inputs with 30 to 20 V Field Supply Requiring Series Resistance

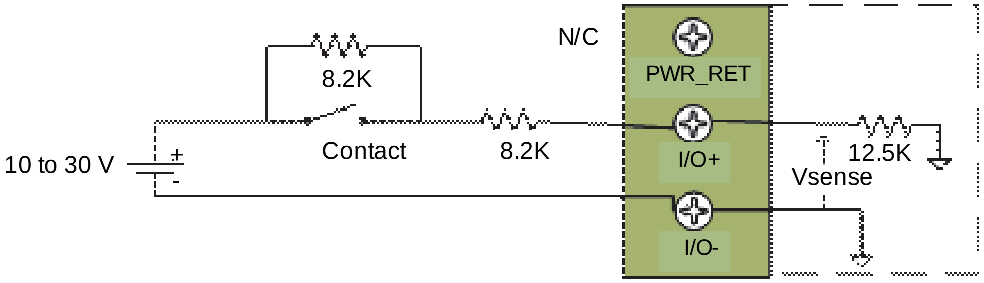
For switches using a field supply of higher than 20 V, external resistance is required to limit current to a safe value (where the current is due to the higher voltage back-feeding the internal 20 V circuity supply rail). It is highly recommended to use the line monitoring (open/short detection) scheme that uses two resistors and provides full diagnostic coverage for faults. Alternatively, a single series resistance of 4.7 KΩ ¼ watt can be used as shown in the following diagram solely to limit the current. To do this, the digit input parameter, **LineMonitoring**, on the input point should be set to *Disable* and the parameter **ExtWettingVoltage** should be set to *20 V* to force a simple 10 V decision threshold. However, these settings will only provide fault coverage of over-voltage due to a short from the I/O+ screw to field supply. If this fault occurs, the Point Unhealthy alarm (64–95) and/or the IO Point Input Saturation alarm (2754–2785) will be annunciated.



External Wetted Contact Inputs with Line Monitoring (Open/Short Detection)

For full diagnostic coverage, the user can enable line monitoring. When line monitoring is enabled, a different circuit is required with two resistors added to allow detection of a loop break (too little current) or short (too high a current). This adds two 8.2K ¼ watt resistors in parallel and series with the switch. Even with a 30 V field supply (above normal operation as an extreme), the resistors limit fault current preventing any impairment of the internal 24 V circuitry supply rail. An additional limit is for 20 V at the terminals where this is the maximum linear voltage sensed by the channel's A/D path.

External Wetted Contact with Line Monitoring (open/short detection) Wire Detection

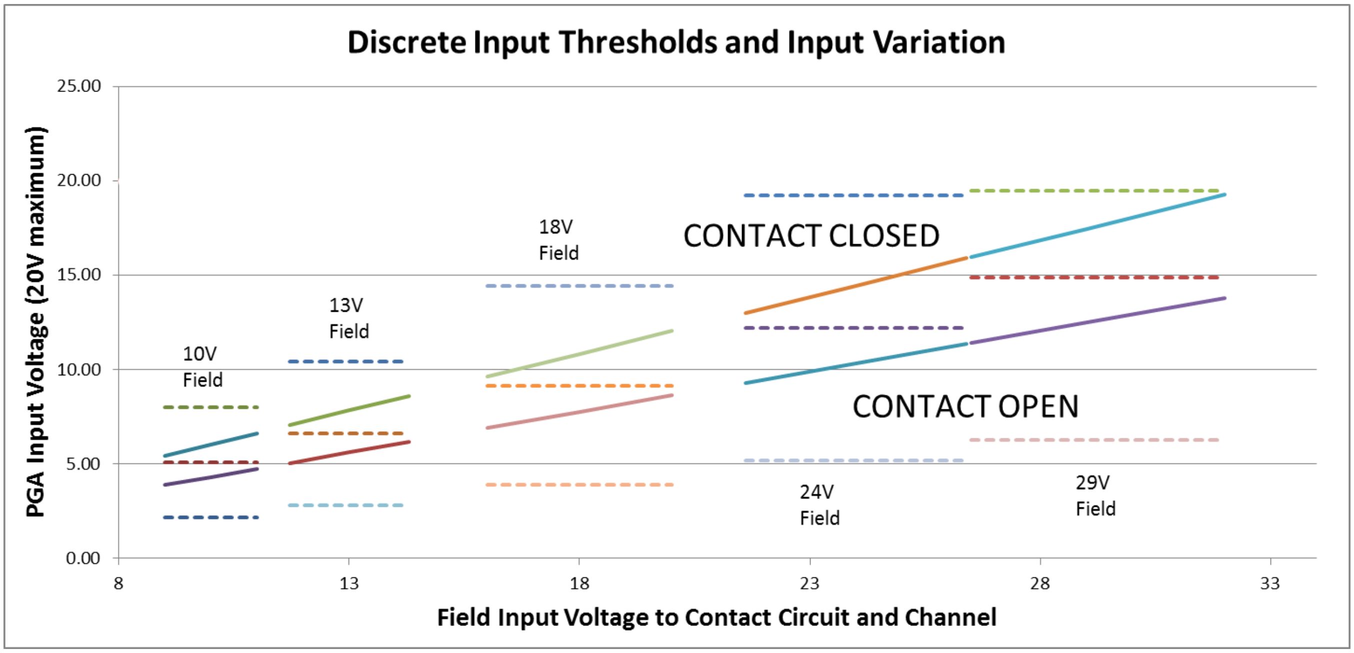


For detection of open and/or short conditions, there are additional thresholds imposed based on the field voltage entered in the ToolboxST application and the external resistors. The dual resistor circuit allows for detection of open loop and short to field supply.

The field supply voltage is entered in the ToolboxST application as the **ExtWettingVoltage** parameter. Using 24 V as an example, the thresholds are determined as follows:

- Open circuit at 50% of typical open contact value or 5.06 V (21% of 24 V)
- Contact open/closed decision at average of open and closed values or 12.42 V (51.75% of 24 V)
- Short threshold at average of closed and field level or 19.38 V (80.75% of 24 V) where this is within the 20 V limit of the signal path's linear range. Therefore, field supplies greater than 24 V have a short threshold that is not supported by the 20 V limit of the path's linear range.

Examples of various field settings for line monitoring (open/short detection) are shown in the following plot, where the thresholds for open/contact decision/short are shown in dashed lines for entries of 10, 13, 18, 24, and 29 V field supplies for contacts using two resistors allowing for +/- 10% field voltage variation. The lower solid lines are for the open contact voltage at the terminals, upper is for the closed contact voltage.



This mode of input uses low currents due to the load resistance. If the user's contact cannot support under 1 mA of current flow, use the PDIA/STCI combination with 2.5 or 10 mA current flow.

Attention

This mode of input cannot support a field supply higher than 30 V. If 48 V or 125 V operation is desired, use the appropriate PDIA/STCI combination supporting that supply level.

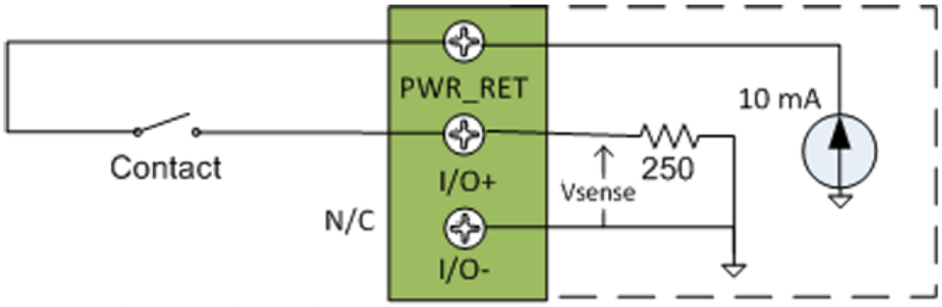
17.11.3 Internal Wetted Contact Inputs

The switch is connected between PWR_RET and IO+, where the channel's DAC output is passed via the external switch circuit to IO+ into the burden resistor. There are two types of external switch circuits supported as follows:

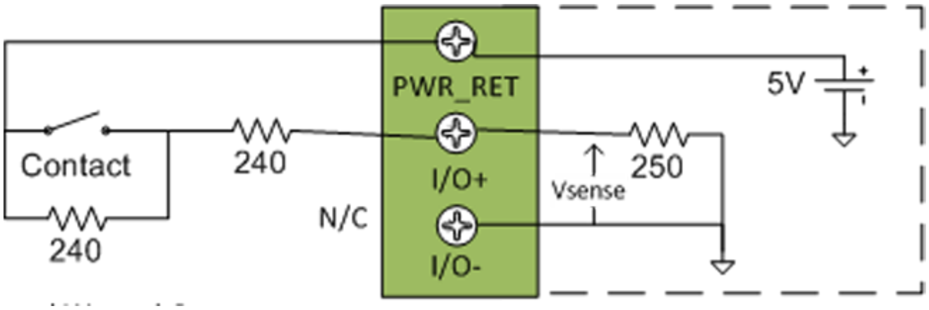
- Simple switch only
- Line monitoring (open/short detection) with the switch having two resistors in parallel and series

For the simple switch, the channel DAC is set for the contact current to flow from PWR_RET through the switch to IO+ into the 250 ohm burden resistor to ground. The decision on switch state is based on current above or below 50% the set value as measured on the burden resistor.

For line monitoring with detection of an open connection compared to an open switch, the DAC is set in voltage output mode by firmware. The user adds two resistors to limit the current in normal operation with both set at the same value based on the choice of desired current through the contact.



Internal Wetted Simple Contact



Internal Wetted Contact with Line Monitoring (Open/Short) Wire Detection

The variations on internal fed switches have the following contact voltages and currents.

Line Monitoring	Disabled	Enabled
Contact current	10 mA	10 mA
	Set by channel DAC in current output mode	Set by resistors, DAC is set to 5V
Resistor values (equal, 1% tolerance)	None	240 ohm ¼ watt
I/O+ for contact closed	2.5V	2.55
Open Contact voltage	Up to 24V	1.64
I/O+ for contact open	0	1.71
Threshold volts at IO+ for open loop	None	0.86
Threshold volts at IO+ for contact decision	1.25	2.13
Threshold volts at IO+ for short	None	3.78

17.11.4 Discrete Output Using mA Outputs and Interposing Relays

While no power output exists on the PUAA, the 24 mA output available on the mA output mode allows for driving interposing relays external to the PUAA. Examples of such devices available on the open market are as follows:

- Phoenix Contact PLC-RSC-24DC/21-296617, 6 Amps electromagnetic relay mounted on base terminal block
- Crydom DR24D06 280 VAC 6A solid state relay
- WAGO series 789 DIN mounted relay modules with various contacts, protection, and indicators available

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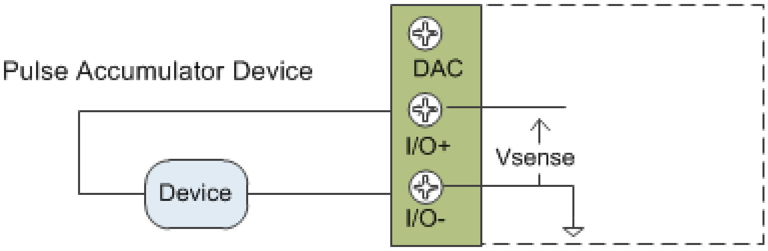
Note **1.** The user is responsible for validating the use of external devices within their application, these are only shown as examples of what a 24 mA output can control. The output will force either 22 V at lower currents or apply a constant current to the external relay coil, where the user should keep the current at a value matching the relay's operating current.

2. Testing is recommended to set the mA level appropriately. If set for 24 mA into a solid state driver or high resistance coil, the actual current could differ triggering unhealthy flags.

3. User must include a flyback diode across any relay coil being driven by PUAA in mA output mode. The cathode goes to IO+ and anode to IO-, suppressing the high voltage spike possible when the current is turned off to the relay coil.

17.12 Pulse Accumulator

The PUAA/YUAA support simple Pulse Accumulator inputs, which can count pulse edges on an input channel across a specified threshold voltage (user declares the threshold voltage with the **PAThreshold** parameter), up to a limited frequency. (Refer to the product specifications.) The connected device can be a dedicated externally-powered device that provides pulse inputs, or it can be an external power supply and contact, similar to the configuration supported for *externally-wetted contact inputs*.



Wiring Details for Pulse Accumulator Inputs

The PUAA/YUAA firmware counts the pulse detected in an unsigned 16-bit integer and delivers it to the controller as a REAL input. This REAL input will only ever contain an integer value (0-65535). When the counter value reaches 65535, the next pulse seen will cause it to change to 0. In order to detect this rollover and accumulate counts beyond this, the user must write application blockware to keep track of the total accumulation separately. Refer to the section *Pulse Accumulator Buffer Example* for an example of a simple way to do this.

The user can also use additional application blockware to determine the rate of the input. Refer to the example in the section *Frequency Calculation Example*.

17.13 Configuration

The ToolboxST configuration for PUAA/YUAA is different than most I/O packs. Since each point can process different types of I/O, there is a **Mode** selection in the **Configuration** tab that has to be set in the ToolboxST application Component Editor for each IOPoint (or left Unused if not used). The ToolboxST application does not enforce any limitations for available mA outputs with respect to the potential ambient environment inside the cabinet.

17.13.1 Parameters

The following are global configuration options for the PUAA/YUAA.

Name	Value { } = default	Description
TempUnits	°C {°F}	Temperature unit selection is use for RTDs, Thermocouples, and Cold Junction values
ColdJuncType	{Local} Remote	Cold Junction source for thermocouple inputs
AMS_Msgs_Only	{Disable} Enable	AMS Messages only - do not send control messages if enabled.
AMS_Mux_Scans_Permitted	{Disable} Enable	AMS mulitplexer scans for command 1 and 2 are allowed (command 3 always allowed)
Min_MA_Hart_Output	{4.0} 0 to 22.5	Minimum MA output for a Hart Enabled Device

17.13.2 Configuration (Modes)

Channel configuration can be done at any time, but requires a channel be taken from an Unused mode to an assigned mode (or from an assigned mode to Unused), but not directly from one mode to a different mode. This does not require a device reboot or impact adjacent channels.

The PUAA/YUAA allows changing individual point configuration though an Online Load (parameter download without rebooting) without affecting any other point, however changing from any one type of point to another first requires that the point be configured as Unused. The product will protect against an invalid transition and will fail the download and issue a diagnostic alarm to indicate the issue.

Name	Mode { } = default	Direction	Data Type	Description
IOPoint01	{Unused}			Universal I/O Point01
↓	CurrentInput	AnalogInput	REAL	↓
IOPoint16	VoltageInput	AnalogInput	REAL	Universal I/O Point16
	RTD	AnalogInput	REAL	
	CurrentOutput	AnalogOutput	REAL	
	Thermocouple	AnalogInput	REAL	
	PulseAccum	AnalogInput	REAL	
	DigitalInput	Input	BOOL	

Caution

To prevent damage to the SUAA, when the PWR_RET terminals are serving as a ground return for the channel, verify that the current to the ground is limited to 50 mA or less. If the ground path is capable of higher currents, then an external series resistor should be inserted in series with the terminal connection to serve as a current limit. As an example, if a 24 V circuit was capable of being incorrectly wired to the PWR_RET terminal, then a 510 ohm 2 watt resistor would be used in series as a protection device.

Caution

To prevent damage to field devices, verify wiring prior to configuring the I/O pack. Avoid any incorrectly wired channel that could act as an output driving back into an analog input device. The PUAA is capable of acting as an output or input channel under software command. The terminal blocks are in groups of 3 screws to allow for channels to be attached one at a time as part of wiring checks.

Current Inputs

CurrentInputs	Low_Input	Low_Value	High_Input	High_Value	InputFilter	ExternPwrEnab	Min_MA_ Input	Max_MA_Input
Descriptions	Input mA at Low Value	Low Input in Engineering Units	Input MA at High Value	High Input in Engineering Units	Filter Bandwidth in Hz	Enable External Power for 4-20ma inputs	Set the minimum mA for healthy input	Set the maximum mA for healthy input
Choices {defaults}	{4}	{0}	{20}	{100}	0.75hz 1.5hz 12hz 3hz 6hz {Unused}	Disable {Enable}	{3}	{22.5}

Low_Input, Low_Value, High_Input, High_Value settings are used by the PUAA/YUAA firmware to define the linear relationship between mA and customer-defined engineering units. The I/O Point value will be in Engineering units. Engineering units are specific to the field device being used.

Current Inputs (continued)

Hart_Enable ‡	Hart_CtrVars	Hart_ExStatus	Hart_MfgID	Hart_DevType	Hart_DevID
Enable Hart protocol on this channel	Number of control vars to read from Hart device Set to zero if not used.	Number of extended status bytes to read from Hart device Set to zero if not used.	Hart Field Device - Manufacture ID Note: For HART7 field devices, this is the upper byte of Expanded Device Type A diagnostic alarm is sent if the field device ID differs from this value and the value is non-zero. This value can be uploaded from the PUAA if the field device is connected. (Right-click on device name and select Update HART IDS)	Hart Field Device - Device Type Note: For HART7 field devices, this is lower byte of Expanded Device Type	Hart Field Device - Device ID
{Enable} Disable	{0} 0-5	{0} 0-26	{0} 0-255	{0} 0-255	{0} 0-116777215

Attention

‡ The first time all channel 1–8 are disabled, the I/O pack will require a reboot. The first time all channel 9–16 are disabled, the I/O pack will require a reboot.

The first time any channel 1–8 is enabled, the I/O pack will require a reboot. The first time any channel 9–16 is enabled, the I/O pack will require a reboot.

Current Outputs

Current Outputs	OutputState	Low_MA	Low_Value	High_MA	High_Value	Output_Value ‡
Description	State of the output when offline	Output low in mA	Low output value in engineering units	Output high in mA	High output in engineering units	This field is only available if **OutputState** = OutputValue
Choices {defaults}	HoldLastValue OutputValue {PwrDownMode}	{4}	{0}	{20}	{100}	{0}

‡ Scroll all the way to the right to find this value because the field does not appear directly right of the High_Value as expected.

If the I/O pack loses communication with the controller, **OutputState** determines how it drives the outputs as follows:

- PwrDownMode: drive outputs to zero current
- HoldLastVal: hold the last value received from the controller
- Output_Value: go to the configured output value set by the **Output_Value** (units are Engineering Units, not mA)

Low_MA, Low_Value, High_MA, High_Value settings are used by the I/O pack firmware to define the linear relationship between customer-defined engineering units and output mA. The I/O Point value will be in Engineering units, and the firmware will convert it to mA. Engineering units are specific to the field device being used.

Current Outputs (continued)

Hart_Enable ‡	Hart_CtrVars	Hart_ExStatus	Hart_MfgID	Hart_DevType	Hart_DevID
Enable Hart protocol on this channel	Number of control vars to read from Hart device Set to zero if not used.	Number of extended status bytes to read from Hart device Set to zero if not used.	Hart Field Device - Manufacture ID Note: For HART7 field devices, this is the upper byte of Expanded Device Type A diagnostic alarm is sent if the field device ID differs from this value and the value is non-zero. This value can be uploaded from the PUAA if the field device is connected. (Right-click on device name and select Update HART IDS)	Hart Field Device - Device Type Note: For HART7 field devices, this is lower byte of Expanded Device Type	Hart Field Device - Device ID
{Disable} Enable	{0} 0-5	{0} 0-26	{0} 0-255	{0} 0-255	{0} 0-116777215

Attention

‡ The first time any channel 1–8 is enabled, the I/O pack will require a reboot. The first time any channel 9–16 is enabled, the I/O pack will require a reboot.

The first time all channel 1–8 are disabled, the I/O pack will require a reboot. The first time all channel 9–16 are disabled, the I/O pack will require a reboot.

17.13.3 Voltage Inputs

Voltage Inputs	InputType	Low_Input	Low_Value	High_Input	High_Value	InputFilter
Description	Type of Analog Input	Input Volts at Low Value	Low Input in Engineering Units	Input Volts at High Value	High Input in Engineering Units	Filter Bandwidth in Hz
Choices {defaults}	+/-10volt {+/-5volt}	{-5}	{0}	{5}	{100}	0.75, 1.5, 3, 6, 12, {Unused}

Low_Input, Low_Value, High_Input, High_Value settings are used by the I/O pack firmware to define the linear relationship between Volts and customer-defined engineering units. The I/O Point value will be in Engineering units. Engineering units are specific to the field device being used.

17.13.4 RTDs

RTDType	Compatible Type	Notes
MINCO_NA	N 120	RTDType selects the type of RTD device connected to the input. The Ohms type returns a value of resistance, with the TempUnits parameter ignored. The temperature units parameter, TempUnits, can be either Fahrenheit or Celsius, and is set from the Parameters tab.
MINCO_PA	PT100 PURE	
MINCO_PB	PT100 USIND	
{MINCO_PD}	PT100 DIN	
MINCO_PIA		
MINCO_PK	PT 200	
MINCO_PN		
MINCO_CA	CU10	
Ohms		
PT100_SAMA	SAMA 100	

17.13.5 Thermocouples

ThermCplType	ReportOpenTC	Notes
B E J K {mV} N R S T	{Fail_Cold} Fail_Hot	ThermCplType selects the type of TC device connected to the input. The mV type shall only return a value of millivolts, the Units parameter shall be ignored for this type, and no cold junction compensation shall be performed. ReportOpenTC is a Fail_Hot/Fail_Cold configuration to control the reported TC value when an open circuit occurs. On open circuit detection the PUAA will report the calculated value at -40 mV (Open TC Threshold) when Fail_Cold in enabled, and will report 3632 ºF (2000 ºC) when Fail_Hot is enabled. The temperature units parameter, TempUnits, can be either Fahrenheit or Celsius, and is set from the Parameters tab.

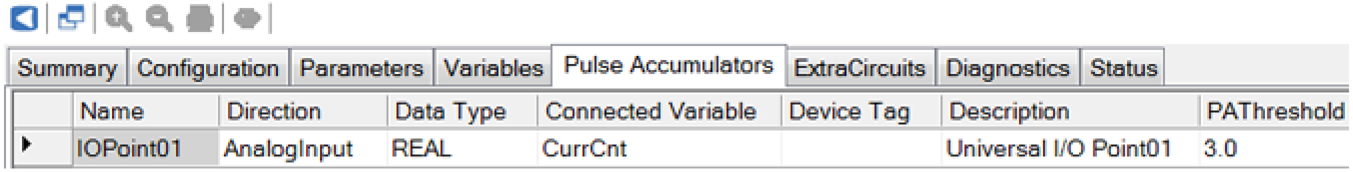
17.13.6 Digital Inputs

Digital Inputs	SignalInvert	SeqOfEvents	LineMonitoring	InputMode	SignalFilter	ExtWettingVoltage
Description	Inversion makes signal true if contact is open	Record contact transitions in sequence of events	Open/shorted input detection Does not apply when InputMode is set to NAMUR, as line monitoring is inherent in NAMUR operation.	Internal/ExternalWetting, NAMUR Sensor	Contact input filter in milliseconds	External wetting voltage Only applicable if InputMode is set to External Wetting
Choices {defaults}	{normal} Invert	{Disable} Enable	{Disable} Enable	{Internal} External NAMUR	{Unfiltered} 10 ms 20 ms 50 ms 100 ms	{24.0}

17.13.7 Pulse Accumulators

Pulse Accumulators	**PAThreshold**
Description	Pulse threshold voltage
Choices {defaults}	{3.0}

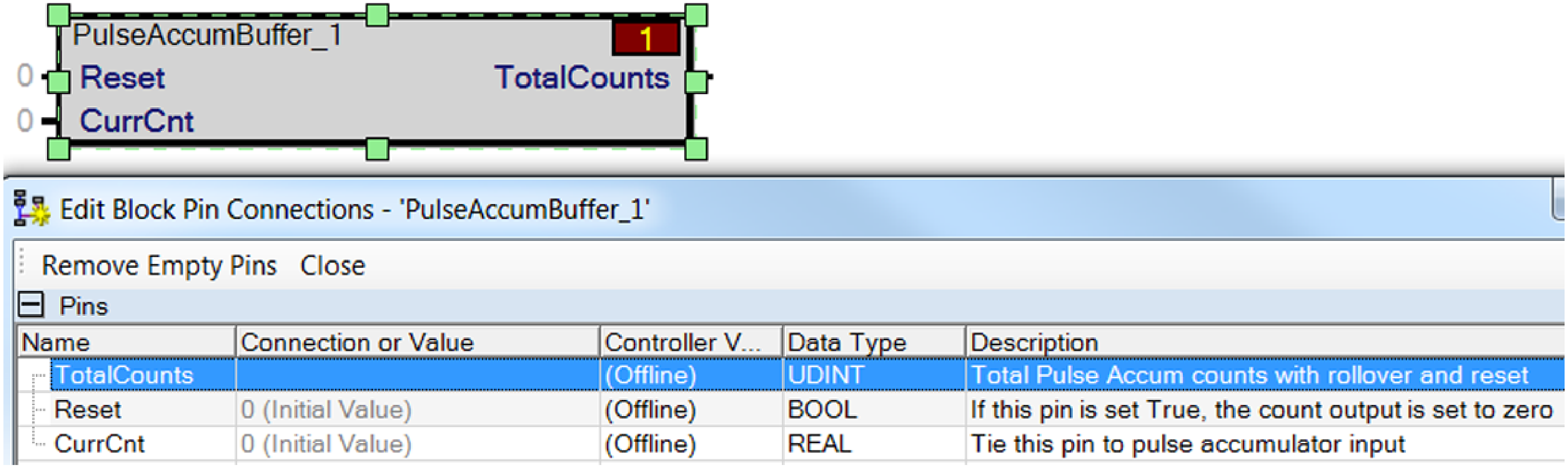
This example configuration with connected variable is used in the following two example applications. It is recommended that the user set a threshold midway between the expected low and high input levels.



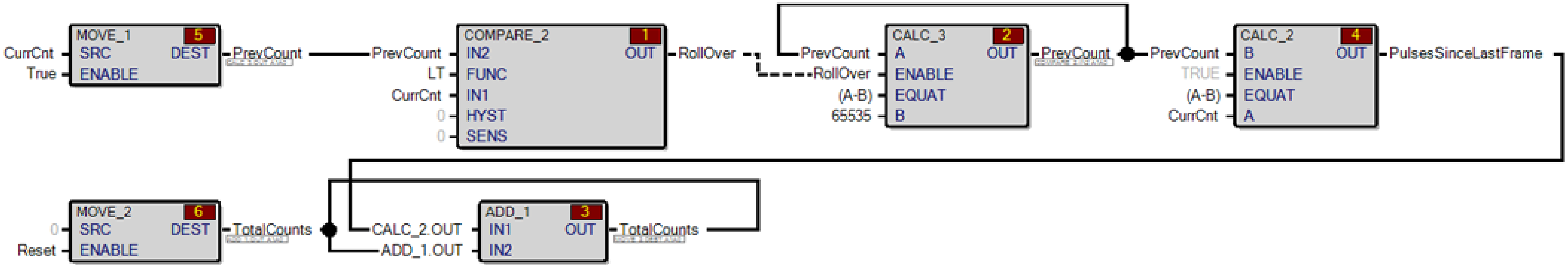
Name	Direction	Data Type	Connected Variable	Device Tag	Description	PAThreshold
IOPoint01	AnalogInput	REAL	CurrCnt		Universal I/O Point01	3.0

17.13.8 Pulse Accumulator Buffer Example

This user block example connects to PUAA/YUAA pulse accumulator inputs to provide a Total Counts output that is a 32-bit integer. It handles PUAA 16-bit rollovers and implements a user reset of total counts to zero. The 16-bit accumulator resets to zero when the I/O pack reboots or the channel's mode is changed. The counter increments when the input voltage transitions above the **PAThreshold** setting. The next pulse after accumulator is at 65535 will result in the accumulator rolling over to zero and continuing to count from there on following pulses.

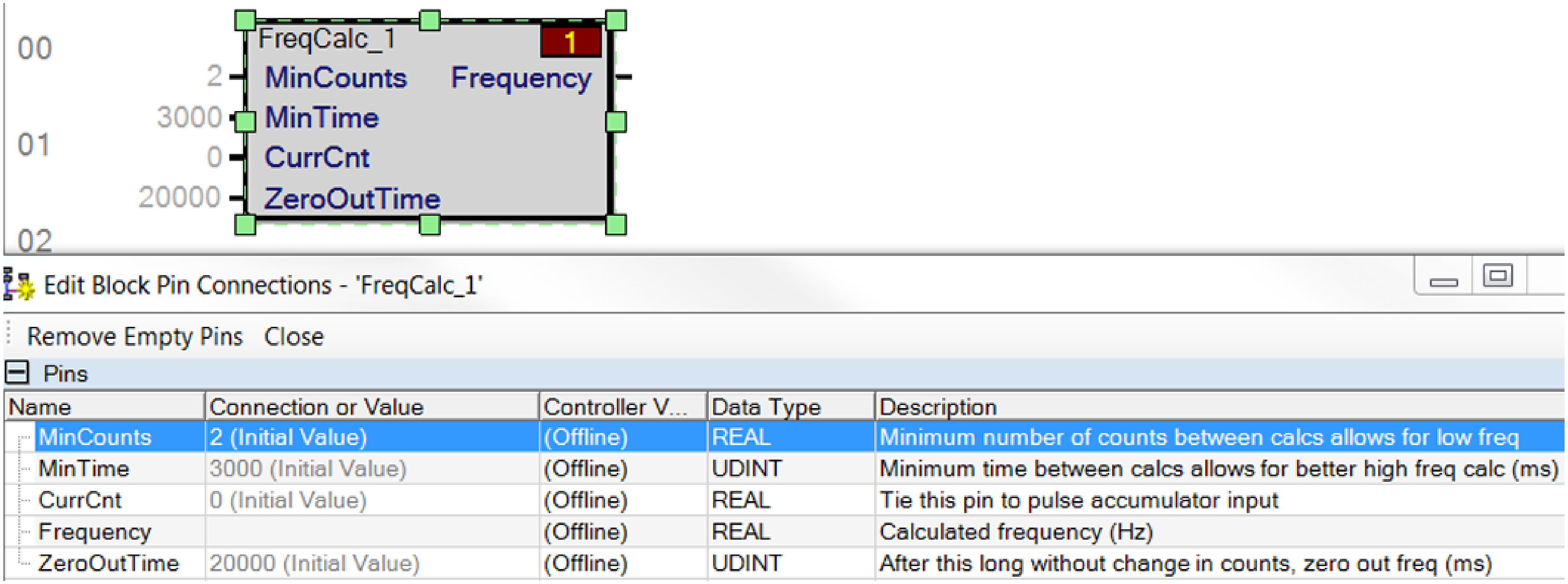


Name	Connection or Value	Controller V...	Data Type	Description
TotalCounts		(Offline)	UDINT	Total Pulse Accum counts with rollover and reset
Reset	0 (Initial Value)	(Offline)	BOOL	If this pin is set True, the count output is set to zero
CurrCnt	0 (Initial Value)	(Offline)	REAL	Tie this pin to pulse accumulator input

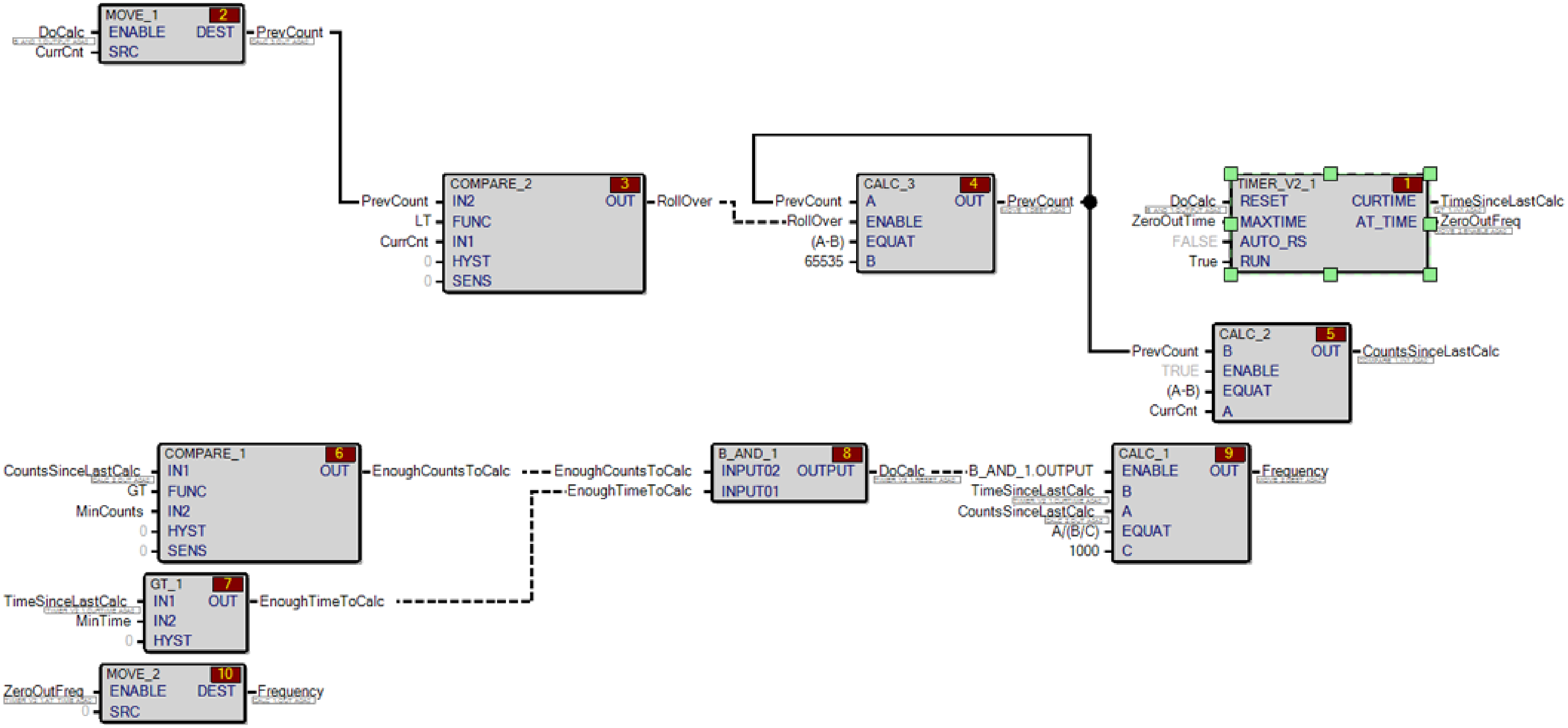


17.13.9 Frequency Calculation Example

This user block example connects to PUAA/YUAA pulse accumulator inputs to provide a frequency output. Rollover is handled. Three configuration values are offered.



Name	Connection or Value	Controller V...	Data Type	Description
MinCounts	2 (Initial Value)	(Offline)	REAL	Minimum number of counts between calcs allows for low freq
MinTime	3000 (Initial Value)	(Offline)	UDINT	Minimum time between calcs allows for better high freq calc (ms)
CurrCnt	0 (Initial Value)	(Offline)	REAL	Tie this pin to pulse accumulator input
Frequency		(Offline)	REAL	Calculated frequency (Hz)
ZeroOutTime	20000 (Initial Value)	(Offline)	UDINT	After this long without change in counts, zero out freq (ms)


MOVE_1
2
DoCalc
ENABLE
DEST
PrevCount
CurrCnt
SRC
COMPARE_2
3
PrevCount
IN2
OUT
RollOver
LT
FUNC
CurrCnt
IN1
0
HYST
0
SENS
CALC_3
4
PrevCount
A
OUT
PrevCount
RollOver
ENABLE
(A-B)
EQUAT
65535
B
TIMER_V2_1
1
DoCalc
RESET
CURTIME
TimeSinceLastCalc
ZeroOutTime
MAXTIME
AT_TIME
ZeroOutFreq
FALSE
AUTO_RS
True
RUN
CALC_2
5
PrevCount
B
OUT
CountsSinceLastCalc
TRUE
ENABLE
(A-B)
EQUAT
CurrCnt
A
COMPARE_1
6
CountsSinceLastCalc
IN1
OUT
EnoughCountsToCalc
GT
FUNC
MinCounts
IN2
0
HYST
0
SENS
B_AND_1
8
EnoughCountsToCalc
INPUT02
OUTPUT
DoCalc
EnoughTimeToCalc
INPUT01
CALC_1
9
B_AND_1.OUTPUT
ENABLE
OUT
Frequency
TimeSinceLastCalc
B
CountsSinceLastCalc
A
A/(B/C)
EQUAT
1000
C
GT_1
7
TimeSinceLastCalc
IN1
OUT
EnoughTimeToCalc
MinTime
IN2
0
HYST
MOVE_2
10
ZeroOutFreq
ENABLE
DEST
Frequency
0
SRC

17.13.10 Variables

Name	Direction	Data Type	Description
L3DIAG_XXXX_R	Input	BOOL	I/O Diagnostic Indication, where XXXX is either PUAA or YUAA
LINK_OK_XXXX_R	Input	BOOL	I/O Link Okay Indication, where XXXX is either PUAA or YUAA
ATTN_XXXX_R	Input	BOOL	I/O Attention Indication, where XXXX is either PUAA or YUAA
OutxxMA	AnalogInput	REAL	Current Output Feedback in mA, where xx = the channel number
PS18V_XXXX_R	Input	BOOL	I/O 18V Power Supply Indication, where XXXX is either PUAA or YUAA
PS28V_XXXX_R	Input	BOOL	I/O 28V Power Supply Indication, where XXXX is either PUAA or YUAA
IOPackTmpr_R	AnalogInput	REAL	IO Pack Temperature (deg F)
CJBackup	AnalogOutput	REAL	Backup Cold Junction Temperature (Deg F/C based on Cold Junction config)
CJRemote	AnalogOutput	REAL	Remote Cold Junction Temperature. Used when ColdJuncType is set to Remote (Deg F/C based on Cold Junction config)
ColdJunc01	AnalogInput	REAL	Cold Junction sensor #1
ColdJunc02	AnalogInput	REAL	Cold Junction sensor #2
AckHartCfgChange	Output	BOOL	Toggle to True to reset Hart configuration change alarms on rising edge
HartMux_Health	Input	BOOL	Hart Mux Health

17.13.11 HART Signal Definitions

Signal	Type	Description
Hxx_CommCnt	Integer	Number of times the CommStat signal was not zero after a HART message
Hxx_CommStat	Bit encoded integer	Most Recent Slave-Reported Communication Status Error
		Bit 1 – RX buffer overflow
		Bit 3 – Checksum error
		Bit 4 – Framing error Bit 5 – Overrun error Bit 6 – Parity error
Hxx_DevCnt	Integer	Number of times the DevStat signal was not zero after a HART message.
Hxx_DevStat	Bit encoded integer	Most Recent Device Response Codes: bits 0-7
		Bit 0 – Primary variable out of limits Bit 1 – Non primary var out of limits Bit 2 – Analog output saturated
		Bit 3 – Analog output current fixed
		Bit 4 – More status available (ExStat) Bit 5 – Cold start
		Bit 6 – Configuration changed Bit 7 – Field device malfunction Command response byte: bits 8-15
		2: Invalid selection requested
		3: Passed parameter too large
		4: Passed parameter too small
		5: Too few bytes received
		6: Device specific device error
		7: In write protect mode
		8-15: Device specific
		16: Access restricted
		32: Device is busy
		64: Command not implemented
Hxx_DevRev	Integer	Field Device - Device revision code as read from the device.

Signal	Type	Description
Hxx_HwSwRev	Integer	Byte 0 - Field device software revision Byte 1 - Field device hardware revision
Hxx_mA †	Float	Field Parm 1 – current reading of the primary signal
Hxx_PV †	Float	Field Device Specific Control Parm 2 - Primary field device value
Hxx_SV †	Float	Field Device Specific Control Parm 3 - Secondary value
Hxx_TV †	Float	Field Device Specific Control Parm 4 -Third value
Hxx_FV †	Float	Field Device Specific Control Parm 5 -Fourth value
† To view these variables, the Hart_CtrlVars parameter must have a value greater than zero.		

17.13.12 HART Extended Status

The extended status bits are device-specific, and can be interrogated by using an AMS system. In general, the status bits are grouped as follows:

- Bytes 0-5: Device specific status
- Byte 6: Extended Device Status
- Byte 7: Device Operating Mode
- Byte 8: Standardize Status 0
- Byte 9: Standardize Status 1
- Byte 10: Analog Channel Saturated
- Byte 11: Standardize Status 2
- Byte 12: Standardize Status 3
- Byte 13: Analog Channel Fixed
- Bytes 14-26: Device-specific

Each field device supports a specific number of control parameters and extended status bits. Refer to the Field Device documentation to determine the correct number and configure the ToolboxST application accordingly. A diagnostic alarm message will be generated if the Field Device and ToolboxST configuration do not match.

Hxx_ExStat_1	Bit Encoded	Extended Status Bytes 1-4
Hxx_ExStat_2	Bit Encoded	Extended Status Bytes 5-8
Hxx_ExStat_3	Bit Encoded	Extended Status Bytes 9-12
Hxx_ExStat_4	Bit Encoded	Extended Status Bytes 13-16
Hxx_ExStat_5	Bit Encoded	Extended Status Bytes 17-20
Hxx_ExStat_6	Bit Encoded	Extended Status Bytes 21-24
Hxx_ExStat_7	Bit Encoded	Extended Status Bytes 25-26

17.14 Diagnostics

17.14.1 I/O Point Health Status

Each I/O point on the module has an associated health status. The health of each point is continuously monitored and marked unhealthy for the following conditions (and a per-point diagnostic alarm is generated):

- For mA inputs
  - if the user-defined Min/Max mA limits are exceeded.
  - if the currents through the burden resistor exceed 30 mA
- For voltage inputs, if the hardware input limits are exceeded
- For RTD inputs
  - if the input value exceeds the maximum or is below the minimum temperature range of the selected device
  - if the expected data received is missing or invalid.
  - if hardware limits are exceeded
- For each TC input
  - if the input value exceeds the maximum or is below the minimum temperature range of the selected device
  - if the temperature value is calculated using an extrapolated range beyond the device temperature curve table.
  - if the input voltage exceeds the HW input limits of -40 mV to 114 mV.
  - if the input is open, no sensor connected (burnout detection).
- For mA outputs
  - if commanded current exceeds the hardware limits
  - if current output feedback (from sense resistor) does not match the commanded current
- For Digital Inputs
  - if input voltage exceeds HW max or min limits
  - if an open wire is detected when using line monitoring
  - if a short is detected when using line monitoring
  - if sensor fault is detected when using a NAMUR input
- For Pulse Accumulator Inputs
  - if input voltage exceeds HW input limits of -11 V to 21 V

17.14.2 I/O Status LEDs

The following I/O status LEDs are driven by the I/O pack firmware. For common BPPC processor LEDs, refer to GEH-6721_ Vol_II, the section *Common I/O Module Functionality.*

Channel Number	Color	Status
1–16	Green	assigned/healthy
	Red	unhealthy or point initialization in progress
	Not Lit	channel not used

Note Refer to the illustration of the I/O pack faceplate in the section *Mark VIe PUAA Universal I/O Pack* or *Mark VIeS YUAA Universal I/O Pack* for the I/O status LEDs.

17.14.3 Other Diagnostic Monitors

- Channel configuration at startup and at online load time is verified and a diagnostic is issued when an error occurs.
- Cold Junction sensors are monitored for healthy range and are marked unhealthy and a diagnostic alarm is issued when they are out of range.
- Factory calibration data is validated and a diagnostic alarm is issued if the data is missing or corrupted (indicating product is not running with applied factory calibration).

17.15 Replacement

Attention

Replacement of the terminal board requires full reconfiguration of the changed component using the ToolboxST application. For this reason, it is generally preferable to replace only the I/O pack unless the terminal board is known to be the point of failure.

17.15.1 Replacing a PUAA/YUAA I/O Pack with another PUAA/YUAA I/O Pack

PUAA/YUAA I/O packs are hot-swappable, where a pull and replace may occur with power supplied to the power connector. It is online repairable, with no IONet disturbance due to removal or insertion of the I/O pack. It also supports auto-reconfiguration for I/O pack replacement (not terminal board replacement).

➢ **To replace a PUAA/YUAA I/O pack**

1. Follow all applicable site safety procedures and the Cautions and Warnings published in GEH-6721_Vol_II, the chapter *Maintenance and Replacement*.
2. Verify that the replacement I/O pack is compatible with one being replaced by comparing the model numbers.
3. Remove the power connector from the I/O pack.
4. Unplug the IONet cable(s) from the I/O pack, and mark the positions of the removed cables (if using dual IONets).
5. Remove the two mounting screws that hold the I/O pack onto the terminal board.
6. Unplug the I/O pack.
7. Plug in the replacement I/O pack. Make sure the I/O pack connector is fully seated on all sides, then properly tighten the mounting screws to 2.15 nm (19 in lb) torque to firmly hold the new I/O pack onto the terminal board.
8. Plug the Ethernet and power cables back into the I/O pack.
9. If the Auto-Reconfiguration feature is enabled, the controller detects the I/O module running with a different configuration, and a reconfiguration file is automatically downloaded from the controller to the new I/O module.

17.15.2 Replacing the SUAA Terminal Board

➢ **To replace the SUAA terminal board**

1. Follow all applicable site safety procedures and the Cautions and Warnings published in GEH-6721_Vol_II, the chapter *Maintenance and Replacement*.
2. Perform LOTO procedures and isolate the power sources.
3. Check the voltage on each terminal to ensure that there is no voltage present.
4. Gently pry the segment of the terminal block containing the field wiring away from the part attached to the terminal board, leaving the wiring in place. If necessary, tie the block to the side out of the way.
5. If panel mounted, remove the mounting screws and terminal board.
6. If DIN-rail mounted, refer to the section *Mounting* for DIN-rail installation and removal instructions.
7. Remove the I/O pack from the old terminal board (if the I/O pack is in good working order).
8. Gently pry the segment of the new terminal block that would contain the field wiring away from the part attached to the new terminal board. Then, slide the segment containing the field wiring from the old board into the new terminal block. Ensure that the numbers on the segment with the field wires match the numbers on the terminal block. Press together firmly. Ensure that all field wiring is secure.
9. Install the new SUAA onto the mounting base or DIN-rrail.
10. Install the I/O pack onto the terminal board (if not present).

17.15.3 Replacing an Existing Mark VIe I/O Module with a PUAA I/O Module or an Existing Mark VIeS I/O Module with a YUAA I/O Module

Depending on application requirements and field devices used, some existing Mark VIe and Mark VIeS I/O modules can be replaced with the PUAA/YUAA. Refer to the appropriate retrofit table in the section *Wiring and Configuration* for details on supported applications, and then the instructions for field wiring and configuration provided in this manual. Contact your nearest GE Sales or Service office, or an authorized GE Sales Representative for more information.

17.16 PUAA Diagnostic Alarms

The following diagnostic alarms are specific to the PUAA universal analog functions. Common Mark VIe I/O module processor diagnostics are listed separately.

32-63

Description Failed loading configuration for point [ ]

Possible Cause

- Attempted to change an already configured point to a different point type without making the point unused first.
- Hardware communication failure

Solution

- Set the PointType for the specified point to Unused and download before changing to desired PointType.
- Re-download configuration

64-95

Description Point [ ] unhealthy

Possible Cause Use the following table to identify the possible cause for this unhealthy point, based on the configured Mode of the channel and field device.

Solution Use the following table to identify a solution for this unhealthy point, based on the configured Mode of the channel and field device.

Point Unhealthy Troubleshooting

Mode	Possible Cause	Solution
CurrentInput	The excitation to transducer is wrong or missing.	Check the field wiring and connections to indicated analog input channel. Check the field device for failure. Check the PUAA power from terminal board screw.
CurrentInput	The transducer is defective.	Replace the transducer.
CurrentInput	There is an open or short-circuit on input.	Check the field wiring and connections to indicated analog input channel.
CurrentInput	The analog current input is beyond the specified range 4-20 mA	Check the field wiring and connections to indicated analog input channel. Check the field device for failure. If incorrectly configured, from the ToobloxST Component Editor, modify the specified range.
Current Input	The burden resistor protection has been activated, greater than 30 mA has been detected	Check the field wiring and connections to indicated analog input channel.
Current Input	Hardware failure in the I/O Module or Terminal Board.	Replace the I/O Module. Replace the Terminal Board.
VoltageInput	The excitation to transducer is wrong or missing.	Check the field wiring and connections to indicated analog input channel. Check the field device for failure. Check the PUAA power from terminal board screw is correct.
VoltageInput	The transducer is defective.	Replace the transducer.
VoltageInput	There is an open or short-circuit on input.	Check the field wiring and connections to indicated analog input channel.
VoltageInput	The analog voltage input is beyond the specified range.	Check the field wiring and connections to indicated analog input channel. Check the field device for failure. If incorrectly configured, from the ToolboxST Component Editor, modify the specified range.

Point Unhealthy Troubleshooting (continued)

Mode	Possible Cause	Solution
CurrentOutput	The commanded output is beyond the range of the output.	Verify that the commanded output is within the range of the output.
CurrentOutput	There is a field wiring problem	Check the field wiring and device.
CurrentOutput	There is an open loop or too much resistance in the loop.	Confirm the correct I/O pack 28 V input power. Check the field wiring and device.
CurrentOutput	The I/O pack has failed.	Replace the I/O pack.
CurrentOutput	The terminal board has failed.	Replace the terminal board.
RTD	RTD wiring/cabling open or high impedance.	Check the field wiring and connections to indicated RTD input channel.
RTD	Open on connections to the terminal board.	Check the field wiring and field device.
RTD	RTD device failed.	Replace the RTD device.
RTD	PUAA module internal hardware problem.	Replace the I/O pack.
RTD	Current source on PUAA for RTD faulty or measurement device failed.	Replace the I/O pack. Replace the field device.
RTD	Wrong type of RTD configured or selected by default.	From the ToolboxST application, modify the PUAA I/O pack to correct the configuration.
RTD	High-resistance values created by high voltage and/or low current.	Check the field wiring and field device.
Thermocouple	Thermocouple millivolt input exceeds the limits of the PUAA hardware.	Check field wiring, including shields. Measure incoming mV signal and verify that it is within the specified thermocouple range. Check installation of the I/O pack on the terminal board. This problem is usually not an I/O pack or terminal board failure if other thermocouples are working correctly. Verify that the installed type of thermocouple device matches the configuration found in the ToolboxST application. Replace the field device.
Thermocouple	Cold junction input to the analog-to-digital converter exceeded the limits of the converter. If a cold junctions fails, the CJ_Backup value is used.	Check installation of the I/O pack on the terminal board. If local CJ, replace the terminal board.
Thermocouple	Thermocouple mV input exceeded range of linearization (lookup) table for this TC type. Refer to documentation for specified thermocouple ranges.	Check field wiring, including shields. Measure incoming mV signal and verify that it is within the specified thermocouple range. Check installation of the I/O pack on the terminal board. Note: The problem is usually not an I/O pack or terminal board failure if other thermocouples are working correctly. Verify that the installed type of thermocouple device matches the configuration found in the ToolboxST application. Replace the field device.
Thermocouple	Thermocouple configured as wrong type.	Verify that the installed type of thermocouple device matches the configuration found in the ToolboxST application.
Thermocouple	Board detected a thermocouple open	Check field wiring, including shields. Replace the field device.
Thermocouple	Stray voltage or noise caused the input to exceed its range.	Check field wiring, including shields. Replace the field device.

Point Unhealthy Troubleshooting (continued)

Digital Input	Internal Wetted Input exceeded range of operation	Check field wiring. Measure incoming mA signal and verify that it is 10 mA.
Digital Input	External Wetted Input exceeded range of operation	Check field wiring. Measure voltage across digital inputs terminal points and verify it is between -1 V and 21 V.
Digital Input	NAMUR input exceeded range of operation	Check field wiring. Verify mA signal through field device does not exceed 9 mA. Replace the field device.
Digital Input	Digital Input mode configured as wrong type	Verify field wiring and field device matches the configured Input Mode found in the ToolboxST application.
Digital Input	Open circuit detected on digital input signal	Check the wiring between the terminal board and the device. Verify that the recommended line monitoring resistors are being used.
Digital Input	Short detected on digital input signal	Check the wiring between the terminal board and the device. Verify that the recommended line monitoring resistors are being used.
Pulse Accumulator	Pulse input voltage exceeds the limits of the PUAA hardware	Check field wiring. Measure incoming signal and verify that it is within -11 V and 21 V. Replace the field device.

96

Description Invalid calibration settings

Possible Cause

- Calibration file not detected
- Calibration file corrupted
- Calibration constants invalid
- Hardware Failure

Solution Replace the I/O pack.

97-98

Description Cold Junction temp [ ] exceeds range limit ([ ])

Possible Cause Cold junction input to the analog-to-digital converter exceeded the limits of the converter. If a cold junctions fails, the **CJ_Backup** value is used.

Solution

- Check the mounting of the I/O pack on the terminal board.
- Replace the terminal board.
- Replace the I/O pack.

99-130

Description IOPoint [ ] - Current output commanded current feedback error

Possible Cause

- The measured current feedback does not match the commanded current.
- There is an open circuit on an output.
- Output impedance is too high (max allowed 800 Ohms).

Solution

- Check the field wiring and device.
- Verify that the commanded output is within output range.
- Replace the I/O pack.

131-162

Description IOPoint [ ] - Open field wire detected

Possible Cause An open circuit has been detected at the terminal board based on the sensor type.

Solution

- Digital Input:
  - Check the wiring between the terminal board and the device.
  - Verify that the recommended line monitoring resistors are being used (refer to the PUAA user documentation).
- Thermocouple Input: verify the wiring of the thermocouple at the inputs.

163-194

Description IOPoint [ ] - Thermocouple input millivolt exceeds hardware limit ([ ] mV)

Possible Cause

- Thermocouple millivolt input exceeds the hardware limit
- An open thermocouple was detected.

Solution This is usually not a I/O pack or terminal board failure if other thermocouples are working correctly.

- Check the field wiring, including shields.
- Check the installation of the I/O pack on the terminal board.
- Replace the I/O pack.

195-226

Description IOPoint [ ] - Thermocouple value beyond range of configured TC type ([ ] deg)

Possible Cause

- Thermocouple mV input exceeded range of linearization (lookup) table for this TC type. Refer to documentation for specified thermocouple ranges.
- Thermocouple configured as wrong type
- Stray voltage or noise caused the input to exceed its range.

Solution

- Check the field wiring, including shields.
- Check the thermocouple for an open circuit.
- Verify that the thermocouple type matches the configuration.
- Measure the incoming mV signal and verify that it is within the specified thermocouple range.

2400-2431

Description IOPoint [ ] - RTD voltage out of range ([ ] mV)

Possible Cause

- There is a break in the RTD wiring/cabling or high impedance is blocking the signal.
- The sensor impedance is too high.
- The RTD device has failed.

Solution

- Check the field wiring for an open circuit or high impedance.
- Verify that the connections to the terminal board are correct.
- Check the RTD for proper operation and sensor type.
- Replace the I/O pack.

2432-2463

Description IOPoint [ ] - RTD current out of range ([ ] mA)

Possible Cause

- There is a break in the RTD wiring/cabling open or high impedance is blocking the signal.
- There is a break in the connections to the terminal board.
- The current source on the PUAA has failed.
- The measurement device has failed.

Solution

- Check the field wiring for an open circuit or high impedance.
- Verify that the connections to the terminal board are correct.
- Replace the I/O pack.

2464-2495

Description IOPoint [ ] - RTD resistance beyond range of configured RTD type ([ ] Ohms)

Possible Cause

- RTD input exceeded range of linearization (lookup) table for this RTD type. Refer to documentation for specified RTD ranges.
- The wrong type of RTD has been configured or selected by default.
- High-resistance values were created by high voltage and/or low current.

Solution

- Check the field wiring and sensor.
- Verify that the RTD-type configuration matches the attached device type.
- Check the field wiring for high impedance.

2496-2527

Description IOPoint [ ] - HART not initialized

Possible Cause Unable to communicate with connected HART sensor

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

2528-2559

Description IOPoint [ ] - HART address mismatch

Possible Cause One of configuration parameters (**Hart_MfgID**, **Hart_DevTyp**, or **Hart_DevID** does not match the field device.

Solution From the ToolboxST Component Editor, PUAA, Hardware tab, right-click the device and select **Upload the HART ID**.

2560-2591

Description IOPoint [ ] - HART field device modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what modification was made and if it is correct, then clear the diagnostic. From the **Variables** tab, toggle the **AckHartCfgChange** to TRUE and then back to FALSE.

2592-2623

Description IOPoint [ ] - HART control parameter mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in Hart Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

2624-2655

Description IOPoint [ ] - HART extended status mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in Hart Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

2656

Description HART control messages disabled. AMS HART messages only

Possible Cause The **AMS_Msgs_Only** parameter is **Enabled**. No control messages are sent. This parameter overrides the values in the **Hart_Ctrl** and **Hart_ExStatus** for each individual channel.

Solution

- To send AMS messages only, but clear this alarm: Set the **AMS_Msgs_Only** parameter to **Disabled** and set each channel's **Hart_Ctrl** and **Hart_ExStatus** to zero.
- To allow control messages *and* AMS messages, set **AMS_Msgs_Only** to **Disabled**.

2657

Description Coldjunction temperature [ ] value beyond specified table limits (-40 °F to 215 °F) or (-40 °C to 102 °C)

Possible Cause

- Cold Junction temperature exceeds the lookup table range (-40 to 215°F) or (-40 to 101.67 °C)
- Ambient temperature is too hot/cold

Solution

- If remote or backup cold junction is being used, then confirm those values are within the lookup table range.
- Check the ambient temperature. If the temperatures are too high or low, power off the I/O pack and restart it after the ambient temperatures are within -40 to 215 °F.

2658-2689

Description IOPoint [ ] - Internal burden resistor protection activated

Possible Cause

- The I/O pack has detected too much (> 30 mA) current flowing through the internal burden resistor on indicated I/O point and has opened an internal switch to protect the given I/O point. The I/O pack periodically closes the switch and checks again if the current has dropped below the threshold.
- Improper device operation or Improper wiring

Solution

- Check the field wiring and determine if a connected device is sourcing currents beyond the specified range on the given I/O point.
- After checking and correcting the wiring, wait approximately 15 seconds for the error to correct itself.

2690-2721

Description IOPoint [ ] - Shorted field wire detected

Possible Cause A short circuit has been detected at the terminal board, based on the sensor type.

Solution Digital Input:

- Check the wiring between the terminal board and the device.
- Verify that the recommended line monitoring resistors are being used (refer to the PUAA user documentation).

2722-2753

Description IOPoint [ ] - NAMUR Sensor failure detected

Possible Cause Detected NAMUR sensor operation is outside its two normal current levels (between 1.0 mA and 2.2 mA)

Solution Digital Input:

- Check the wiring between the terminal board and the sensor.
- Check the sensor for proper operation.
- Replace the NAMUR device.

2754-2785

Description IOPoint [ ] - Input Saturation detected

Possible Cause An internal component's valid input range was exceeded. This could be due to the following reasons:

- Input signal equal to or exceeds the valid input range for the input type (improper sensor connected, sensor failure)
- Open-circuit field wiring
- Internal hardware failure

Solution

- Current Input: check field wiring and verify that the input source is between -11 V and 20 V (or 80 mA).
- Voltage Input:
  - For ± 5 V input, check field wiring and verify that the input source is between -11 V and 20 V.
  - For ± 10 V input, check field wiring and verify that the input source is between -11 V and 22 V.
- RTD Input:
  - For MINCO_CA type, check for open circuits in the field wiring and then verify that the input source is between -78.125 mV and 78.125 mV.
  - For all other RTD types, check field wiring and verify that the input source is between -1.25 V and 1.25 V.
- TC Input: check field wiring and verify that the input source is between -625 mV and 625 mV.
- Digital Input:
  - For externally wetted inputs, check field wiring and verify that the input source is between -11 V and 20 V.
  - For internally wetted inputs, check field wiring and verify input source is between -11 V and 20 V.
- Pulse Accumulator (PA) Input: check field wiring and verify that the input source is between -11 V and 22 V.

2818

Description Outputs are disabled

Possible Cause Input voltage dropped below 18 V. I/O pack or module input power is required to be within range 28 V ±5%.

Solution Check the I/O pack or module power within the control cabinet.

2819-2820

Description Cold Junction Sensor [ ] failure

Possible Cause The Cold Junction temperature sensor on the terminal board failed to deliver an updated reading, most likely due to hardware failure.

Solution

- Verify that the I/O module is properly seated on the terminal board.
- Replace the I/O module.
- Replace the terminal board.

2821

Description Cold Junction difference detected

Possible Cause The difference between the two local Cold Junction sensors on the terminal board exceeds 5°C (41 °F), indicating a failed sensor. If ColdJuncType is set to Local, then the BackupCj will be used instead.

Solution

- Check for abnormal ambient air heat sources close to the module.
- Replace the terminal board.

2822

Description Internal hardware issue detected (code[ ])

Possible Cause An internal hardware issue has occurred, most likely due to an internal hardware failure. Possible causes include:

- Internal power supply failure
- Internal data corruption (either due to a single-event upset or internal failure)

Solution

- Cycle power on the I/O module.
- Replace the I/O module.

17.17 YUAA Diagnostic Alarms

The following diagnostic alarms are specific to the YUAA universal analog functions. Common Mark VIeS I/O module processor diagnostics are listed separately.

32-63

Description Failed loading configuration for point [ ]

Possible Cause

- Attempted to change an already configured point to a different point type without making the point unused first.
- Hardware communication failure

Solution

- Set the PointType for the specified point to Unused and download before changing to desired PointType.
- Re-download configuration

64-95

Description Point [ ] unhealthy

Possible Cause Use the following table to identify the possible cause for this unhealthy point, based on the configured Mode of the channel and field device.

Solution Use the following table to identify a solution for this unhealthy point, based on the configured Mode of the channel and field device.

Point Unhealthy Troubleshooting

Mode	Possible Cause	Solution
CurrentInput	The excitation to transducer is wrong or missing.	Check the field wiring and connections to indicated analog input channel. Check the field device for failure. Check the PUAA power from terminal board screw.
CurrentInput	The transducer is defective.	Replace the transducer.
CurrentInput	There is an open or short-circuit on input.	Check the field wiring and connections to indicated analog input channel.
CurrentInput	The analog current input is beyond the specified range 4-20 mA	Check the field wiring and connections to indicated analog input channel. Check the field device for failure. If incorrectly configured, from the TooblxoST Component Editor, modify the specified range.
Current Input	The burden resistor protection has been activated, greater than 30 mA has been detected	Check the field wiring and connections to indicated analog input channel.
Current Input	Hardware failure in the I/O Module or Terminal Board.	Replace the I/O Module. Replace the Terminal Board.
VoltageInput	The excitation to transducer is wrong or missing.	Check the field wiring and connections to indicated analog input channel. Check the field device for failure. Check the PUAA power from terminal board screw is correct.
VoltageInput	The transducer is defective.	Replace the transducer.
VoltageInput	There is an open or short-circuit on input.	Check the field wiring and connections to indicated analog input channel.
VoltageInput	The analog voltage input is beyond the specified range.	Check the field wiring and connections to indicated analog input channel. Check the field device for failure. If incorrectly configured, from the ToolboxST Component Editor, modify the specified range.

Point Unhealthy Troubleshooting (continued)

Mode	Possible Cause	Solution
CurrentOutput	The commanded output is beyond the range of the output.	Verify that the commanded output is within the range of the output.
CurrentOutput	There is a field wiring problem	Check the field wiring and device.
CurrentOutput	There is an open loop or too much resistance in the loop.	Confirm the correct I/O pack 28 V input power. Check the field wiring and device.
CurrentOutput	The I/O pack has failed.	Replace the I/O pack.
CurrentOutput	The terminal board has failed.	Replace the terminal board.
RTD	RTD wiring/cabling open or high impedance.	Check the field wiring and connections to indicated RTD input channel.
RTD	Open on connections to the terminal board.	Check the field wiring and field device.
RTD	RTD device failed.	Replace the RTD device.
RTD	PUAA module internal hardware problem.	Replace the I/O pack.
RTD	Current source on PUAA for RTD faulty or measurement device failed.	Replace the I/O pack. Replace the field device.
RTD	Wrong type of RTD configured or selected by default.	From the ToolboxST application, modify the PUAA I/O pack to correct the configuration.
RTD	High-resistance values created by high voltage and/or low current.	Check the field wiring and field device.
Thermocouple	Thermocouple millivolt input exceeds the limits of the PUAA hardware.	Check field wiring, including shields. Measure incoming mV signal and verify that it is within the specified thermocouple range. Check installation of the I/O pack on the terminal board. This problem is usually not an I/O pack or terminal board failure if other thermocouples are working correctly. Verify that the installed type of thermocouple device matches the configuration found in the ToolboxST application. Replace the field device.
Thermocouple	Cold junction input to the analog-to-digital converter exceeded the limits of the converter. If a cold junctions fails, the CJ_Backup value is used.	Check installation of the I/O pack on the terminal board. If local CJ, replace the terminal board.
Thermocouple	Thermocouple mV input exceeded range of linearization (lookup) table for this TC type. Refer to documentation for specified thermocouple ranges.	Check field wiring, including shields. Measure incoming mV signal and verify that it is within the specified thermocouple range. Check installation of the I/O pack on the terminal board. Note: The problem is usually not an I/O pack or terminal board failure if other thermocouples are working correctly. Verify that the installed type of thermocouple device matches the configuration found in the ToolboxST application. Replace the field device.
Thermocouple	Thermocouple configured as wrong type.	Verify that the installed type of thermocouple device matches the configuration found in the ToolboxST application.
Thermocouple	Board detected a thermocouple open	Check field wiring, including shields. Replace the field device.
Thermocouple	Stray voltage or noise caused the input to exceed its range.	Check field wiring, including shields. Replace the field device.

Point Unhealthy Troubleshooting (continued)

Digital Input	Internal Wetted Input exceeded range of operation	Check field wiring. Measure incoming mA signal and verify that it is 10 mA.
Digital Input	External Wetted Input exceeded range of operation	Check field wiring. Measure voltage across digital inputs terminal points and verify it is between -1 V and 21 V.
Digital Input	NAMUR input exceeded range of operation	Check field wiring. Verify mA signal through field device does not exceed 9 mA. Replace the field device.
Digital Input	Digital Input mode configured as wrong type	Verify field wiring and field device matches the configured Input Mode found in the ToolboxST application.
Digital Input	Open circuit detected on digital input signal	Check the wiring between the terminal board and the device. Verify that the recommended line monitoring resistors are being used.
Digital Input	Short detected on digital input signal	Check the wiring between the terminal board and the device. Verify that the recommended line monitoring resistors are being used.
Pulse Accumulator	Pulse input voltage exceeds the limits of the PUAA hardware	Check field wiring. Measure incoming signal and verify that it is within -11 V and 21 V. Replace the field device.

96

Description Invalid calibration settings

Possible Cause

- Calibration file not detected
- Calibration file corrupted
- Calibration constants invalid
- Hardware Failure

Solution Replace the I/O pack.

97-98

Description Cold Junction temp [ ] exceeds range limit ([ ])

Possible Cause Cold junction input to the analog-to-digital converter exceeded the limits of the converter. If a cold junctions fails, the **CJ_Backup** value is used.

Solution

- Check the mounting of the I/O pack on the terminal board.
- Replace the terminal board.
- Replace the I/O pack.

99-130

Description IOPoint [ ] - Current output commanded current feedback error

Possible Cause

- The measured current feedback does not match the commanded current.
- There is an open circuit on an output.
- Output impedance is too high (max allowed 800 Ohms).

Solution

- Check the field wiring and device.
- Verify that the commanded output is within output range.
- Replace the I/O pack.

131-162

Description IOPoint [ ] - Open field wire detected

Possible Cause An open circuit has been detected at the terminal board based on the sensor type.

Solution

- Digital Input:
    - Check the wiring between the terminal board and the device.
    - Verify that the recommended line monitoring resistors are being used (refer to the PUAA user documentation).
- Thermocouple Input: verify the wiring of the thermocouple at the inputs.

163-194

Description IOPoint [ ] - Thermocouple input millivolt exceeds hardware limit ([ ] mV)

Possible Cause

- Thermocouple millivolt input exceeds the hardware limit
- An open thermocouple was detected.

Solution This is usually not a I/O pack or terminal board failure if other thermocouples are working correctly.

- Check the field wiring, including shields.
- Check the installation of the I/O pack on the terminal board.
- Replace the I/O pack.

195-226

Description IOPoint [ ] - Thermocouple value beyond range of configured TC type ([ ] deg)

Possible Cause

- Thermocouple mV input exceeded range of linearization (lookup) table for this TC type. Refer to documentation for specified thermocouple ranges.
- Thermocouple configured as wrong type
- Stray voltage or noise caused the input to exceed its range.

Solution

- Check the field wiring, including shields.
- Check the thermocouple for an open circuit.
- Verify that the thermocouple type matches the configuration.
- Measure the incoming mV signal and verify that it is within the specified thermocouple range.

2400-2431

Description IOPoint [ ] - RTD voltage out of range ([ ] mV)

Possible Cause

- There is a break in the RTD wiring/cabling or high impedance is blocking the signal.
- The sensor impedance is too high.
- The RTD device has failed.

Solution

- Check the field wiring for an open circuit or high impedance.
- Verify that the connections to the terminal board are correct.
- Check the RTD for proper operation and sensor type.
- Replace the I/O pack.

2432-2463

Description IOPoint [ ] - RTD current out of range ([ ] mA)

Possible Cause

- There is a break in the RTD wiring/cabling open or high impedance is blocking the signal.
- There is a break in the connections to the terminal board.
- The current source on the PUAA has failed.
- The measurement device has failed.

Solution

- Check the field wiring for an open circuit or high impedance.
- Verify that the connections to the terminal board are correct.
- Replace the I/O pack.

2464-2495

Description IOPoint [ ] - RTD resistance beyond range of configured RTD type ([ ] Ohms)

Possible Cause

- RTD input exceeded range of linearization (lookup) table for this RTD type. Refer to documentation for specified RTD ranges.
- The wrong type of RTD has been configured or selected by default.
- High-resistance values were created by high voltage and/or low current.

Solution

- Check the field wiring and sensor.
- Verify that the RTD-type configuration matches the attached device type.
- Check the field wiring for high impedance.

2496-2527

Description IOPoint [ ] - HART not initialized

Possible Cause Unable to communicate with connected HART sensor

Solution

- Verify that the field device is attached to the correct I/O point.
- Using a HART handheld communicator, confirm that the field device is operating correctly and communicating.

2528-2559

Description IOPoint [ ] - HART address mismatch

Possible Cause One of configuration parameters (**Hart_MfgID**, **Hart_DevTyp**, or **Hart_DevID** does not match the field device.

Solution From the ToolboxST Component Editor, PUAA, Hardware tab, right-click the device and select **Upload the HART ID**.

2560-2591

Description IOPoint [ ] - HART field device modified

Possible Cause The configuration of the HART field device was externally modified with either an AMS or a HART handheld communicator.

Solution Determine what modification was made and if it is correct, then clear the diagnostic. From the **Variables** tab, toggle the **AckHartCfgChange** to TRUE and then back to FALSE.

2592-2623

Description IOPoint [ ] - HART control parameter mismatch - configured: [ ] received: [ ]

Possible Cause The number of dynamic variables returned in Hart Message 3 (Read dynamic variables) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

2624-2655

Description IOPoint [ ] - HART extended status mismatch - configured: [ ] received: [ ]

Possible Cause The number of extended status bytes returned in Hart Message 48 (Read extended status) does not agree with the ToolboxST configuration.

Solution Verify that the correct device is attached, and set the ToolboxST configured value to either 0 or the received value.

2656

Description HART control messages disabled. AMS HART messages only

Possible Cause The **AMS_Msgs_Only** parameter is **Enabled**. No control messages are sent. This parameter overrides the values in the **Hart_Ctrl** and **Hart_ExStatus** for each individual channel.

Solution

- To send AMS messages only, but clear this alarm: Set the **AMS_Msgs_Only** parameter to **Disabled** and set each channel's **Hart_Ctrl** and **Hart_ExStatus** to zero.
- To allow control messages *and* AMS messages, set **AMS_Msgs_Only** to **Disabled**.

2657

Description Coldjunction temperature [ ] value beyond specified table limits (-40 °F to 215 °F) or (-40 °C to 102 °C)

Possible Cause

- Cold Junction temperature exceeds the lookup table range (-40 to 215°F) or (-40 to 101.67 °C)
- Ambient temperature is too hot/cold

Solution

- If remote or backup cold junction is being used, then confirm those values are within the lookup table range.
- Check the ambient temperature. If the temperatures are too high or low, power off the I/O pack and restart it after the ambient temperatures are within -40 to 215 °F.

2658-2689

Description IOPoint [ ] - Internal burden resistor protection activated

Possible Cause

- The I/O pack has detected too much (> 30 mA) current flowing through the internal burden resistor on indicated I/O point and has opened an internal switch to protect the given I/O point. The I/O pack periodically closes the switch and checks again if the current has dropped below the threshold.
- Improper device operation or Improper wiring

Solution

- Check the field wiring and determine if a connected device is sourcing currents beyond the specified range on the given I/O point.
- After checking and correcting the wiring, wait approximately 15 seconds for the error to correct itself.

2690-2721

Description IOPoint [ ] - Shorted field wire detected

Possible Cause A short circuit has been detected at the terminal board, based on the sensor type.

Solution Digital Input:

- Check the wiring between the terminal board and the device.
- Verify that the recommended line monitoring resistors are being used (refer to the PUAA user documentation).

2722-2753

Description IOPoint [ ] - NAMUR Sensor Failure detected

Possible Cause Detected NAMUR sensor operation is outside its two normal current levels (between 1.0 mA and 2.2 mA)

Solution Digital Input:

- Check the wiring between the terminal board and the sensor.
- Check the sensor for proper operation.
- Replace the NAMUR device.

2754-2785

Description IOPoint [ ] - Input Saturation detected

Possible Cause An internal component's valid input range was exceeded. This could be due to the following reasons:

- Input signal equal to or exceeds the valid input range for the input type (improper sensor connected, sensor failure)
- Open-circuit field wiring
- Internal hardware failure

Solution

- Current Input: check field wiring and verify that the input source is between -11 V and 20 V (or 80 mA).
- Voltage Input:
  - For ± 5 V input, check field wiring and verify that the input source is between -11 V and 20 V.
  - For ± 10 V input, check field wiring and verify that the input source is between -11 V and 22 V.
- RTD Input:
  - For MINCO_CA type, check for open circuits in the field wiring and then verify that the input source is between -78.125 mV and 78.125 mV.
  - For all other RTD types, check field wiring and verify that the input source is between -1.25 V and 1.25 V.
- TC Input: check field wiring and verify that the input source is between -625 mV and 625 mV.
- Digital Input:
  - For externally wetted inputs, check field wiring and verify that the input source is between -11 V and 20 V.
  - For internally wetted inputs, check field wiring and verify input source is between -11 V and 20 V.
- Pulse Accumulator (PA) Input: check field wiring and verify that the input source is between -11 V and 22 V.

2786-2817

Description IOPoint [ ] - HART field device not write protected in locked mode

Possible Cause It is expected that field devices be put into locked mode via an AMS or HART handheld communicator when the Mark VIeS is in locked mode. This alarm indicates that the device on the specified channel is not in a write-protected or secured mode while the controller is in locked mode.

Solution Refer to the field device manual to determine how to place the device in the write-protected mode. All devices used in a safety-protected system must be able to be placed in a read-only mode.

2818

Description Outputs are disabled

Possible Cause Input voltage dropped below 18 V. I/O pack or module input power is required to be within range 28 V ±5%.

Solution Check the I/O pack or module power within the control cabinet.

2819-2820

Description Cold Junction Sensor [ ] failure

Possible Cause The Cold Junction temperature sensor on the terminal board failed to deliver an updated reading, most likely due to hardware failure.

Solution

- Verify that the I/O module is properly seated on the terminal board.
- Replace the I/O module.
- Replace the terminal board.

2821

Description Cold Junction difference detected

Possible Cause The difference between the two local Cold Junction sensors on the terminal board exceeds 5°C (41 °F), indicating a failed sensor. If ColdJuncType is set to Local, then the BackupCj will be used instead.

Solution

- Check for abnormal ambient air heat sources close to the module.
- Replace the terminal board.

2822

Description Internal hardware issue detected (code[ ])

Possible Cause An internal hardware issue has occurred, most likely due to an internal hardware failure. Possible causes include:

- Internal power supply failure
- Internal data corruption (either due to a single-event upset or internal failure)

Solution

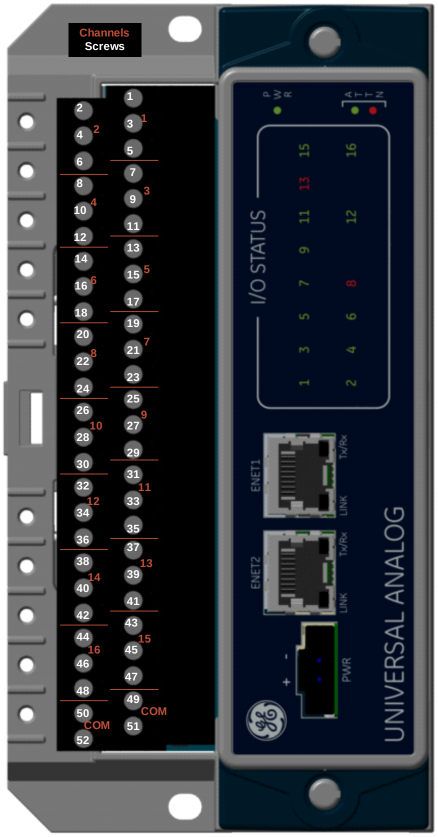
- Cycle power on the I/O module.
- Replace the I/O module.

17.18 SUAA Universal Analog Terminal Board

The SUAA terminal board is a simplex universal analog I/O board that provides 48 terminals, grouped in threes to provide 16 channels or IO points. There are four additional screws (49, 50, 51, and 52) that provide a grounding option for special-case I/O pack-powered 4–wire field device applications. A single PUAA or YUAA I/O pack mounts to the terminal board, using two screws. SUAA provides local cold junction sensing at the terminal block (two local cold junctions). The pack-supplied power from the terminals to the field devices is a current-limited 24 V supply.

The terminal blocks are removable on a per channel basis because of how the points are grouped together as PWR_RTN, IO+, and IO- respectively. For example, screws 1, 3, 5 provide channel 1, with screw 1 = PWR_RTN, screw 2 = IO+, and screw 3 = IO-.

Although this screw and channel assignment continues for the remaining screws and channels, there are certain modes where power is supplied from the IO+ screw, or where power is supplied at the device itself (in either case the first screw in the series is not used).



SUAA Terminal Board Screw Definitions

Screw	Name	Channel	Screw	Name	Channel
2	PWR_RTN	2	1	PWR_RTN	1
4	IO+	2	3	IO+	1
6	IO-	2	5	IO-	1
8	PWR_RTN	4	7	PWR_RTN	3
10	IO+	4	9	IO+	3
12	IO-	4	11	IO-	3
14	PWR_RTN	6	13	PWR_RTN	5
16	IO+	6	15	IO+	5
18	IO-	6	17	IO-	5
20	PWR_RTN	8	19	PWR_RTN	7
22	IO+	8	21	IO+	7
24	IO-	8	23	IO-	7
26	PWR_RTN	10	25	PWR_RTN	9
28	IO+	10	27	IO+	9
30	IO-	10	29	IO-	9
32	PWR_RTN	12	31	PWR_RTN	11
34	IO+	12	33	IO+	11

SUAA Terminal Board Screw Definitions (continued)

Screw	Name	Channel	Screw	Name	Channel
36	IO-	12	35	IO-	11
38	PWR_RTN	14	37	PWR_RTN	13
40	IO+	14	39	IO+	13
42	IO-	14	41	IO-	13
44	PWR_RTN	16	43	PWR_RTN	15
46	IO+	16	45	IO+	15
48	IO-	16	47	IO-	15
50	COM		49	COM	
52	COM		51	COM	

18 PDM Power Distribution Modules

18.1 Power Distribution Overview

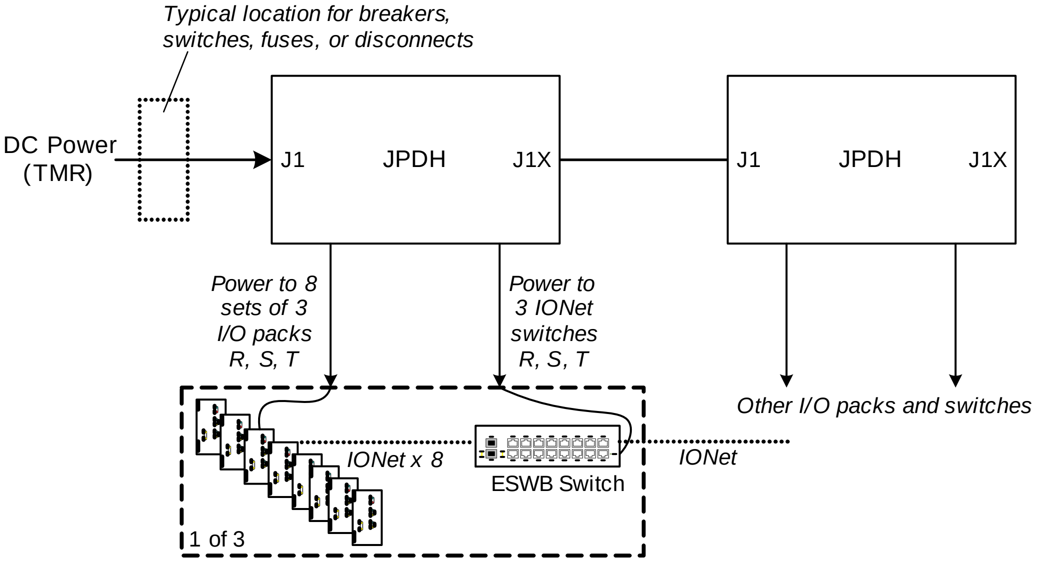
The Power Distribution Modules (PDM) are designed specifically for the Mark* VIe and Mark VIeS control systems. The term PDM is used as a name for all of the individual pieces forming the power distribution for a control system. The PDM uses individual boards to accept and condition primary control power inputs of 125 V dc, 48 V dc, 24 V dc, and 100 to 250 V ac for use in redundant combinations. Applied power is distributed to system terminal boards for use in field circuits and converted to 28 V dc for operation of the Mark VIe and Mark VIeS I/O modules. The PDM is divided into two different categories: core and branch.

Core distribution circuits are a portion of the PDM serving as the primary power management for a cabinet or series of cabinets. Input power from one or more sources is received by a corresponding module or board. The power is distributed to terminal boards and one or more bulk power supplies producing 28 V dc power to operate the control electronics. The 28 V power is monitored and distributed by one or more 28 V output boards. The JPDB accepts ac input power from two independent ac sources. Input power is managed by the JPDE (24/48 V dc) and the JPDF (125 V dc).

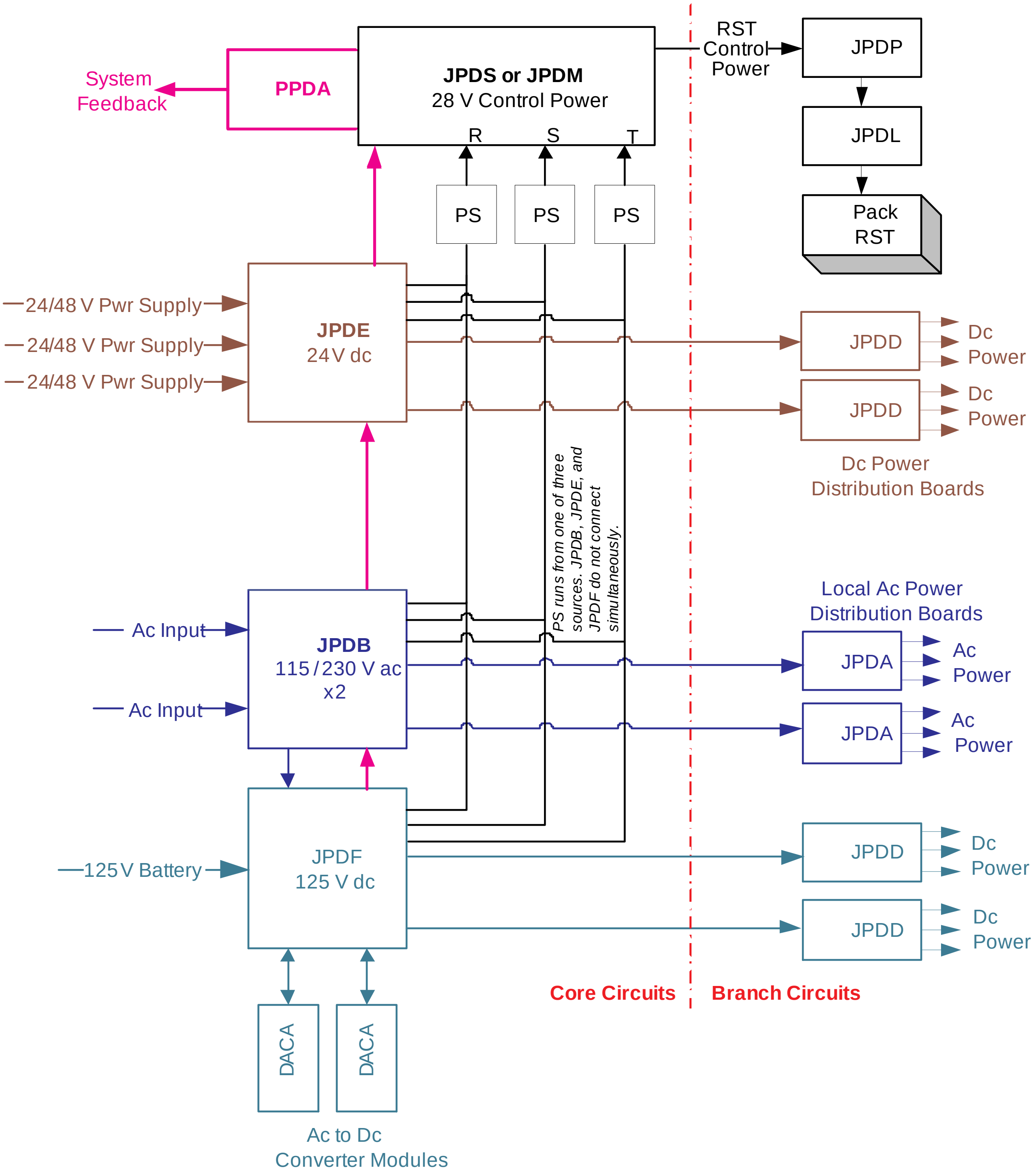
The 28 V dc control power output boards (JPDS, *JPDM*, JPDG and JPDC) can host a PPDA I/O pack to provide power system feedback. Ribbon cables can daisy chain other core boards in the system to the board holding the PPDA. Complete monitoring and system feedback sets this power system apart from conventional methods of power distribution. Bulk power supplies are considered a part of the core PDM system.

Branch circuit boards split the power output from the PDM core components into individual ac and dc circuits for use in the cabinets. Elements receiving power from the branch circuits provide their own power status feedback signals to the control system. Branch circuit elements are usually single circuit boards. Branch circuits do not connect to the PPDA I/O pack for system feedback.

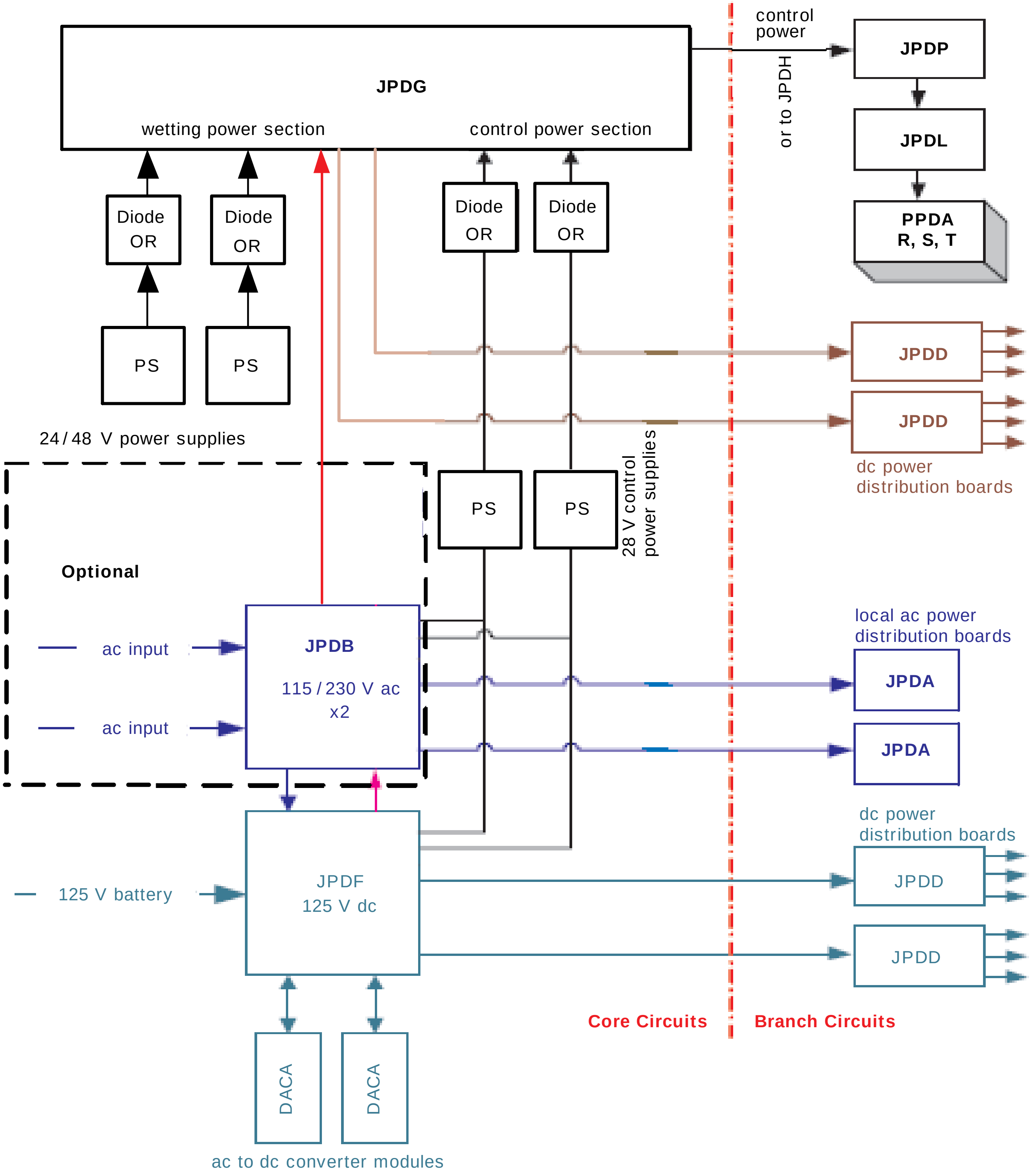
Remote I/O Cabinet (DC Fed)


Typical location for breakers, switches, fuses, or disconnects
DC Power (TMR)
J1
JPDH
J1X
J1
JPDH
J1X
Power to 8 sets of 3 I/O packs R, S, T
Power to 3 IONet switches R, S, T
Other I/O packs and switches
IONet x 8
ESWB Switch
IONet
1 of 3

JPDH is used for power branch circuits.



JPDS or JPDM Example



JPDG Example

18.1.1 Core Components

The following core components have primary control power inputs of 125 V dc, 24 V dc, and 100 to 250 V ac for use in redundant combinations:

- **IS2020JPDB** consists of a sheet metal structure containing two sets of input line filters and the IS200JPDB circuit board. Power input from two separate ac sources passes through the line filters to the JPDB board. The board provides output for bulk 28 V dc control power supplies, terminal boards, and other loads. The JPDB board uses ribbon cable connections for system feedback through PPDA including both ac bus voltages and individual branch circuit feedback. There are two versions of the IS200JPDB board:
  - **IS2020JPDBG2** can connect to an external ac selector module
  - **IS2020JPDBG1** omits this feature
- **IS2020JPDC** combination board combines input and output functions from several designs to provide distribution of 125 V dc, 100 to 250 V ac, and 28 V dc to other boards within a turbine control system. The JPDC module consists of a sheet metal structure containing diode assembly, two resistors, and a JPDC board. It provides a single 100 to 250 V ac connection at the bottom, one or two 125 V dc battery input connections, and up to three separate 28 V dc source connections. The PPDA mounts on the JPDC. The JPDC module combines functionality of JPDM, JPDB, and JPDF modules.
- **IS200JPDE** 24/48 V dc input board mounts on a sheet metal structure. Power input is accepted from a battery and two dc power supplies. An optional dc circuit breaker and filter are available for use with a battery power source. The JPDE board distributes the dc power to terminal boards and other loads. In small systems, JPDE can be used between a battery and 150 W dc power supplies. The JPDE board uses ribbon cable connections for system feedback through the PPDA, including dc bus voltage, ground fault detection, and individual branch circuit status.
- **IS2020JPDF** 125 V dc module consists of a sheet metal structure containing a dc circuit breaker, input filter, series diode, current limiting resistors, and an IS200JPDF circuit board. Power from a 125 V dc battery feeds through the circuit breaker, filter, and diode to the JPDF board. The board also has connections for two DACA modules providing ac input/125 V dc output. When one or both DACA modules are used, a wire harness between JPDB and JPDF is used for the ac power. The result is a module that could accept power from a battery and / or one or two ac sources, creating a highly reliable dc supply.

  The IS200JPDF board distributes dc power to bulk dc: dc supplies, terminal boards, and other loads. Two special output circuits, with series current limiting resistors, are provided for specific applications. The JPDF board uses ribbon cable connections for system feedback through PPDA including dc bus voltage, ground fault detection, and individual branch circuit status. The JPDF supports a floating dc bus for wetting power that is centered on earth by using resistors.
- **IS200JPDG** provides distribution of 28 V dc (control power) and 48 V or 24 V dc (wetting power) to other boards within the control system. For both control and wetting power, the JPDG supports dual redundant power supply inputs through external diodes. JPDG provides fuse protection for all 28 V dc and 24/48 V dc outputs. The PPDA I/O pack mounts on the JPDG board.

For wetting power distribution, the JPDG is able to operate at either 24 V dc or 48 V dc. The JPDG supports a floating dc bus for wetting power that is centered on earth by using resistors. It provides voltage feedback through the PPDA to detect system ground faults, and integrates into the PDM system feedback. JPDG can support sensing and diagnostic for two ac signals, which are distributed outside this board.

- **IS200JPDM** 28 V dc control power output board is similar to JPDS except it has fewer output connectors and includes branch circuit fuses. JPDM is used for systems requiring 28 V dc supplies with current limit exceeding branch circuit capability. This includes systems that use two or more 500 W systems connected together forming a redundant control power source. The PPDA I/O pack mounts on the JPDM board.

- **IS200JPDS** 28 V dc control power output board mounts on a sheet metal structure. The JPDS circuit board contains three independent 28 V dc power buses with one bulk power supply input for each bus. Barrier screw terminals connect the power buses when a single bus with multiple supplies is desired. Output circuits from JPDS do not contain fuses with the exception of three auxiliary circuits.

The JPDS uses the current limit of the attached power supplies for branch circuit protection. The PPDA I/O pack mounts on the JPDS board. The JPDS board uses ribbon cable connections for system feedback through the PPDA, including dc bus voltage, power supply status contact feedback, and auxiliary circuit status.

- **IS220PPDA** I/O pack – The optional power diagnostic I/O pack can mount on a JPDC, JPDG, JPDM, or JPDS board.
- **DACA** ac to dc conversion module – This module takes incoming ac power and converts it to 125 V dc. It is used in conjunction with or in place of 125 V battery power. DACA provides capacitive energy storage for power-dip ride through when required.
- **Vendor Manufactured Control Power Supplies (VMCPS)** – There are only certain *VMCPS* used with the Mark VIe and Mark VIeS control systems.

18.1.1.1 PPDA Status Feedback

The Mark VIe and Mark VIeS control systems can use a PPDA I/O pack for power distribution system feedback. The core JPDx boards can function without a working connection to the PPDA making it a non-critical element of the system. There are no provisions for PPDA redundancy without using a fully redundant set of JPDx boards. The PPDA provides timely information supporting system maintenance. Refer to the section, *PPDA Power Distribution System Feedback*.

The PPDA provides five analog signal inputs with an electronic ID for each connected core PDM component. The PPDA checks the ID lines to determine what boards are attached and then populates the corresponding signal space values. The PPDA also operates local indicator lamps displaying system status.

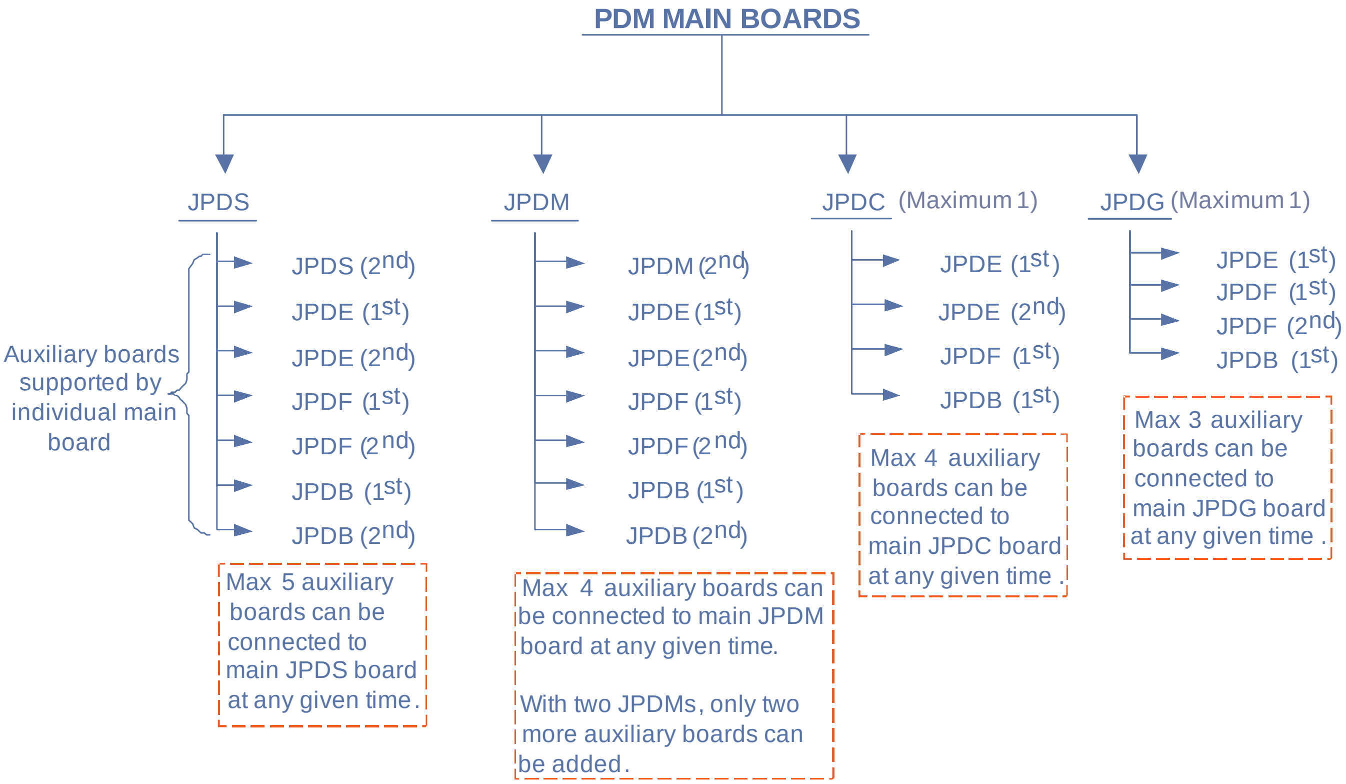
Ribbon cables are used to daisy chain other core boards to the board hosting the PPDA. The I/O pack can identify connected core boards and pass feedback signals to one or two IONet connections. The PPDA has numerous indicator LEDs, providing visual power distribution status. The PPDA does not take direct protective actions. It only reports information to the Mark VIe or Mark VIeS controller where corrective action can be programmed. Refer to the section, *Valid Core Board Combinations*.

18.1.1.2 Valid Core Board Combinations

The PPDA can receive feedback from as many as six connected core PDM components. The following rules apply when cabling components into a PPDA:

- JPDS, JPDM, JPDG, or JPDC is selected as the power distribution main board that hosts a PPDA I/O pack.
- A maximum of six boards can be used with a single PPDA I/O pack.
- When used, a single JPDM or JPDC board counts as two boards due to the large number of PPDA feedback signals used. A single JPDG board counts as three boards due to the large number of PPDA feedback signals.
- Either JPDM or JPDS can be used. The two board types cannot be mixed in a system.
- A maximum of two of any given board type can be used , with the exception of JPDG and JPDC; only one of each type of these boards is allowed in chain.
- When JPDG is used in the system, JPDS, JPDM, or JPDC cannot be used along with JPDG. Only one JPDB and one JPDE can be used along with JPDG. Two JPDFs can be used along with JPDG. Two JPDGs cannot be used in the power distribution diagnostic daisy chain.

The following figure displays all possible combinations for JPDG, JPDS, JPDM, and JPDC boards.



Max 5 auxiliary boards can be connected to main JPDS board at any given time.

Max 4 auxiliary boards can be connected to main JPDM board at any given time.

With two JPDMs, only two more auxiliary boards can be added.

Max 4 auxiliary boards can be connected to main JPDC board at any given time .

Max 3 auxiliary boards can be connected to main JPDG board at any given time .

Core Board Combinations

18.1.2 Branch Circuit Boards

Branch circuit boards provide additional distribution of dc/ac power for output of the core PDM elements. These boards are not connected to the PPDA feedback cable. Branch circuit boards are identified as:

- **IS200JPDA** distributes a single ac power output into multiple loads. This board has four switched ac outputs. Each load has a switch, for maintenance purposes, and a fuse on the line side with LEDs for each load.
- **IS200JPDD** distributes a single dc power output into multiple loads. It can be used with a single input of 24 V, 48 V, or 125 V dc. Each load has a switch for maintenance purposes and fuses with a local indicator light.

- **IS200JPDL** provides two control power I/O pack power output connectors for each of the R, S, and T power sources. JPDL can be connected in series with other JPDL boards providing power to a vertical column of terminal boards and their associated I/O packs. Each output is protected with a self-resetting fuse that is coordinated with the wire size the pack connectors can accept.
- **IS200JPDP** receives R, S, and T power from the 28 V control power board (JPDS, JPDM, JPDG, or JPDC) and distributes it to the local pack power distribution board (JPDL). JPDP contains no fuses or indicators.
- **IS200JPDH** is a 28 V dc power distribution board. This board receives 28 V dc power from the R, S and T power source. It provides up to 24 output connectors of 28 V dc for I/O packs, eight each for R, S and T. These outputs are protected with a positive temperature coefficient fuse. The JPDH board also provides three unprotected 28 V dc outputs to be connected to R, S and T Ethernet switches. The JPDH may also be used in daisy-chain mode to distribute 28 V dc power to more than 24 I/O packs.

18.1.3 Circuit Protection

Circuit protection for the PDM includes:

- Fault current protection limits the current to the capability of the system components.
- Branch circuit system feedback
- Ground fault protection in floating systems
- Redundant applications, if possible

Systems using multiple power applications create the possibility of applying the wrong power to a load or interconnecting power buses. The PDM use specific connector conventions to eliminate this problem. The specific connectors are displayed in the following table.

Power from main PDM	Connector
125 V dc from JPDF to JPDD	2-pin Mate-N-Lok®
125/230 V ac from JPDB to JPDA	3-pin Mate-N-Lok
24/48 V dc from JPDE to JPDD	4-pin in-line Mate-N-Lok
28 V dc control power from JPDS to JPDP	3x2 pin Mate-N-Lok
28 V dc control power from JPDP to JPDL	5-pin in-line Mate-N-Lok
Dc power supply output to JPDE, JPDS, JPDM	3x3 pin Mate-N-Lok (power + status)
DACA connection to JPDF	3x4 pin Mate-N-Lok

Exceptions to the above table exist. An effort has been made to clearly mark the connector function on the boards. For example: a 5-pin in-line Mate-N-Lok connector is used on JPDB and JPDF to pass ac power between the boards. Both connectors are clearly marked for their intended use and are physically placed to ensure proper connection.

Existing terminal boards designs present the greatest risk of being improperly connected. These boards use a three position Mate-N-Lok for power input regardless of whether it is an ac or dc connection. The existing boards also have two parallel connectors to allow power daisy-chain wiring within a panel.

The JPDF board can detect an improper wiring connection, such as applying ac power on a floating 125 V dc battery bus, and report it through the PPDA I/O pack.

18.1.3.1 P28 Control Power Protection

JPDS/JPDM/JPDG/JPDC control power characteristics are as follows:

- The negative side of the JPDS/JPDM/JPDG/JPDC is grounded at every I/O pack to functional earth (FE). This grounding aids in the conduction of transient noise to earth. Similarly, the negative side of the 28 V dc distribution section of the JPDG is grounded at every I/O pack to FE. It is impossible to float the JPDS/JPDM/JPDG/JPDC power supply.

- The supply voltage provided by the approved power sources can be 28 V ±5%.
- The I/O packs are designed with minimal power disturbance ride-through capability.
- Bulk energy storage is provided by the control power supplies.
- Control power cannot be used for tasks such as contact wetting for field inputs. External connections are controlled and filtered by the terminal board/pack combination.
- JPDS/JPDM/JPDG/JPDC, JPDP, and JPDL support independent control power systems for each controller and associated I/O pack. A redundant control system maintains a separation of control power ensuring system reliability.

P28 System Monitoring

Incoming power is monitored as follows:

- Incoming power is monitored by every I/O pack. An alarm will signal any incoming power that falls below 28 V – 5%. The control can continue to operate with depressed voltage in most cases.
- Depressed voltage effects are dependent on the connected field devices. Determining the voltage required for failure can only be accomplished if the entire system is analyzed.
- A second alarm will be sounded if the control power falls below 16 V. The 16 V alarm can help isolate the source of failure during further analysis.
- JPDS/JPDM/JPDG/JPDC provide voltage monitoring for R, S, and T power buses.
- VMCPS include a dry contact status feedback circuit. This contact will be closed when the power supply is operating normally and will open if it is not. The Mark VIe PDIA, Mark VIeS YDIA, or other contact input pack reads the status signals as a Boolean value. These values are necessary when multiple supplies are connected in parallel for redundant systems. They provide the only way to determine when one supply is not functioning correctly.
- JPDM monitors all fused output branch circuits and indicates a fuse failure.
- JPDC, JPDM, and JPDS power supplies provide four test points, with current limited by 10 kΩ series resistors, used to connect external test equipment.
- IS200JPDG power distribution board provides distribution of 28 V dc (control power) and 48 V/ 24 V dc (wetting power) to other boards within the control system. For both control and wetting power, the JPDG supports dual redundant power supply inputs through external diodes. The JPDG provides fuse protection for all 28 V dc and 24/48 V dc outputs. The voltage at common 28 V bus is monitored by the JPDG, and it supports feedbacks for eight fuses in the 28 V dc distribution section.

P28 Branch Circuit Protection

Branch circuit protection, starting at the terminal board and working back toward the power source, is displayed below:

- Terminal boards supplying output power to field devices provide individual branch circuit protection using a small three terminal regulator. The regulator includes a thermal shut down feature that responds quickly to any overload condition.
- All I/O packs have a fast acting solid-state circuit breaker at the power input point. This breaker ensures that any problem with a connected terminal board can not propagate to other system components.
- The pack circuit breaker is used as a soft-start feature for the pack. Hot-plugging the 28 V dc power into a pack results in a very gradual turn-on of the pack. This ensures no other system component can be affected.
- The JPDL includes a self-recovering fuse coordinated with the wiring to the pack. This device limits current if a short circuit or failure of the protection occurs within the pack. The fuse can protect the wiring, but it doesn't always act fast enough to prevent disturbance of other packs on the same power bus.
- The JPDP board uses only copper conductors and connections. It can carry the same circuits as the JPDL.
- The JPDM board uses individual branch circuit fuses in the positive output to the JPDP board. These fuses can protect wiring and circuit boards between JPDM and the protection on JPDL. Auxiliary outputs are protected by self-resetting devices rated at 1.4 A.
- The JPDS board does not use fuses like JPDM. The board is rated for Class I Division 2 (potentially explosive atmosphere) and the use of fuses is not desired. The JPDS wiring is protected by self-restarting devices rate at 1.4 A.
- Each power supply has current limiting on the output. Current limiting is sufficient to protect the wiring through the JPDP and JPDL when a single 500 W power supply or up to three 150 W supplies are wired together to power a system bus. When JPDS is used for distribution, this current limit protects branch circuit wiring. Multiple supplies, exceeding 500 W, use JPDM or JPDS with external fuses.
- The IS200JPDC provides 1.6 A fuse protection to 26 I/O pack 28 V dc output. The outputs for controller power and the Ethernet switch are not fuse protected.

Distribution component design provides control power branch circuit protection. Specific areas that require monitoring are:

- Supply current limit protecting wiring cannot exceed 500 W. The maximum allowable wire size must be used in the Mate-N-Lok connectors.
- Maximum allowable wire sizes must also include wiring to Ethernet switches and control rack power supplies.
- Parallel or single 28 V supplies, yielding a total capability greater than 500 W, must include branch circuit protection using JPDM, JPDG, or JPDC where the protection is included, or JPDS with added external branch circuit protection.

18.1.3.2 Ac Power Protection

Specific characteristics of ac power distribution components are:

- Ac power distribution components are designed for using a grounded neutral supply.
- By design, the JPDB board can not be damaged if the line and neutral connections are reversed.
- JPDB and JPDA boards have fuses in the line side only. Reversing the connections between line and neutral can eliminate series circuit protection.
- An ac power source similar to US domestic applications could have a 230 V ac winding with the grounded neutral on a center tap. In this case, both neutral connections of the JPDB must be wired.
- The connectors on JPDB are arranged on the board edge in an AC1, AC2, AC1, and AC2 pattern. A wire harness can be created to pick up line connections from two adjacent connectors yielding 230 V ac from dual 115 V ac feeds. This arrangement puts a fuse on both line connections for proper circuit protection.

Note The preceding items do not apply when using a 230 V ac input power source with a grounded neutral connection.

- JPDB is designed with sufficient voltage clearance between the two ac inputs, such as two 208 V or 230 V, from a three-phase source and does not cause voltage clearance problems.
- JPDB uses input filtering to provide a *transients known and controlled* voltage environment for the circuit board. These filters are part of JPDB module and no additional filters are required.
- JPDB delivers 10 A per ac input to both the DACA feed JAF1 and protected branch circuit outputs for a total of 20 A per ac input.
- JPDC has sufficient voltage and current clearance for ac input at JAC, with 300 V rms of voltage clearance and 12.5 A rms current rating supported.
- JPDC supplies 10 A outputs on HAC1 and JAC2 with 450 V peak voltage clearance. Both outputs are fuse protected.

Ac System Monitoring

System monitoring is provided as follows:

- JPDB provides ac voltage magnitude feedback for both input circuits.
- JPDB provides on/off value system feedback for all switched or fused branch circuit outputs.
- JPDA provides a visible LED indicator all four switched/fused branch circuit outputs.
- JPDB provides test point outputs from the two ac inputs for connection of external test equipment. Each test point has a series current limiting 100 kΩ resistor.

Ac Branch Circuit Protection

Caution

Using a slow trip circuit breaker or one rated more than 30 A could cause damage to the board in the event the breaker must be opened.

- JPDB inputs must be protected by a maximum 30 A circuit breaker with normal trip characteristics.
- JPDB is designed for a grounded neutral ac connection. Voltage clearances on the neutral circuit are the same as the line inputs. This prevents board damage from incorrect connections.
- JPDB includes a 5 A fuse on the line side of each output. This fuse was selected to coordinate with the output switch maximum current rating.
- Two un-switched fused outputs have a 5 A fuse while the board artwork and connector are sized to support a 10 A fuse. This was done so all the board fuses have the same value and reduces errors of replacing fuses with the wrong sizes.
- JPDB is designed to deliver 10 A continuously to two DACA modules connected through JAC1 and JPDF.
- JPDA has four switched ac outputs with a fuse in the line side. The board is powered from JPDB through one of the 5 A fused branch circuits. The switch used on JPDA is the same as used on JPDB. Both switches use a 5 A fuse. JPDA uses 15 A fuses. JPDA is connected to JPDB and any occurring fault can open the fuse on JPDB first. JPDB is connected to the system through PPDA. JPDAG2A has empty fuse holders accepting 5 mm X 20 mm fuses and features a black fuse holder cap. JPDAG3A has empty fuse holders accepting a 0.25 in x 1.25 in fuse with a gray fuse holder cap. Both JPDAG2A and JPDAG3A allow the use of a JPDA board with custom fuse rating that is coordinated with a load device limited to less than 5 A.
- JPDA should be used with a power feed of a fused 5 A JPDB feed. JPDA fusing applications should be addressed if other power feeds are used.
- JPDC provides two ac outputs through JAC1 and JAC2. JAC1 is a switched output with a fuse in the line side. JAC2 is not a switched output; however, it does have 10 A fuse in the line side. Therefore, the protection for these ac outputs is provided through a 10 A fuse.

18.1.3.3 125 V dc Power Protection

Characteristics for using a 125 V dc battery as a power source for the PDM are as follows:

- A nominal 125 V dc battery is used as a dc power source for the Mark VIe PDM system.
- The maximum voltage the dc battery can feed to the system is 140 V dc.
- The 125 V dc input to 28 V dc output supply, used to supply control electronics, can function down to 70 V dc. Field devices must be reviewed on an individual basis.

Note The Mark VIe and Mark VIeS control systems can go into over-voltage shutdown should the supplied dc power exceed 145 V dc.

- The 125 V dc battery must be floating with respect to earth. This arrangement eliminates a hard ground on both the positive and negative bus. A single ground fault applied to the system can pass current defined by the centering resistor value and dc bus magnitude. Shift in bus voltage, in respect to earth, can then be detected to indicate a ground fault.
- Ground fault current in a floating battery system is defined by the fixed centering resistance value. The Mark VIe system is classified as Non-hazardous Live because the ground fault current is below dangerous levels. JPDF is designed so that when using provided centering resistors (JP1 in place), the resulting ground resistance is within Non-hazardous Live requirements. When two JPDF boards are wired in parallel for greater current capacity or branch circuit count, only one set of centering resistors should be used.
- When JPDF centering resistors are not used and voltage centering is provided by other means, calculation of centering impedance must allow for the fixed voltage attenuators, 1,500,000 Ω resistors, between the positive bus and earth and the negative bus and earth on JPDF. The resistors provide attenuated bus voltage feedback to PPDA. All other branch circuit feedback signals use isolating devices that do not provide a path to ground.
- JPDF applications with dc input filtering yield a transients known and controlled environment for the board voltage clearance class. Required filtering is provided as part of the JPDF module. No additional input filters are needed.
- The DACA module is designed to coordinate power delivery with a 125 V dc battery. One or two DACA modules, powered by a reliable ac power source, could be used to provide backup power if battery failure occurs.

- JPDC receives 125 V dc power from battery through JD1 and JD2. These inputs are diode ORed on JPDC. This becomes ORed with 125 V dc from the DACA module, through a diode on the DACA module, to form a 125 V dc bus PDC. Total current through this dc bus should not exceed 20 A. All JPDC output voltage feedbacks are attenuated and feedback is received in the PPDA.
  - Ground fault detection is provided through 85K Ω resistance when JP2 is installed.
  - JPDC provides 125 V dc outputs with 10 A fuse protection and toggle switches to external power supplies through J1R, J1S, and J1T.
  - JPDC provides three additional 125 V dc outputs are provided with 10 A fuse protection and toggle switches providing power through J7A, J7B and J7C.
  - Outputs for TBCI J8A, J8B, and J8C are fuse protected and do not have any toggle switches. A 22 W external resistor is required to limit the output power.

125 V dc System Monitoring

Monitoring for the 125 V dc power systems is as follows:

- JPDC and JPDF provide voltage magnitude feedback through PPDA for positive and negative dc voltage with respect to earth. The difference between the two signals equals the bus magnitude. The difference between the two bus voltage magnitudes could be used to detect a system ground fault in a floating system.
- JPDF includes additional circuitry on the bus voltage feedback that detects ac current. PPDA can issue an alarm when a JPDF board displays more 30 V ac on the dc bus.
- JPDF has a visible LED for each switched and fused branch circuit outlet.
- JPDC has visible LEDs for the battery inputs to the board.

125 V dc Branch Circuit Protection

Branch circuit protection for the 125 V dc power system is as follows:

- The JPDF module has a 30 A dc circuit breaker in the input power feed to ensure correct input power protection.
- JPDF has 5 A fuses on both sides of the J1 R, S, and T output branch circuits. The fuses coordinate with the rating of the switches provided with these outputs.
- JPDF has 5 A fuses on both sides of the J7 X, Y, and Z output branch circuits. The fuses coordinate with the rating of the switches provided with these outputs. There is a series 1 Ω resistor in each leg, with the same rating as the switches, provided with these outputs.
- JPDF has 12 A fuses on both sides of the J8A and J8B output branch circuits. The connector uses 12 AWG wire.
- JPDF has 3 A fuses on both sides of the J12 output branch circuit. The J12 circuit has 22 Ω resistors in series limiting fault current to [ ] V dc/44 A.
- JPDD has six switched and fused dc outputs (12 fuses of type depending on *board revision*). The board is powered by JPDF. The board is fed by a 5 A branch circuit from JPDF. JPDF is visible to the system through PPDA. A fault on the JPDF circuit cannot result in opening the fuses on JPDD.
- JPDC has six switched and 10 A fused dc battery outputs (three are fast blow for use with TRLY circuits and three are slow blow for use with dc/dc circuits), and three additional fused current limited dc battery outputs. The battery outputs are all fed from two separate battery inputs and the DACA input using diode-OR circuitry.

18.1.3.4 24/48 V dc Power Protection

Characteristics of the 24 V dc power protection system are as follows:

- 24 V dc power distribution is a utility system using a 24 V nominal dc battery. A typical ac system uses one or more dc power supplies for contact wetting and relay outputs.
- The maximum allowable battery voltage is 36 V dc. The Mark VIe and Mark VIeS controllers can initiate over-voltage shutdown when the battery output voltage exceeds the allowable limit.
- The 24 V dc input to 28 V dc output powers Mark VIe and Mark VIeS control electronics.
- The 24 V dc battery has no hard ground on either the positive or the negative dc bus. A high resistance from the positive and negative dc is applied to earth to center the bus on earth. A single ground fault applied to this system can pass current defined by centering resistor value and dc bus magnitude. The shift in voltage, with respect to earth, can be detected and signal the presence of a ground fault.
- The JPDE board provides centering resistors selected by using JP1. In the event the battery has external centering resistors on the battery bus, JP1 could be eliminated to avoid higher ground fault currents.
- The JPDE board is designed application using dc input filtering. Additional input filters are not needed.
- The IS200JPDG power distribution board provides distribution of 28 V dc (control power) and 48 V/ 24 V dc (wetting power) to other boards within the control system. For both control and wetting power, the JPDG supports dual redundant power supply inputs through external diodes. The JPDG provides fuse protection for all 28 V dc and 24/48 V dc outputs. The voltage at common 24/48 V bus is monitored by the JPDG, and it supports feedbacks for 14 fuses in the 24/48 V dc distribution section.

For the 48 V dc power protection system, the JPDE may be configured to operate correctly using 48 V dc input power for power distribution.

18.2 PPDA Power Distribution System Feedback

PDM
IS220PPDAH1B
Fault ACP AC2 App3 24P 24G App1 125D 125V TSrc RSrc PbS
JPDR ACA AC1 App2 24D 24V 125P 125G Aux SSrc PbT PbH
ATTN PWR
Tx/Rx LINK
ENET1
Tx/Rx LINK
ENET2
336A5026A0P1A

The Power Distribution System Feedback (PPDA) I/O pack produces system feedback signals for power bus voltages, branch circuit status, ground fault detection, and bulk power supply health from the connected core distribution board(s). The I/O pack accepts inputs from up to a maximum of six power distribution boards or up to six sets of feedback signals. It conditions the board feedback signals and provides a dual redundant Ethernet interface to the Mark VIe or Mark VIeS controllers. The PPDA feedback is structured to be plug and play, using electronic IDs to determine the power distribution boards wired into it. This information is then used to populate the IONet output providing correct feedback from connected boards.

The PPDA I/O pack is hosted by the JPDS, JPDM, JPDG, or JPDC 28 V dc control power distribution board. Additional boards are connected using 50-pin ribbon cable jumpers that are wired pin 1 to pin 1. Each board contributes one feedback group to the PPDA. The PPDA I/O pack is compatible with the feedback signals created by the JPDB, JPDE, and JPDF.

The following are PPDA I/O pack versions and minimum software requirements:

- The PPDAH1A contains a BPPB processor board. These processors are reaching end of life. With ControlST* software V04.07 and later, the PPDAH1A can be replaced with a PPDAH1B.
- The PPPDAH1B contains BPPC processor board that is supported in the ControlST software V04.07 and later.
- With PPDAH1B and ControlST software V05.02 or later, the PPDA can be used to send power distribution feedback data to the Mark VIeS Safety controller.
- With ControlST V5.02 or later, the PPDA no longer supports a board-mounted accelerometer. Be aware if upgrading from a previous version, the ToolboxST application does not identify existing use of connected accelerometer variables.

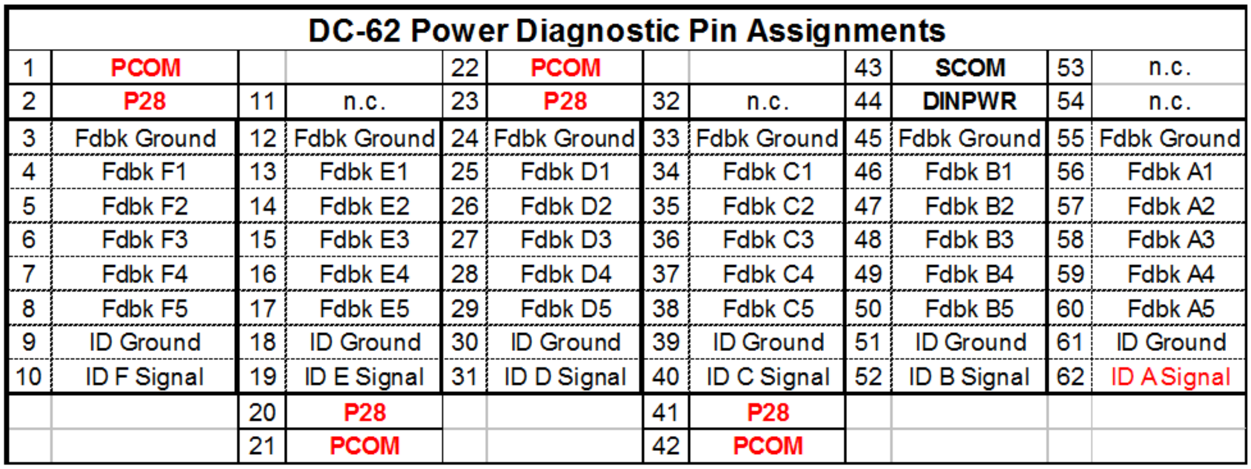
18.2.1 Compatibility

At the heart of the core PDM is the PPDA I/O pack. This I/O pack is designed to accept inputs from up to six different power distribution boards, condition the signals, and provide a dual redundant Ethernet interface to the controllers. The feedback is structured to be *plug and play* meaning the PPDA is able to check the power distribution boards that are wired into it using electronic IDs. It uses this information along with ToolboxST configuration to populate the IONet signal space output with the correct feedback signals from connected boards.

The PPDA I/O pack is hosted by the JPDS, JPDM, JPDG, or JPDC 28 V dc control power boards on the Mark* VIe control Power Distribution Module (PDM). It is compatible with the feedback signals created by JPDB, JPDE, and JPDF.

18.2.2 Signal Input

The PPDA I/O pack features a 62–pin connector to the host board. It is helpful to review the pin assignments on that connector:



DC-62 Power Diagnostic Pin Assignments

1	**PCOM**			22	**PCOM**			43	**SCOM**	53	n.c.
2	**P28**	11	n.c.	23	**P28**	32	n.c.	44	**DINPWR**	54	n.c.
3	Fdbk Ground	12	Fdbk Ground	24	Fdbk Ground	33	Fdbk Ground	45	Fdbk Ground	55	Fdbk Ground
4	Fdbk F1	13	Fdbk E1	25	Fdbk D1	34	Fdbk C1	46	Fdbk B1	56	Fdbk A1
5	Fdbk F2	14	Fdbk E2	26	Fdbk D2	35	Fdbk C2	47	Fdbk B2	57	Fdbk A2
6	Fdbk F3	15	Fdbk E3	27	Fdbk D3	36	Fdbk C3	48	Fdbk B3	58	Fdbk A3
7	Fdbk F4	16	Fdbk E4	28	Fdbk D4	37	Fdbk C4	49	Fdbk B4	59	Fdbk A4
8	Fdbk F5	17	Fdbk E5	29	Fdbk D5	38	Fdbk C5	50	Fdbk B5	60	Fdbk A5
9	ID Ground	18	ID Ground	30	ID Ground	39	ID Ground	51	ID Ground	61	ID Ground
10	ID F Signal	19	ID E Signal	31	ID D Signal	40	ID C Signal	52	ID B Signal	62	ID A Signal
		20	**P28**			41	**P28**				
		21	**PCOM**			42	**PCOM**				

The signals shown in red are predefined for all I/O packs that use the 62–pin connector. This ensures that if a I/O pack is mounted to an incorrect board, there will not be power or ID wiring problems. The diagram arrangement displays six clear groups of signals. Each group consists of a feedback ground reference, five analog signals, and two wires for an ID line. Each group originates on a JPDx board with each board type providing a different set of signal definitions. On the PPDA each analog signal is sensed differentially with respect to the group *Fdbk_Ground* providing substantial immunity to common mode noise and differences between the I/O pack ground (FE) and the JPDx board ground (sometimes PE). The ID line for each group allows the PPDA to identify the board that is driving the signals of each group and respond accordingly. The PPDA provides a modest amount of output power using DINPWR and SCOM to support boards where a fully passive feedback circuit is not possible. This power passes straight through the ribbon cable to all connected boards.

18.2.3 PPDA LED Control

The PPDA I/O pack includes a full set of 24 LEDs to indicate power supply status. The function of most is fixed in firmware, while four provide an opportunity for application specific indications.

LED	I/O Pack Text	Signal Content	Firmware
1	Pb R	Pbus R is in regulation	Magnitude is 28 ±5%
2	Pb S	Pbus S is in regulation (not used on JPDG)	Magnitude is 28 ±5%
3	Pb T	Pbus T is in regulation (not used on JPDG)	Magnitude is 28 ±5%
4	RSrc	All R Pbus Sources OK	R PBUS power supply status switch OK
5	SSrc	All S Pbus Sources OK	S PBUS power supply status switch OK
6	TSrc	All T Pbus Sources OK (not used on JPDG)	T PBUS power supply status switch OK
7	Aux	Aux 28 outputs OK	All three aux boolean OK
8	125V	125 V battery volts OK	Magnitude is 125 V ± configurable
9	125G	125 V battery floating	Volts centered within ± V configurable
10	125D	125 V JPDD feeds OK	Output to JPDD boolean values OK
11	125P	125 V Pbus feeds OK	Booleans on pwr supply feeds OK
12	App1	Application driven	Driven by signal space input boolean
13	24V	24 V battery volts OK	Magnitude is 24 V ± configurable
14	24G	24 V battery floating	Volts centered within ± V configurable
15	24D	24 V JPDD feeds OK	Output to JPDD boolean values OK
16	24P	24 V Pbus feeds OK	Booleans on pwr supply feeds OK
17	App2	Application driven	Driven by signal space input boolean
18	App3	Application driven	Driven by signal space input boolean
19	AC 1	AC input 1 is OK	Magnitude is OK, config range
20	AC 2	AC input 2 is OK	Magnitude is OK, config range
21	AC A	AC1 Outputs OK	JPDB AC1 output boolean values OK
22	AC P	AC2 Outputs OK	JPDB AC2 output boolean values OK
23	JPDR	JPDR Src. Select OK	Status feedback from JPDR is OK
24	Fault	Application driven	Driven by signal space input boolean

Unless specified, each LED is turned on to indicate OK operation. In order to keep the LED operation simple, the LEDs only reflect the status of the first board of any type in the system. For example, if there are two JPDF boards used, the LEDs only indicate the status of the first board. The application driven LEDs are used if there is a desire to visually indicate some aspect of a dual–board arrangement.

Using the LED number as a reference, a detailed description of the operation of each LED follows:

1. This LED indicates that the PBUS power on JPDS/M that feeds the R control is within 28 V ±5%. In the case where two JPDS/M boards are used the LED reflects the status of the board that holds the PPDA I/O pack. Since JPDS/M is the host for the PPDA this LED should always be functional.
2. This is the same as LED #1, except it uses the magnitude of the S power bus.
3. This is the same as LED #1, except it uses the magnitude of the T power bus.
4. This LED is driven from the status feedback switch that may be wired into the JPDS/M R power bus power supply input connector. The sense of the LED is to turn it on when the switch is closed.
5. This is the same as LED #4, except it uses the switches from the S power supplies.
6. This is the same as LED #4, except it uses the switches from the T power supplies.
7. The JPDS/M has three Aux outputs protected by self-resetting fuses. This LED indicates that all three outputs, JAR, JAS, and JAT, are providing output voltage.
8. The JPDF creates a high-reliability 125 V dc bus using a battery input and two optional DACA modules. This LED indicates that the 125 V is above an adjustable threshold that indicates sufficient voltage. 125 V is read as the difference between the positive and negative dc voltage inputs.
9. The JPDF 125 V dc is typically centered on earth such that each voltage input indicates about of the total dc volts. If there is a ground on the dc system most of the voltage will appear on one or the other dc signal. This LED is turned on when the dc is centered within a specified threshold.
10. This LED is on when JPDF J8A, J8B, and J12 outputs are indicating a valid output.
11. This LED is on when JPDF J1R, J1S, and J1T outputs are indicating a valid output.
12. This LED is driven by a signal space input to the PPDA from application code.
13. The JPDE creates a high-reliability 24 V or 48 V dc bus using a battery input and other sources. This LED indicates that the bus is above a specified threshold that indicates sufficient voltage. Voltage is read as the difference between the positive and negative dc voltage inputs.
14. The JPDE dc voltage is typically centered on earth such that each voltage input indicates about half of the total dc volts. If there is a ground on the dc system most of the voltage will appear on one or the other dc signal. This LED is turned on when the dc is centered within a specified threshold.
15. This LED indicates that JPDE connectors JS1, JS2, and JS3 have voltage present.
16. This LED indicates that JPDE connectors JFA, JFB, and JFC have voltage present.
17. This LED is driven by a signal space input to the PPDA from application code.
18. This LED is driven by a signal space input to the PPDA from application code.
19. JPDB FDBK_A1 indicates the magnitude of the ac 1 input. A threshold is provided as part of PPDA configuration. If the ac 1 input is above the threshold voltage then this LED should be turned on.
20. JPDB FDBK_A2 indicates the magnitude of the ac 2 input. A threshold is provided as part of PPDA configuration. Note that this is not the same threshold as used for A1. If the ac 2 input is above the threshold voltage then this LED is turned on.
21. This LED is on when the four outputs associated with ac 1 are indicating voltage is present. Includes JAC1, JAC3, JAC5, and JA1.

22. This LED is on when the four outputs associated with ac 2 are indicating voltage is present. Includes JAC2, JAC4, JAC6, and JA2.

23. Placeholder for future ac source selector status indication.

24. This LED is driven by a signal space input to the PPDA from application code.

18.2.4 Installation

Caution

In 240 V ac applications, do not inadvertently cross-connect the 240 V ac and the dc voltages. The peak voltage will exceed the Transorb rating, resulting in a failure.

Most ac supplies operate with a grounded neutral, and if an inadvertent connection between the 125 V dc and the ac voltage is created, the sum of the ac peak voltage and the 125 V dc is applied to Transorbs connected between dc and ground. However, in 120 V ac applications, the Transorb rating can withstand the peak voltage without causing a failure.

➢ **To install the PPDA I/O pack**

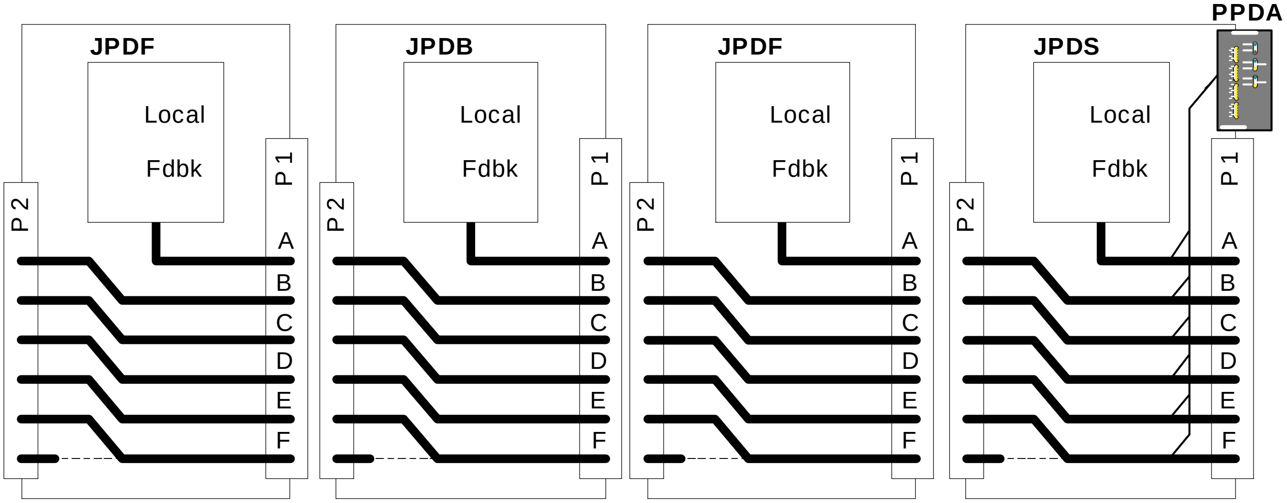
1. Securely mount the desired terminal board.
2. Directly plug the PPDA I/O pack into the JA1 terminal board connectors. The PPDA I/O pack mounts on a JPDG, JPDS, JPDM, or JPDC 28 V dc control power distribution board. Refer to the section, *Valid PDM Core Board Combinations*.
3. Mechanically secure the I/O pack using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right-angle force applied to the DC-62 pin connector between the I/O pack and the terminal board. The adjustment should only be required once in the service life of the product.
4. Plug in one or two Ethernet cables depending on the system configuration. The I/O pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
5. Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to remove power from the cable before plugging it in because the I/O pack has inherent soft-start capability that controls current inrush on power application.
6. Connect ribbon cables from connector P2 on JPDG, JPDS, JPDM, or JPDC to daisy chain other core boards feeding information to PPDA.

Note Additional power distribution feedback signals may be brought into the PPDA I/O pack through the P2 connector on the host board. The P1 connector is never used on a board that hosts the PPDA I/O pack, PPDA must always be at the end of the feedback cable daisy chain.

7. Use the ToolboxST application to configure the I/O pack as necessary. From the Component Editor, press F1 for help.

18.2.4.1 Signal Routing

The PPDA I/O pack is mounted to either a JPDG, JPDS, JPDM, or a JPDC board. Additional boards are connected using 50-pin ribbon cable jumpers that are wired pin 1 to pin 1. Each board contributes one feedback group to PPDA. This connection passes through up to five previous boards. The following figure displays this hookup.



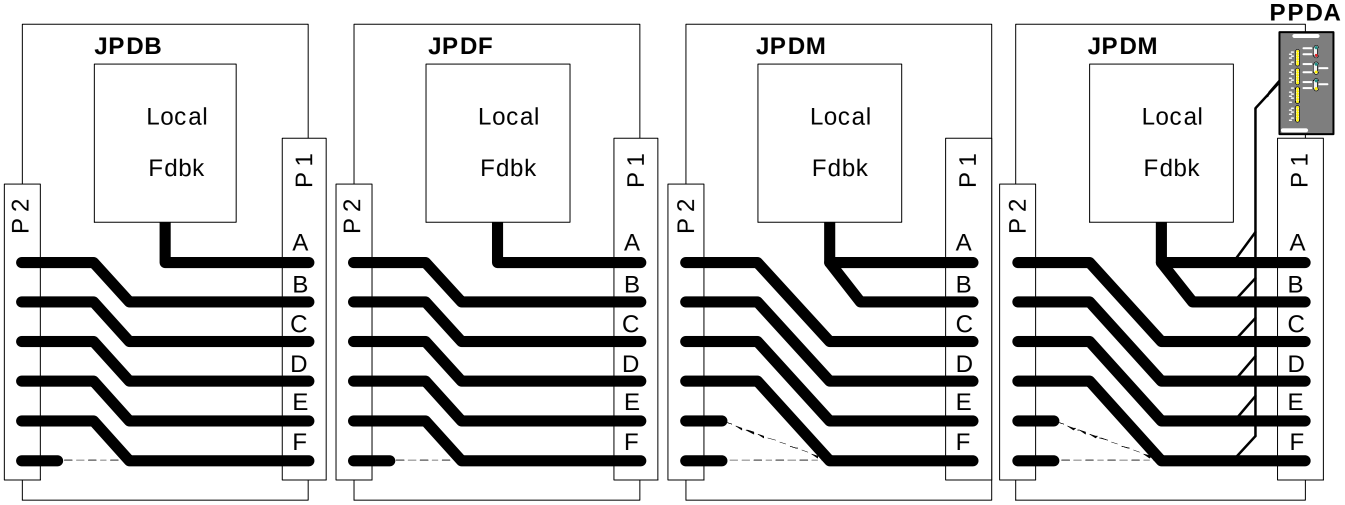
PPDA Basic Hookup Diagram

In the above figure, feedback groups are displayed as bold lines and connectors P1 and P2 of each board are displayed. From right to left, the JPDS board hosts the PPDA I/O pack and hookups are as follows:

- Local feedback from JDPS is on signal group A
- Feedback from JPDF is on signal group B
- Feedback from JPDB is on signal group C
- An additional JPDF would use signal group D
- An additional board would use signal group E

Note The maximum length of the FRC is supported. If one end of the FRC is open, the PPDA may read incorrect values.

JPDM uses two sets of feedback signals due to the large number of feedback lines from that board. JPDM does support the use of two boards. The arrangement would look like the following figure.



PPDA Wiring Using Two JPDM Boards

18.2.5 Operation

The following features are common to the distributed I/O modules:

- *BPPx Processor*
- *Processor LEDs*
- *Power Management*
- *ID Line*
- *I/O Module Common Diagnostic Alarms*

18.2.6 Specifications

Item	**PPDA Specification**
Feedback Signals	The PPDA can read feedback signals from different power distribution boards like JPDS, JPDM, JPDC, JPDG, JPDB, JPDE, and JPDF.
Number of Boards	Accepts inputs from up to a maximum of six power distribution boards or up to six sets of feedback signals
JPDS	It uses one set of feedback signals. If JPDS is used in the system, a maximum of five other boards can be supported.
JPDM	It uses two sets of feedback signals due to the large number of feedback lines from that board. If JPDM is used in the system, a maximum of four other boards can be connected.
JPDC	It uses two sets of feedback signals. If JPDC is used in the system, a maximum of four other boards can be supported.
JPDG	It uses three sets of feedback signals. If JPDG is used in the system, a maximum of three other boards can be supported.
Number of Channels	5 channels per feedback set, total 30 channels for six feedback sets
Input Converter Resolution	16 bit analog-to-digital converter
Power Consumption	5.3 W typical, 6.2 W worst case
Size	8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in x 1.65 in x 4.78 in)
Technology	Surface mount
Ambient Rating for Enclosure Design†	PPDAH1B is rated from -40 to 70ºC (-40 to 158 ºF) PPDAH1A is rated from -30 to 65ºC (-22 to 149 ºF)

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

18.2.7 Diagnostics

The PPDA performs the following self-diagnostic tests:

- A power-up self-test including checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition card, and processor card confirming the hardware set matches, followed by a check confirming the application code loaded from flash memory is correct for the hardware set
- The analog input hardware includes precision reference voltages in each scan. Measured values are compared against expected values and are used to confirm health of the A/D converter circuits.
- Details of the individual diagnostics are available from the ToolboxST application. The diagnostic signals are individually latched, and then reset with the RESET_DIA signal if they go healthy.

18.2.7.1 Power Distribution LEDs

LED	Color	Description	Variable
Pb R	Yellow	Pbus R is in Regulation	Pbus_R_LED
Pb S	Yellow	Pbus S is in Regulation (not used on JPDG)	Pbus_S_LED
Pb T	Yellow	Pbus T is in Regulation (not used on JPDG)	Pbus_T_LED
RSrc	Yellow	All R Pbus Sources OK	Src_R_LED
SSrc	Yellow	All S Pbus Sources OK	Src_S_LED
TSrc	Yellow	All T Pbus Sources OK (not used on JPDG)	Src_T_LED
Aux	Yellow	Aux 28 outputs OK	Aux_LED
125V	Yellow	125 V battery volts OK	Batt_125V_LED
125G	Yellow	125 V battery floating	Batt_125G_LED
125D	Yellow	125 V JPDD feeds OK	JPDD_125D_LED
125P	Yellow	125 V Pbus feeds OK	Pbus_125P_LED
App1	Yellow	Application driven	App_1_LED
24V	Yellow	24/48 V battery volts OK	Batt_24V_LED
24G	Yellow	24/48 V battery floating	Batt_24G_LED
24D	Yellow	24/48 V JPDD feeds OK	JPDD_24D_LED
24P	Yellow	24/48 V Pbus feeds OK	Pbus_24P_LED
App2	Yellow	Application driven	App_2_LED
App3	Yellow	Application driven	App_3_LED
AC1	Yellow	Ac input 1 OK	AC_Input1_LED
AC2	Yellow	Ac input 2 OK	AC_Input2_LED
ACA	Yellow	Ac JPDA feeds OK	AC_JPDA_LED
ACP	Yellow	Ac Pbus feeds OK	AC_Pbus_LED
Fault	Red	Fault Led - Application driven	Fault_LED

18.2.8 Configuration

The PPDA I/O pack uses configuration values for operation with desired PDM boards. The ToolboxST application provides the correct options for the version of PDM hardware in use in a given system. A brief summary of the types of configurations encountered are as follows:

- JPDB: The nominal voltage magnitude is selected, the magnitude tolerance specified, and a correction factor for neutral voltage is provided for each of the two ac buses. Each of the switched branch circuit fuse status can be turned on or off.
- JPDC:
  - The PPDA needs to know if P28R, S, and T can be present in a system. If it is indicated that one is not present, the low voltage diagnostics for that power bus can be turned off.
  - The 125 V bus magnitude and centering tolerance can be configured, and the diagnostic associated with switched branch circuit fuse status can be turned on or off.
  - For ac input, the nominal voltage magnitude is selected, the magnitude tolerance specified, and a correction factor for neutral voltage is provided for the ac bus. Each of the switched branch circuit fuse status can be turned on or off.
- JPDG:
  - P28 feedback and diagnostics can be turned on/off. Keeping them on is recommended.
  - The 24/48 V bus magnitude and centering tolerance can be configured, and the diagnostic associated with switched branch circuit fuse status can be turned on or off.
- JPDE: The 24 V bus magnitude and centering tolerance can be configured, and the diagnostic associated with switched branch circuit fuse status can be turned on or off.
- JPDF: The 125 V bus magnitude and centering tolerance can be configured, and the diagnostic associated with switched branch circuit fuse status can be turned on or off.
- JPDS / JPDM: The PPDA needs to know if P28R, S, and T can be present in a system. If it is indicated that one is not present, the low voltage diagnostics for that power bus can be turned off.
- PPDA: The I/O pack needs to know what PDM boards are in the diagnostic daisy chain.

Note If two JPDM or JPDS boards are present, it is recommended that one of the boards' inputs be disabled.

18.2.8.1 Variables

Variable	Description	Direction	Type
L3DIAG_PPDA_R	I/O Diagnostic indication	Input	BOOL
LINK_OK_PPDA_R	I/O Link Okay indication	Input	BOOL
ATTN_PPDA_R	I/O Attention indication	Input	BOOL
PS18V_PPDA_R	I/O 18 V Power Supply indication	Input	BOOL
PS28V_PPDA_R	I/O 28 V Power Supply indication	Input	BOOL
IOPackTmpr_R	I/O pack temperature (° F)	AnalogInput	REAL
Pbus_R_LED	Pbus R is in Regulation	Input	BOOL
Pbus_S_LED	Pbus S is in regulation	Input	BOOL
Pbus_T_LED	Pbus T is in regulation	Input	BOOL
Src_R_LED	All R Pbus sources OK	Input	BOOL
Src_S_LED	All S Pbus sources OK	Input	BOOL
Src_T_LED	All T Pbus sources OK	Input	BOOL
Aux_LED	Aux 28 outputs OK	Input	BOOL
Batt_125V_LED	125 V battery volts OK	Input	BOOL
Batt_125G_LED	125 V battery floating	Input	BOOL
JPDD_125D_LED	125 V JPDD feeds OK	Input	BOOL
Pbus_125P_LED	125 V Pbus feeds OK	Input	BOOL
Batt_24V_LED	24 V battery volts OK	Input	BOOL
Batt_24G_LED	24 V battery floating	Input	BOOL
JPDD_24D_LED	24V JPDD feeds OK	Input	BOOL
Pbus_24P_LED	24 V Pbus feeds OK	Input	BOOL
AC_Input1_LED	AC input 1 OK	Input	BOOL
AC_Input2_LED	AC input 2 OK	Input	BOOL
AC_JPDA_LED	AC JPDA feeds OK	Input	BOOL
AC_Pbus_LED	AC Pbus feeds OK	Input	BOOL
JPDR_LED	JPDR source select OK	Input	BOOL
App_1_LED	Application driven	Output	BOOL
App_2_LED	Application driven	Output	BOOL
App_3_LED	Application driven	Output	BOOL
Fault_LED	Fault Led - application driven	Output	BOOL
SrcSel_Stat_1	JPDR #1	Input	BOOL

18.2.8.2 JPDS/M Inputs

Parameter	Description	Choices
PS28vEnable	PS 28 V feedback enable; Enable – Enables feedback Disable – Disables feedback and diagnostics NoDryCnt – Enables feedback, but disables dry contact diagnostics	Enable, Disable, NoDryCnt

Variable**	Description	Direction	Type
PS28vStat_x_y	PS 28 V feedback from Pbus x input	AnalogInput	REAL
** x = R, S, T and y = 1, 2			

18.2.8.3 JPDS Contact/Fuse

Variable**	Description	Direction	Type
DryCntStat_x_y	Pbus x dry contact status (connector Jx)	Input	BOOL
AuxFuseStat_x_y	Pbus x fuse status (connector JAx)	Input	BOOL
** x = R, S, T and y = 1, 2			

18.2.8.4 JPDM Contact/Fuse

Variable**	Description	Direction	Type
DryCntStat_x_y	Pbus x dry contact status (connector Jx)	Input	BOOL
AuxFuseStat_x_y	Pbus x fuse status (connector JAx)	Input	BOOL
FU1_Stat_y	Fuse FU1 status (connector JCR)	Input	BOOL
↓	↓	↓	↓
FU12_Stat_y	Fuse FU12 status (Connector J3)	Input	BOOL
** x = R, S, T and y = 1, 2			

18.2.8.5 JPDC Inputs

Parameter	Description	Choices
PS28vEnable	PS 28 V feedback enable; Enable – Enables feedback Disable – Disables feedback and diagnostics NoDryCnt – Enables feedback, but disables dry contact diagnostics Applicable only to PS28vStat_x_1, where x= R, S, T	Enable, Disable, NoDryCnt
InputDiagEnab	DC or AC volt diagnostics enable Applicable only to 125VFdbkMag_1 and AC_Fdbk1_Volt_1	Enable, Disable
DC_125v_Trig_Volt	DC 125 V fault trigger voltage Applicable only to DC_125VFdbkMag_1	42 to 500
Gnd_Mag_Trig_Volt	Ground magnitude fault trigger voltage Applicable only to Gnd_125VFdbkMag_1	5 to 500
ACFdbkInVoltage	AC feedback input voltage Applicable only to AC_Fdbk1_Volt_1	100 to 250
ACFdbkInTol	Percentage variation tolerance on AC input Applicable only to AC_Fdbk1_Volt_1	0pct, 5pct, 10pct, 20pct

Variable**	Description	Direction	Type
PS28vStat_x_1	Main JPDC - PS 28 V feedback from Pbus x input	AnalogInput	REAL
DC_125VFdbkMag_1	Main JPDC - DC 125 V magnitude	AnalogInput	REAL
Gnd_125VFdbkMag_1	Main JPDC - DC 125 V ground magnitude	AnalogInput	REAL
AC_Fdbk1_Volt_1	Main JPDC - AC 100 to 250 V Feedback input Voltage	AnalogInput	REAL
** x = R, S, T			

18.2.8.6 JPDC Fuse/Dry Contacts

Parameter	Description	Choices
InputDiagEnab	Option to suppress fuse diagnostic; Fuse diagnostics are also suppressed if source on which they exist are unhealthy due to failure of low limit threshold on them.	Enable, Disable

Variable	Description	Direction	Type
FU71_FU72_Stat_1	Main JPDC - FU71/FU72 fuse status (connector J7A)	Input	BOOL
FU73_FU74_Stat_1	Main JPDC - FU73/FU74 fuse status (connector J7B)	Input	BOOL
FU75_FU76_Stat_1	Main JPDC - FU75/FU76 fuse status (connector J7C)	Input	BOOL
FU1R_FU2R_Stat_1	Main JPDC - FU1R/FU2R fuse status (connector J1R)	Input	BOOL
FU1S_FU2S_Stat_1	Main JPDC - FU1S/FU2S fuse status (connector J1S)	Input	BOOL
FU1T_FU2T_Stat_1	Main JPDC - FU1T/FU2T fuse status (connector J1T)	Input	BOOL
FU_AC1_Stat_1	Main JPDC - FUAC1 fuse Status (connector JA1)	Input	BOOL
FU_AC2_Stat_1	Main JPDC - FUAC2 fuse status (connector JA2)	Input	BOOL
BAT_Stat_1	Main JPDC - battery status	Input	BOOL
DryCntStat_R_1	Main JPDC - Pbus R dry contact status (connector JR)	Input	BOOL
DryCntStat_S_1	Main JPDC - Pbus S dry contact status (connector JS)	Input	BOOL
DryCntStat_T_1	Main JPDC - Pbus T dry contact status (connector JT)	Input	BOOL

18.2.8.7 JPDG Inputs

Parameter	Description	Choices
InputDiagEnable	DC or AC volt diagnostics enable Applicable only to DC_24VFdbkMag, AC_Fdbk1_Volt_#	Enable, Disable
PS28vEnable	PS 28 V feedback enable; Enable – Enables feedback Disable – Disables feedback and diagnostics NoDryCnt – Enables feedback, but disables dry contact diagnostics Applicable only to PS28vStat	Enable, Disable, NoDryCnt
DC_24v_Trig_Volt	DC 24 V fault trigger voltage Applicable only to DC_24VFdbkMag	10 to 60
Gnd_Mag_Trig_Volt	Ground magnitude fault trigger voltage Applicable only to DC_24VGnd_FdbkMag	1 to 30
ACFdbkInVoltage	AC feedback input voltage Applicable only to AC_Fdbk1_Volt_#	100 to 250 V
ACFdbkInTol	AC feedback tolerance Applicable only to AC_Fdbk1_Volt_#	0pct, 5pct, 10pct, 20pct

Variable	Description	Direction	Type
PS28vStat	Main JPDG - PS 28 V feedback from Pbus R input	AnalogInput	REAL
DC_24VFdbkMag	JPDG - DC 24V/48 V magnitude	AnalogInput	REAL
DC_24VGnd_FdbkMag	JPDG - ground feedback magnitude	AnalogInput	REAL
AC_Fdbk1_Volt_1	Main JPDG - AC 115 to 250 V feedback input voltage	AnalogInput	REAL
AC_Fdbk1_Volt_2	Main JPDG - AC 115 to 250 V feedback input voltage	AnalogInput	REAL

18.2.8.8 JPDG Fuse/Dry Contacts

Variable	Description	Direction	Type
FU1_Stat	Main JPDG - FU1 fuse status (connector J1)	Input	BOOL
FU2_Stat	Main JPDG - FU2 fuse status (connector J1)	Input	BOOL
FU3_Stat	Main JPDG - FU3 fuse status (connector J2)	Input	BOOL
FU4_Stat	Main JPDG - FU4 fuse status (connector J2)	Input	BOOL
FU5_Stat	Main JPDG - FU5 fuse status (connector J3)	Input	BOOL
FU6_Stat	Main JPDG - FU6 fuse status (connector J3)	Input	BOOL
FU7_Stat	Main JPDG - FU7 fuse status (connector J4)	Input	BOOL
FU8_Stat	Main JPDG - FU8 fuse status (connector J4)	Input	BOOL
DryCntStat_1	Main JPDG - P28 V bus dry contact - 1 status	Input	BOOL
DryCntStat_2	Main JPDG - P28 V bus dry contact - 2 status	Input	BOOL
FU10_FU11_Stat	Main JPDG - FU10/FU11 fuse status (connector JFA)	Input	BOOL
FU12_FU13_Stat	Main JPDG - FU12/FU13 fuse status (connector JFB)	Input	BOOL
FU14_FU15_Stat	Main JPDG - FU14/FU15 fuse status (connector JFC)	Input	BOOL
FU16_FU17_Stat	Main JPDG - FU16/FU17 fuse status (connector JFD)	Input	BOOL
FU18_FU19_Stat	Main JPDG - FU18/FU19 fuse Status (connector JFE)	Input	BOOL
FU20_FU21_Stat	Main JPDG - FU20/FU21 fuse status (connector JFF)	Input	BOOL
FU22_FU23_Stat	Main JPDG - FU22/FU23 fuse status (connector JFG)	Input	BOOL
DryCntStat_3	Main JPDG - P24/48 V bus dry contact - 1 status	Input	BOOL
DryCntStat_4	Main JPDG - P24/48 V dry contact - 2 status	Input	BOOL

18.2.8.9 JPDF Inputs

Parameter	Description	Choices
InputDiagEnab	Input diagnostic enable	Enable, Disable
DC_125v_Trig_Volt	DC 125 V fault trigger voltage	42 to 500

Variable**	Description	Direction	Type
DC_125VFdbkMag_x	JPDF x - DC 125 V magnitude	AnalogInput	REAL
** x = 1, 2			

18.2.8.10 JPDF Gnd Volts

Parameter	Description	Choices
Gnd_Mag_Trig_Volt	Ground magnitude fault trigger voltage	5 to 500

Variable**	Description	Direction	Type
Gnd_FdbkMag_x	JPDF x - ground feedback magnitude	AnalogInput	REAL
** x = 1, 2			

18.2.8.11 JPDF Fuse

Parameter	Description	Choices
FuseDiag	Enable/Disable Fuse Diagnostic alarm	Enable, Disable

Variable**	Description	Direction	Type
FU1R_FU2R_Stat_x	JPDF x - FU1R/FU2R fuse status (connector J1R)	Input	BOOL
FU1S_FU2S_Stat_x	JPDF x - FU1S/FU2S fuse status (connector J1S)	Input	BOOL
FU1T_FU2T_Stat_x	JPDF x - FU1T/FU2T fuse status (connector J1T)	Input	BOOL
FU71_FU72_Stat_x	JPDF x - FU71/FU72 fuse status (connector J7X)	Input	BOOL
FU73_FU74_Stat_x	JPDF x - FU73/FU74 fuse status (connector J7Y)	Input	BOOL
FU75_FU76_Stat_x	JPDF x - FU75/FU76 fuse status (connector J7Z)	Input	BOOL
FU81_FU82_Stat_x	JPDF x - FU81/FU82 fuse status (connector J8A)	Input	BOOL
FU83_FU84_Stat_x	JPDF x - FU83/FU84 fuse status (connector J8B)	Input	BOOL
FU12_FU13_Stat_x	JPDF x - FU12/FU13 fuse status (connector J12)	Input	BOOL
** x = 1, 2			

18.2.8.12 JPDE Inputs

Parameter	Description	Choices
InputDiagEnab	Input diagnostic enable	Enable, Disable
DC_24v_Trig_Volt	DC 24/48 V fault trigger voltage	10 to 60

Variable**	Description	Direction	Type
DC_24VFdbkMag_x	JPDE x - DC 24/48 V magnitude	AnalogInput	REAL
** x = 1, 2			

18.2.8.13 JPDE Gnd Volts

Parameter	Description	Choices
Gnd_Mag_Trig_Volt	Ground magnitude fault trigger voltage	1 to 30

Variable**	Description	Direction	Type
DC_24VGnd_FdbkMag_x	JPDE x - ground feedback magnitude	AnalogInput	REAL
** x = 1, 2			

18.2.8.14 JPDE Fuse

Parameter	Description	Choices
FuseDiag	Enable/Disable fuse diagnostic alarm	Enable, Disable

Variable**	Description	Direction	Type
FU11_FU12_Stat_x	JPDE x - FU11/FU12 fuse status (connector JS1)	Input	BOOL
FU21_FU22_Stat_x	JPDE x - FU21/FU22 fuse status (connector JS2)	Input	BOOL
FU31_FU32_Stat_x	JPDE x - FU31/FU32 fuse status (connector JS3)	Input	BOOL
FUA1_FUA2_Stat_x	JPDE x - FUA1/FUA2 fuse status (connector JFA)	Input	BOOL
FUB1_FUB2_Stat_x	JPDE x - FUB1/FUB2 fuse status (connector JFB)	Input	BOOL
FUC1_FUC2_Stat_x	JPDE x - FUC1/FUC2 fuse status (connector JFC)	Input	BOOL
Dry_Cnt_JPS1_Stat_x	JPDE x - Dry Cnt 1 status (connector JPS1)	Input	BOOL
Dry_Cnt_JPS2_Stat_x	JPDE x - Dry Cnt 2 status (connector JPS2)	Input	BOOL
** x = 1, 2			

18.2.8.15 JPDB Inputs

Parameter	Description	Choices
InputDiagEnab	Input diagnostic enable	Enable, Disable
ACFdbkInVoltage	AC feedback input voltage	100 to 250
ACFdbkInTol	Percentage variation tolerance on AC input	0pct, 5pct, 10pct, 20pct
ACDiffVoltOff	AC difference voltage offset; Adjust AC voltage reading in signal space based on AC voltage reading at screws.	Any value

Variable**	Description	Direction	Type
AC_Fdbk1_Volt_x	JPDB x - AC 100 to 250 V feedback input 1 voltage	AnalogInput	REAL
AC_Fdbk2_Volt_x	JPDB x - AC 100 to 250 V feedback input 2 voltage	AnalogInput	REAL
** x = 1, 2			

18.2.8.16 JPDB Fuse

Parameter	Description	Choices
FuseDiag	Enable/Disable fuse diagnostic alarm; Fuse diagnostics are also suppressed if source on which they exist are unhealthy due to failure of low limit threshold on them. Applicable only to FU1 to FU6	Enable, Disable

Variable**	Description	Direction	Type
FU1_Stat_x	JPDB x - FU1 fuse Status (connector JAC1)	Input	BOOL
FU2_Stat_x	JPDB x - FU2 fuse Status (connector JAC2)	Input	BOOL
FU3_Stat_x	JPDB x - FU3 fuse Status (connector JAC3)	Input	BOOL
FU4_Stat_x	JPDB x - FU4 fuse Status (connector JAC4)	Input	BOOL
FU5_Stat_x	JPDB x - FU5 fuse Status (connector JAC5)	Input	BOOL
FU6_Stat_x	JPDB x - FU6 fuse Status (connector JAC6)	Input	BOOL
FU7_Stat_x	JPDB x - FU7 fuse Status (connector JA1)	Input	BOOL
FU8_Stat_x	JPDB x - FU8 fuse Status (connector JA2)	Input	BOOL
** x = 1, 2			

18.3 PPDA Specific Alarms

The following alarms are specific to the PPDA I/O pack.

32, 35

Description JPDS-[ ] P28v-R volt fdbk (JR/PR connector) out of range

Possible Cause

- The 28 V Power supply input is out of range. It is expected to be within ±5% of 28 V.
- The 28 V R power supply has not been connected.
- There could be a power supply problem.

Solution

- The input is not used. Set *PS28vEnable* to *Disable*.
- Verify the power supply connections (JR/PR) to the terminal board.
- Verify that the power supply feedback on the **JPDS/M Inputs** tab in the ToolboxST application is within the expected tolerance (±5%).

33, 36

Description JPDS-[ ] P28v-S volt fdbk (JS/PS connector) out of range

Possible Cause

- The 28 V Power supply input is out of range. It is expected to be within ±5% of 28 V.
- The 28 V S power supply has not been connected.
- There could be a power supply problem.

Solution

- The input is not used. Set *PS28vEnable* to **Disable**.
- Verify the power supply connections (JS/PS) to the terminal board.
- Verify that the power supply feedback on the **JPDS/M Inputs** tab in ToolboxST is within the expected tolerance (±5%).

34, 37

Description JPDS-[ ] P28v-T volt fdbk (JT/PT connector) out of range

Possible Cause

- The 28 V Power supply input is out of range. It is expected to be within ±5% of 28 V.
- The 28 V T power supply has not been connected.
- There could be a power supply problem.

Solution

- The input is not used. Set *PS28vEnable* to *Disable*.
- Verify the power supply connections (JT/PT) to the terminal board.
- Verify that the power supply feedback on the **JPDS/M Inputs** tab in the ToolboxST application is within the expected tolerance (±5%).

38, 41

Description JPDS-[ ] P28v-R contact input (JR connector) indicates PS problem

Possible Cause

- The power supply contact is open. The power supply is not operating normally.
- The power supply contact feedback is not connected to the terminal board JR connector.
- The power supply contact is not used.

Solution

- Verify the status of the power supply contact and that the power supply is operating correctly.
- Verify the connections between the power supply and the JR connector on the terminal board.
- The JR Input is not used. Set *PS28vEnable* to *Disable*.
- The power supply is used, but the JR contact feedback is not connected. Set *PS28vEnable* to *NoDryCnt* to disable this alarm, but continue to monitor the 28 V power supply input.

39, 42

Description JPDS-[ ] P28v-S contact input (JS connector) indicates PS problem

Possible Cause

- The power supply contact is open. The power supply is not operating normally.
- The power supply contact feedback is not connected to the terminal board JS connector.
- The power supply contact is not used.

Solution

- Verify the status of the power supply contact and that the power supply is operating correctly.
- Verify the connections between the power supply and the JS connector on the terminal board.
- The JS Input is not used. Set *PS28vEnable* to *Disable*.
- The power supply is used, but the JS contact feedback is not connected. Set *PS28vEnable* to *NoDryCnt* to disable this alarm, but continue to monitor the 28 V power supply input.

40, 43

Description JPDS-[ ] P28v-T contact input (JT connector) indicates PS problem

Possible Cause

- The power supply contact is open. The power supply is not operating normally.
- The power supply contact feedback is not connected to the terminal board JT connector.
- The power supply contact is not used.

Solution

- Verify the status of the power supply contact and that the power supply is operating correctly.
- Verify the connections between the power supply and the JT connector on the terminal board.
- The JT Input is not used. Set *PS28vEnable* to *Disable*.
- The power supply is used, but the JT contact feedback is not connected. Set *PS28vEnable* to *NoDryCnt* to disable this alarm, but continue to monitor the 28 V power supply input.

44, 47

Description JPDS-[ ] P28v-R aux output fuse (JAR connector) not OK

Possible Cause

- The auxiliary output JAR fuse has exceeded its current rating (1.6 A at 20°C) and disabled the auxiliary output.

Solution

- Disconnect the auxiliary output connections and troubleshoot the loading of the auxiliary output beyond 1.6 A.
- The fuse is self-resetting. Refer to help documentation.

45, 48

Description JPDS-[ ] P28v-S aux output fuse (JAS connector) not OK

Possible Cause

- The auxiliary output JAS fuse has exceeded its current rating (1.6 A at 20°C) and disabled the auxiliary output.

Solution

- Disconnect the auxiliary output connections and troubleshoot the loading of the auxiliary output beyond 1.6 A.
- The fuse is self-resetting. Refer to help documentation.

46, 49

Description JPDS-[ ] P28v-T aux output fuse (JAT connector) not OK

Possible Cause

- The auxiliary output JAT fuse has exceeded its current rating (1.6 A at 20°C) and disabled the auxiliary output.

Solution

- Disconnect the auxiliary output connections and troubleshoot the loading of the auxiliary output beyond 1.6 A.
- Fuse is self resetting. Refer to help documentation.

50, 53

Description JPDM-[ ] P28v-R volt fdbk (JR/PR connector) out of range

Possible Cause

- The 28 V power supply input is out of range. It is expected to be within ±5% of 28 V.
- The 28 V R power supply has not been connected.
- There could be a power supply problem.

Solution

- The input is not used. Set *PS28vEnable* to *Disable*.
- Verify the power supply connections (JR/PR) to the terminal board.
- Verify that the power supply feedback on the **JPDS/M Inputs** tab in the ToolboxST application is within the expected tolerance (±5%).

51, 54

Description JPDM-[ ] P28v-S volt fdbk (JS/PS connector) out of range

Possible Cause

- The 28 V power supply input is out of range. It is expected to be within ±5% of 28 V.
- The 28 V S power supply has not been connected.
- There could be a power supply problem.

Solution

- The input is not used. Set *PS28vEnable* to *Disable*.
- Verify the power supply connections (JS/PS) to the terminal board.
- Verify that the power supply feedback on the **JPDS/M Inputs** tab in the ToolboxST application is within the expected tolerance (±5%).

52, 55

Description JPDM-[ ] P28v-T volt fdbk (JT/PT connector) out of range

Possible Cause

- The 28 V power supply input is out of range. It is expected to be within ±5% of 28 V.
- The 28 V T power supply has not been connected.
- There could be a power supply problem.

Solution

- The input is not used. Set *PS28vEnable* to *Disable*.
- Verify the power supply connections (JT/PT) to the terminal board.
- Verify that the power supply feedback on the **JPDS/M Inputs** tab in the ToolboxST application is within the expected tolerance (±5%).

56, 59

Description JPDM-[ ] P28v-R contact input (JR connector) indicates PS problem

Possible Cause

- The power supply contact is open. The power supply is not operating normally.
- The power supply contact feedback is not connected to the terminal board JR connector.
- The power supply contact is not used.

Solution

- Verify the status of the power supply contact, and that the power supply is operating correctly.
- Verify the connections between the power supply and the JR connector on the terminal board.
- The JR input is not used. Set *PS28vEnable* to *Disable*.
- The power supply is used, but the JR contact feedback is not connected. Set *PS28vEnable* to *NoDryCnt* to disable this alarm, but continue to monitor the 28 V power supply input.

57, 60

Description JPDM-[ ] P28v-S contact input (JS connector) indicates PS problem

Possible Cause

- The power supply contact is open. The power supply is not operating normally.
- The power supply contact feedback is not connected to the terminal board JS connector.
- The power supply contact is not used.

Solution

- Verify the status of the power supply contact and that the power supply is operating correctly.
- Verify the connections between the power supply and the JS connector on the terminal board.
- The JS input is not used. Set *PS28vEnable* to *Disable*.
- The power supply is used, but the JS contact feedback is not connected. Set *PS28vEnable* to *NoDryCnt* to disable this alarm, but continue to monitor the 28 V power supply input.

58, 61

Description JPDM-[ ] P28v-T contact input (JT connector) indicates PS problem

Possible Cause

- The power supply contact is open. The power supply is not operating normally.
- The power supply contact feedback is not connected to the terminal board JT connector.
- The power supply contact is not used.

Solution

- Verify the status of the power supply contact, and that the power supply is operating correctly.
- Verify the connections between the power supply and the JT connector on the terminal board.
- The JT input is not used. Set *PS28vEnable* to *Disable*.
- The power supply is used, but the JT contact feedback is not connected. Set *PS28vEnable* to *NoDryCnt* to disable this alarm, but continue to monitor the 28 V power supply input.

62, 65

Description JPDM-[ ] P28v-R aux output fuse (JAR connector) not OK

Possible Cause

- The auxiliary output JAR fuse has exceeded its current rating (3.75 A at 20°C, 83 °F) and disabled the auxiliary output.

Solution

- Disconnect the auxiliary output connections and troubleshoot the loading of the auxiliary output beyond 3.75 A.
- The fuse is self-resetting. Refer to the help documentation.

63, 66

Description JPDM-[ ] P28v-S aux output fuse (JAS connector) not OK

Possible Cause

- The auxiliary output JAS fuse has exceeded its current rating (3.75 A at 20°C, 83 °F) and disabled the auxiliary output.

Solution

- Disconnect the auxiliary output connections and troubleshoot the loading of the auxiliary output beyond 3.75 A.
- The fuse is self-resetting. Refer to the help documentation.

64, 67

Description JPDM-[ ] P28v-T aux output fuse (JAT connector) not OK

Possible Cause

- The auxiliary output JAT fuse has exceeded its current rating (3.75 A at 20°C, 83 °F) and disabled the auxiliary output.

Solution

- Disconnect the auxiliary output connections and troubleshoot the loading of the auxiliary output beyond 3.75 A.
- The fuse is self-resetting. Refer to the help documentation.

68, 71

Description JPDM-[ ] fuse FU4 (J1 connector) is blown

Possible Cause

- The specified fuse is blown.
- The 28 V R power supply input is not connected.

Solution

- Replace the fuse.
- Verify the power supply connections to the terminal board.

69, 72

Description JPDM-[ ] fuse FU5 (J1 connector) is blown

Possible Cause

- The specified fuse is blown.
- The 28 V R power supply input is not connected.

Solution

- Replace the fuse.
- Verify the power supply connections to the terminal board.

70, 73

Description JPDM-[ ] fuse FU6 (J1 connector) is blown

Possible Cause

- The specified fuse is blown.
- The 28 V R power supply input is not connected.

Solution

- Replace the fuse.
- Verify the power supply connections to the terminal board.

74, 77

Description JPDM-[ ] fuse FU7 (J2 connector) is blown

Possible Cause

- The specified fuse is blown.
- The 28 V S power supply input is not connected.

Solution

- Replace the fuse.
- Verify the power supply connections to the terminal board.

75, 78

Description JPDM-[ ] fuse FU8 (J2 connector) is blown

Possible Cause

- The specified fuse is blown.
- The 28 V S power supply input is not connected.

Solution

- Replace the fuse.
- Verify the power supply connections to the terminal board.

76,79

Description JPDM-[ ] fuse FU9 (J2 connector) is blown

Possible Cause

- The specified fuse is blown.
- The 28 V S power supply input is not connected.

Solution

- Replace the fuse.
- Verify the power supply connections to the terminal board.

80,83

Description JPDM-[ ] fuse FU10 (J3 connector) is blown

Possible Cause

- The specified fuse is blown.
- The 28 V T power supply input is not connected.

Solution

- Replace the fuse.
- Verify the power supply connections to the terminal board.

81,84

Description JPDM-[ ] fuse FU11 (J3 connector) is blown

Possible Cause

- The specified fuse is blown.
- The 28 V T power supply input is not connected.

Solution

- Replace the fuse.
- Verify the power supply connections to the terminal board.

82,85

Description JPDM-[ ] fuse FU12 (J3 connector) is blown

Possible Cause

- The specified fuse is blown.
- The 28 V T power supply input is not connected.

Solution

- Replace the fuse.
- Verify the power supply connections to the terminal board.

86,89

Description JPDM-[ ] fuse FU1 (JCR connector) is blown

Possible Cause

- The specified fuse is blown.
- The 28 V R power supply input is not connected.

Solution

- Replace the fuse.
- Verify the power supply connections to the terminal board.

87,90

Description JPDM-[ ] fuse FU2 (JCS connector) is blown

Possible Cause

- The specified fuse is blown.
- The 28 V S power supply input is not connected.

Solution

- Replace the fuse.
- Verify the power supply connections to the terminal board.

88,91

Description JPDM-[ ] fuse FU3 (JCT connector) is blown

Possible Cause

- The specified fuse is blown.
- The 28 V T power supply input is not connected.

Solution

- Replace the fuse.
- Verify the power supply connections to the terminal board.

92-95

Description JPDB-[ ] AC In-[ ] [ ]V fdbk (J1 connector) out of range

Possible Cause

- The specified ac input is configured to the wrong nominal voltage value.
- The ac input voltage is out of tolerance from the nominal voltage value.
- The ac source voltage is out of range.
- The ac input is not connected.

Solution

- Verify that the nominal ac input voltage matches the value configured in **ACFdbkInVoltage**.
- The ac tolerance is set too low. Check that **ACFdbkInTol** is set to the proper value.
- Verify that the ac supply is within the specified parameters (Refer to the JPDB help documentation.)
- If the ac input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**AC_Fdbk#_Volt**) to **Disabled**.

96-101, 104-109

Description JPDB-[ ] fuse FU[ ] is blown or SW[ ] switched OFF

Possible Cause

- The specified switch is turned off and **FuseDiag** is enabled.
- The specified fuse is blown.
- The ac input is not connected.

Solution

- If the switch is turned off (the output is not used), disable the diagnostic by setting **FuseDiag** to **Disable.**
- If the output is used, verify that the switch is turned on.
- Replace the fuse.
- Verify the ac input connections to the terminal board.
- If the ac input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**AC_Fdbk#_Volt**) to **Disabled**.

102-103,
110-111

Description JPDB-[ ] fuse FU[ ] is blown

Possible Cause

- The specified fuse is blown.
- The ac input is not connected.

Solution

- Replace the fuse.
- Verify the ac input connections to the terminal board.
- If the ac input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**AC_Fdbk#_Volt**) to **Disabled**.

112,114

Description JPDF-[ ] DC 125V magnitude (JD1/JZ2/JZ3 connector) out of range

Possible Cause

- The 125 V dc input is less than **DC_125v_Trig_Volt**.
- **DC_125v_Trig_Volt** is set too high.
- The 125 V dc source voltage is out of range.
- The 125 V dc input is not connected.

Solution

- Verify that **DC_125v_Trig_Volt** is set correctly.
- If fed from the dc battery Input, check the connections to JD1 and TB1.
- If fed from DACA, check the connections to JZ2 and/or JZ3.
- Verify the grounding of the dc input signals. Refer to the JPDF help for more info.
- If the 125 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_125VFdbkMag**) to **Disabled**.

113, 115

Description JPDF-[ ] DC 125V Ground magnitude (JD1/JZ2/JZ3 connector) out of range

Possible Cause

- The 125 V ground feedback magnitude is greater than **Gnd_Mag_Trig_Volt**.
- **Gnd_Mag_Trig_Volt** is set too low.
- One side of the dc 125 V source voltage is grounded.

Solution

- Verify that **Gnd_Mag_Trig_Volt** is set correctly.
- Check the connections to the specified connector.
- Verify the grounding of the dc input signals. Refer to the JPDF help documentation.
- If DC 125V input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_125VFdbkMag**) to **Disabled**.

116, 125

Description JPDF-[ ] fuse FU1R or FU2R (J1R connector) is blown or SW1R switched OFF

Possible Cause

- The SW1R is turned off and **FuseDiag** is enabled.
- The FU1R or FU2R fuse is blown.
- The 125V dc input is not connected.

Solution

- If the switch is turned off (output is not used), disable the diagnostic by setting **FuseDiag** to **Disable**.
- If the output is used, verify that the switch is turned on.
- Replace the fuse.
- Verify the 125 V dc input connections to the terminal board.
- If the 125 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_125VFdbkMag**) to **Disabled**.

117, 126

Description JPDF-[ ] fuse FU1S or FU2S (J1S connector) is blown or SW1S switched OFF

Possible Cause

- The SW1R is turned off and **FuseDiag** is enabled.
- The FU1S or FU2S fuse is blown.
- The 125 V dc input is not connected.

Solution

- If the switch is turned off (output is not used), disable the diagnostic by setting **FuseDiag** to **Disable**.
- If the output is used, verify that the switch is turned on.
- Replace the fuse.
- Verify the 125 V dc input connections to the terminal board.

118, 127

Description JPDF-[ ] fuse FU1T or FU2T (J1T connector) is blown or SW1T switched OFF

Possible Cause

- The SW1R is turned off and **FuseDiag** is enabled.
- The FU1T or FU2T fuse is blown.
- The 125 V dc input is not connected.

Solution

- If the switch is turned off (output is not used), disable the diagnostic by setting **FuseDiag** to **Disable**.
- If the output is used, verify that the switch is turned on.
- Replace the fuse.
- Verify the 125 V dc input connections to the terminal board.
- If the 125 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_125VFdbkMag**) to **Disabled**.

119, 128

Description JPDF-[ ] fuse FU71 or FU72 (J7X connector) is blown or SW7X switched OFF

Possible Cause

- The SW7X is turned off and **FuseDiag** is enabled.
- The FU71 or FU72 fuse is blown.
- The 125 V dc input is not connected.

Solution

- If the switch is turned off (output is not used), disable the diagnostic by setting **FuseDiag** to **Disable.**
- If the output is used, verify that the switch is turned on.
- Replace the fuse.
- Verify the 125 V dc input connections to the terminal board.
- If the 125 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_125VFdbkMag**) to **Disabled**.

120, 129

Description JPDF-[ ] fuse FU73 or FU74 (J7Y connector) is blown or SW7Y switched OFF

Possible Cause

- The SW7Y is turned off and **FuseDiag** is enabled.
- The FU73 or FU74 fuse is blown.
- The 125 V dc input is not connected.

Solution

- If the switch is turned off (output is not used), disable the diagnostic by setting **FuseDiag** to **Disable**.
- If the output is used, verify that the switch is turned on.
- Replace the fuse.
- Verify the 125 V dc input connections to the terminal board.
- If the 125 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_125VFdbkMag**) to **Disabled**.

121, 130

Description JPDF-[ ] fuse FU75 or FU76 (J7Z connector) is blown or SW7Z switched OFF.

Possible Cause

- The SW7Z is turned off and **FuseDiag** is enabled.
- The FU75 or FU76 fuse is blown.
- The 125 V dc input is not connected.

Solution

- If the switch is turned off (output is not used), disable the diagnostic by setting **FuseDiag** to **Disable**.
- If the output is used, verify that the switch is turned on.
- Replace the fuse.
- Verify the 125 V dc input connections to the terminal board.
- If the 125 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_125VFdbkMag**) to **Disabled**.

122, 131

Description JPDF-[ ] fuse FU81 or FU82 (J8A connector) is blown.

Possible Cause

- The FU81 or FU82 fuse is blown.
- The 125 V dc input is not connected.

Solution

- Replace the fuse.
- Verify the 125 V dc input connections to the terminal board.
- If the 125 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_125VFdbkMag**) to **Disabled**.

123, 132

Description JPDF-[ ] fuse FU83 or FU84 (J8B connector) is blown.

Possible Cause

- The FU83 or FU84 fuse is blown.
- The 125 V dc input is not connected.

Solution

- Replace the fuse.
- Verify the 125 V dc input connections to the terminal board.
- If the 125 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_125VFdbkMag**) to **Disabled**.

124, 133

Description JPDF-[ ] fuse FU12 or FU13 (J12 connector) is blown.

Possible Cause

- The FU12 or FU13 fuse is blown.
- The 125 V dc input is not connected.

Solution

- Replace the fuse.
- Verify the 125 V dc input connections to the terminal board.
- If the 125 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_125VFdbkMag**) to **Disabled**.

135

Description PPDA Invalid Combination: More than 2 JPDS boards present

Possible Cause PPDA allows up to two JPDS boards to be connected as part of the Power Distribution module. The PPDA has detected more than two JPDS boards connected through ribbon cables to the PDM.

Solution

- Verify that only one or two JPDS terminal boards are connected to the PDM through ribbon cables.
- Reboot the PPDA after the hardware connections are corrected.

136

Description PPDA Invalid Combination: More than 2 JPDE boards present

Possible Cause PPDA allows up to two JPDE boards to be connected as part of the Power Distribution module. The PPDA has detected more than two JPDE boards connected through ribbon cables to the PDM.

Solution

- Verify that only one or two JPDE terminal boards are connected to the PDM through ribbon cables.
- Reboot the PPDA after the hardware connections are corrected.

137

Description PPDA Invalid Combination: More than 2 JPDF boards present

Possible Cause PPDA allows up to two JPDF boards to be connected as part of the Power Distribution module. The PPDA has detected more than two JPDF boards connected through ribbon cables to the PDM.

Solution

- Verify that only one or two JPDF terminal boards are connected to the PDM through ribbon cables.
- Reboot the PPDA after the hardware connections are corrected.

138

Description PPDA Invalid Combination: More than 2 JPDB boards present

Possible Cause PPDA allows up to two JPDB boards to be connected as part of the Power Distribution module. The PPDA has detected more than two JPDB boards connected through ribbon cables to the PDM.

Solution

- Verify that only one or two JPDB terminal boards are connected to the PDM through ribbon cables.
- Reboot the PPDA after the hardware connections are corrected.

139

Note This alarm is obsolete.

Description PPDA Invalid Combination: More than 2 JPDR boards present.

Possible Cause PPDA allows up to two JPDR boards to be connected as part of the Power Distribution module. The PPDA has detected more than two JPDR boards connected through ribbon cables to the PDM.

Solution

- Verify that only one or two JPDR terminal boards are connected to the PDM through ribbon cables.
- Reboot the PPDA after the hardware connections are corrected.

140

Note This alarm is obsolete.

Description PPDA Invalid Combination: Terminal board JPDR-[ ] present without JPDB.

Possible Cause PPDA requires that a JPDB board be connected to the PDM for each JPDR connected.

- A JPDR board is connected without a JPDB present.
- Two JPDR boards are connected with only one JPDB present.

Solution

- Verify that for each JPDR connected through ribbon cable, there is one JPDB present.
- Verify that the ToolboxST configuration matches the hardware configuration.
- Reboot the PPDA after the hardware connections are corrected.

141-145

Description Configured TB at Phy Position-[ ] doesn't match actual H/W.

Possible Cause

- The auxiliary terminal board at the specified physical position does not match the ToolboxST configuration.
- The auxiliary terminal boards have been added in the wrong order.

Solution

- Verify that the actual hardware matches the auxiliary terminal board configuration in the ToolboxST configuration.
- Verify that the auxiliary board *physical position* matches the **Phy Pos** value in the ToolboxST configuration. (Right-click the PPDA and click **Modify...**.)
- **NOTE:** JPDM and JPDC boards assume two feedback channels, so the first connected auxiliary terminal board is in **Phy Pos 2** rather than **Phy Pos 1**.

146

Description PPDA Invalid Combination: More than 2 JPDM boards present.

Possible Cause PPDA allows up to two JPDM boards to be connected as part of the Power Distribution module. The PPDA has detected more than two JPDM boards connected through ribbon cables to the PDM.

Solution

- Verify that only one or two JPDM terminal boards are connected to the PDM through ribbon cables.
- Reboot the PPDA after the hardware connections are corrected.

147

Description PPDA Invalid Combination: Both JPDS and JPDM Terminal boards present.

Possible Cause PPDA does not allow JPDS and JPDM terminal boards to be mixed. The PPDA has detected both JPDS and JPDM terminal boards connected through ribbon cables to the PDM.

Solution

- Verify that there are only JPDS or JPDM boards present, but not both.
- Verify that the ToolboxST configuration matches the hardware configuration.
- Reboot the PPDA after the hardware connections are corrected.

148, 150

Description JPDE-[ ] 24/48 VDC magnitude (JD1/JPS1/JPS2 connector) out of range.

Possible Cause

- The 24/48 V dc input is less than **DC_24v_Trig_Volt**.
- **DC_24v_Trig_Volt** is set too high.
- The 24/48 V dc source voltage is out of range.
- The 24/48 V dc input is not connected.

Solution

- Verify that **DC_24v_Trig_Volt** is set correctly.
- Check the connections to the specified connector.
- Verify the grounding of the dc input signals. Refer to the JPDE help documentation.
- If 24/48 VDC input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_24VFdbkMag**) to **Disabled**.

149, 151

Description JPDE-[ ] DC Voltage Gnd fdbk mag (JD1/JPS1/JPS2 connector) out of range.

Possible Cause

- The 24/48 V dc ground feedback magnitude is greater than **Gnd_Mag_Trig_Volt**.
- **Gnd_Mag_Trig_Volt** is set too low.
- One side of the 24/48 V dc source voltage is grounded.

Solution

- Verify that **Gnd_Mag_Trig_Volt** is set correctly.
- Check the connections to the specified connector.
- Verify the grounding of the dc input signals. Refer to the JPDE help documentation.
- If 24/48 VDC input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_24VFdbkMag**) to **Disabled**.

152, 160

Description JPDE-[ ] fuse FU11/FU12 (JS1 connector) is blown or SWS1 switched OFF.

Possible Cause

- The SWS1 is turned off and **FuseDiag** is enabled.
- The FU11 or FU12 fuse is blown.
- The 24/48 V dc input is not connected.

Solution

- If the switch is turned off (output is not used), disable the diagnostic by setting **FuseDiag** to **Disable**.
- If the output is used, verify that the switch is turned on.
- Replace the fuse.
- Verify the 24/48 V dc input connections to the terminal board.
- If the 24/48 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_24VFdbkMag**) to **Disabled**.

153, 161

Description JPDE-[ ] fuse FU21/FU22 (JS2 connector) is blown or SWS2 switched OFF.

Possible Cause

- The SWS2 is turned off and **FuseDiag** is enabled.
- The FU21 or FU22 fuse is blown.
- The 24/48 V dc input is not connected.

Solution

- If the switch is turned off (output is not used), disable the diagnostic by setting **FuseDiag** to **Disable.**
- If the output is used, verify that the switch is turned on.
- Replace the fuse.
- Verify the 24/48 V dc input connections to the terminal board.
- If the 24/48 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_24VFdbkMag**) to **Disabled**.

154, 162

Description JPDE-[ ] fuse FU31/FU32 (JS3 connector) is blown or SWS3 switched OFF.

Possible Cause

- The SWS3 is turned off and **FuseDiag** is enabled.
- The FU31 or FU32 fuse is blown.
- The 24/48 V dc input is not connected.

Solution

- If the switch is turned off (output is not used), disable the diagnostic by setting **FuseDiag** to **Disable.**
- If the output is used, verify that the switch is turned on.
- Replace the fuse.
- Verify the 24/48 V dc input connections to the terminal board.
- If the 24/48 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_24VFdbkMag**) to **Disabled**.

155, 163

Description JPDE-[ ] fuse FUA1/FUA2 (JFA connector) is blown.

Possible Cause

- The FUA1 or FUA2 fuse is blown.
- The 24/48 V dc input is not connected.

Solution

- Replace the fuse.
- Verify the 24/48 V dc input connections to the terminal board.
- If the 24/48 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_24VFdbkMag**) to **Disabled**.

156, 164

Description JPDE-[ ] fuse FUB1/FUB2 (JFB connector) is blown.

Possible Cause

- The FUB1 or FUB2 fuse is blown.
- The 24/48 V dc input is not connected.

Solution

- Replace the fuse.
- Verify 24/48 V dc input connections to the terminal board.
- If the 24/48 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_24VFdbkMag**) to **Disabled**.

157, 165

Description JPDE-[ ] fuse FUC1/FUC2 (JFC connector) is blown.

Possible Cause

- The FUC1 or FUC2 fuse is blown.
- The 24/48 V dc input is not connected.

Solution

- Replace the fuse.
- Verify the 24/48 V dc input connections to the terminal board.
- If the 24/48 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_24VFdbkMag**) to **Disabled**.

158, 166

Description JPDE-[ ] DC Voltage contact input 1 (JPS1 connector) indicates PS problem.

Possible Cause

- The power supply contact is open. The power supply is not operating normally.
- The power supply dry contact feedback is not connected to the terminal board JPS1 connector.

Solution

- Verify the status of the power supply contact, and that the power supply is operating correctly.
- Verify the connections between the power supply and the JR connector on the JPDE.
- If the 24/48 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_24VFdbkMag**) to **Disabled**.

159, 167

Description JPDE-[ ] DC Voltage contact input 2 (JPS2 connector) indicates PS problem.

Possible Cause

- The power supply contact is open. The power supply is not operating normally.
- The power supply dry contact feedback is not connected to the terminal board JPS2 connector.

Solution

- Verify the status of the power supply contact, and that the power supply is operating correctly.
- Verify the connections between the power supply and the JR connector on the JPDE.
- If the 24/48 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_24VFdbkMag**) to **Disabled**.

169

Description Invalid Terminal board ID at Physical Position [ ].

Possible Cause

- The terminal board ID is not recognized or supported by the current firmware version.
- The electronic terminal board ID is not programmed, or is programmed incorrectly.

Solution

- Upgrade the PPDA firmware to a version that supports the terminal board at the specified physical position. Refer to the help documentation for a list of supported terminal boards.
- Replace the terminal board hardware.

170-171

Description Input Src Mismatch on JPDF-[ ]: AC src detected at input instead DC.

Possible Cause

- The ac voltage has been detected at the 125 V dc input.

Solution

- Verify the 125 V dc input connections. Use a DVM to verify dc voltage on the input connections.
- Verify that the positive and negative inputs to the 125 V dc bus are connected to the proper terminals. Refer to the JPDF help documentation.

172

Description JPDC-DC 125V fdbk mag (JD1/JZ2 connector) out of range.

Possible Cause

- The 125 V dc input is less than **DC_125v_Trig_Volt**.
- **DC_125v_Trig_Volt** is set too high.
- The 125 V dc source voltage is out of range.
- The 125 V dc input is not connected.

Solution

- Verify that **DC_125v_Trig_Volt** is set correctly.
- If fed from the dc battery input, check the connections to JD1 and TB1.
- If fed from DACA, check the connections to JZ2.
- Verify the grounding of dc input signals. Refer to the JPDC help documentation.
- If the 125 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_125VFdbkMag**) to **Disabled**.

173

Description JPDC-DC 125V Gnd fdbk mag (JD1/JZ2 connector) out of range.

Possible Cause

- The dc 125 ground feedback magnitude is greater than **Gnd_Mag_Trig_Volt**.
- **Gnd_Mag_Trig_Volt** is set too low.
- One side of the DC 125 V source voltage is grounded.

Solution

- Verify that **Gnd_Mag_Trig_Volt** is set correctly.
- Check the connections to the specified connector.
- Verify the grounding of the dc input signals. Refer to the JPDC help documentation.
- If DC 125V input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_125VFdbkMag**) to **Disabled**.

174

Description JPDC-Fuse FU71 or FU72 (J7A connector) is blown or SW7A switched OFF.

Possible Cause

- The specified switch is turned off and **FuseDiag** is enabled.
- The specified fuse is blown.
- The 125 V dc input is not connected.

Solution

- If the switch is turned off (output is not used), disable the diagnostic by setting **FuseDiag** to **Disable.**
- If the output is used, verify that the switch is turned on.
- Replace the fuse.
- Verify the 125 V dc input connections to the terminal board.
- If the 125 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_125VFdbkMag**) to **Disabled**.

175

Description JPDC-Fuse FU73 or FU74 (J7B connector) is blown or SW7B switched OFF.

Possible Cause

- The specified switch is turned off and **FuseDiag** is enabled.
- The specified fuse is blown.
- The 125 V dc input is not connected.

Solution

- If the switch is turned off (output is not used), disable the diagnostic by setting **FuseDiag** to **Disable**.
- If the output is used, verify that the switch is turned on.
- Replace the fuse.
- Verify the 125 V dc input connections to the terminal board.
- If the 125 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_125VFdbkMag**) to **Disabled**.

176

Description JPDC-Fuse FU75 or FU76 (J7C connector) is blown or SW7C switched OFF.

Possible Cause

- The specified switch is turned off and **FuseDiag** is enabled.
- The specified fuse is blown.
- The 125 V dc input is not connected.

Solution

- If the switch is turned off (output is not used), disable the diagnostic by setting **FuseDiag** to **Disable.**
- If the output is used, verify that the switch is turned on.
- Replace the fuse.
- Verify the 125 V dc input connections to the terminal board.
- If the 125 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_125VFdbkMag**) to **Disabled**.

177

Description JPDC-Fuse FU1R or FU2R (J1R connector) is blown or SW1R switched OFF.

Possible Cause

- The specified switch is turned off and **FuseDiag** is enabled.
- The specified fuse is blown.
- The 125 V dc input is not connected.

Solution

- If the switch is turned off (output is not used), disable the diagnostic by setting **FuseDiag** to **Disable**.
- If the output is used, verify that the switch is turned on.
- Replace the fuse.
- Verify the 125 V dc input connections to the terminal board.
- If the 125 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_125VFdbkMag**) to **Disabled**.

178

Description JPDC-Fuse FU1S or FU2S (J1S connector) is blown or SW1S switched OFF.

Possible Cause

- The specified switch is turned off and **FuseDiag** is enabled.
- The specified fuse is blown.
- The 125 V dc input is not connected.

Solution

- If the switch is turned off (output is not used), disable the diagnostic by setting **FuseDiag** to **Disable**.
- If the output is used, verify that the switch is turned on.
- Replace the fuse.
- Verify the 125 V dc input connections to the terminal board.
- If the 125 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_125VFdbkMag**) to **Disabled**.

179

Description JPDC-Fuse FU1T or FU2T (J1T connector) is blown or SW1T switched OFF.

Possible Cause

- The specified switch is turned off and **FuseDiag** is enabled.
- The specified fuse is blown.
- The 125 V dc input is not connected.

Solution

- If the switch is turned off (output is not used), disable the diagnostic by setting **FuseDiag** to **Disable**.
- If the output is used, verify that the switch is turned on.
- Replace the fuse.
- Verify the 125 V dc input connections to the terminal board.
- If the 125 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_125VFdbkMag**) to **Disabled**.

180

Description Input Src Mismatch on JPDC: AC src detected at input instead DC.

Possible Cause

- The ac voltage has been detected at the 125 V dc input.

Solution

- Verify the 125 V dc input connections. Use a DVM to verify the dc voltage on the input connections.
- Verify that the positive and negative inputs to the 125 V dc bus are connected to the proper terminals. Refer to the JPDC help documentation.
- If the 125 V dc input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**DC_125VFdbkMag**) to **Disabled**.

181

Description JPDC-AC [ ]V fdbk (JAC connector) out of range.

Possible Cause

- The specified ac input is configured to the wrong nominal voltage value.
- The ac input voltage is out of tolerance from the nominal voltage value.
- The ac source voltage is out of range.
- The ac input is not connected.

Solution

- Verify that the nominal ac input voltage matches the value configured in **ACFdbkInVoltage**.
- The ac tolerance is set too low. Verify that **ACFdbkInTol** is set to the proper value.
- Verify that the ac supply is within the specified parameters. Refer to the JPDC help documentation.
- If the ac input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**AC_VFdbk1_Volt**) to **Disabled**.

182

Description JPDC-Fuse FUAC1 (JAC1 connector) is blown or SWAC1 switched OFF.

Possible Cause

- The specified switch is turned off and **FuseDiag** is enabled.
- The specified fuse is blown.
- The ac input is not connected.

Solution

- If the switch is turned off (output is not used), disable the diagnostic by setting **FuseDiag** to **Disable**.
- If the output is used, verify that the switch is turned on.
- Replace the fuse.
- Verify the ac input connections to the terminal board.
- If the ac input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**AC_VFdbk1_Volt**) to **Disabled**.

183

Description JPDC-Fuse FUAC2 (JAC2 connector) is blown.

Possible Cause

- The specified fuse is blown.
- The ac input is not connected.

Solution

- Replace the fuse.
- Verify the ac input connections to the terminal board.
- If the ac input is not used, this diagnostic alarm can be disabled by setting the **InputDiagEnab** parameter on the associated input (**AC_VFdbk1_Volt**) to **Disabled**.

184

Description JPDC-P28v-R volt fdbk (JR/PR connector) out of range.

Possible Cause

- The 28 V power supply input is out of range. It should be within ±5% of 28 V.
- The 28 V power supply has not been connected.
- There may be a power supply problem.

Solution

- The input is not used. Set **PS28vEnable** to **Disable**.
- Verify the power supply connections (specified connector) to the terminal board.
- Verify that the power supply feedback on the **JPDC Inputs** tab in the ToolboxST configuration is within the expected tolerance (±5%).

185

Description JPDC-P28v-S volt fdbk (JS/PS connector) out of range.

Possible Cause

- The 28 V power supply input is out of range. It should be within ±5% of 28 V.
- The 28 V power supply has not been connected.
- There may be a power supply problem.

Solution

- The input is not used. Set **PS28vEnable** to **Disable**.
- Verify the power supply connections (specified connector) to the terminal board.
- Verify that the power supply feedback on the **JPDC Inputs** tab in the ToolboxST configuration is within the expected tolerance (±5%).

186

Description JPDC-P28v-T volt fdbk (JT/PT connector) out of range.

Possible Cause

- The 28 V power supply input is out of range. It should be within ±5% of 28 V.
- The 28 V power supply has not been connected.
- There may be a power supply problem.

Solution

- The input is not used. Set **PS28vEnable** to **Disable**.
- Verify the power supply connections (specified connector) to the terminal board.
- Verify that the power supply feedback on the **JPDC Inputs** tab in the ToolboxST configuration is within the expected tolerance (±5%).

187

Description JPDC-P28v-R contact input (JR connector) indicates PS problem.

Possible Cause

- The power supply contact is open. The power supply is not operating normally.
- The power supply contact feedback is not connected to the specified terminal board connector.
- The power supply dry contact is not used.

Solution

- Verify the status of the power supply contact, and that the power supply is operating correctly.
- Verify the connections between the power supply and the specified connector on the JPDC.
- The input is not used. Set **PS28vEnable** to **Disable**.
- The power supply is used, but the dry contact feedback is not connected. Set **PS28vEnable** to **NoDryCnt** to disable this alarm, but continue to monitor the 28 V power supply input.

188

Description JPDC-P28v-S contact input (JS connector) indicates PS problem.

Possible Cause

- The power supply contact is open. The power supply is not operating normally.
- The power supply contact feedback is not connected to the specified terminal board connector.
- The power supply dry contact is not used.

Solution

- Verify the status of the power supply contact, and that the power supply is operating correctly.
- Verify the connections between the power supply and the specified connector on the JPDC.
- The input is not used. Set **PS28vEnable** to **Disable**.
- The power supply is used, but the dry contact feedback is not connected. Set **PS28vEnable** to **NoDryCnt** to disable this alarm, but continue to monitor the 28 V power supply input.

189

Description JPDC-P28v-T contact input (JT connector) indicates PS problem.

Possible Cause

- The power supply contact is open. The power supply is not operating normally.
- The power supply contact feedback is not connected to the specified terminal board connector.
- The power supply dry contact is not used.

Solution

- Verify the status of the power supply contact, and that the power supply is operating correctly.
- Verify the connections between the power supply and the specified connector on the JPDC.
- The input is not used. Set **PS28vEnable** to **Disable**.
- The power supply is used, but the dry contact feedback is not connected. Set **PS28vEnable** to **NoDryCnt** to disable this alarm, but continue to monitor the 28 V power supply input.

190

Description PPDA Invalid Combination: More than 1 JPDC board present.

Possible Cause The PPDA allows only one JPDC board to be connected as part of the Power Distribution module. The PPDA has detected more than one JPDC boards connected through the ribbon cables to the PDM.

Solution

- Verify that only one JPDC terminal boards is connected to the PPDA. The PPDA should be plugged into the JPDC terminal board.
- Reboot the PPDA after the hardware connections are corrected.

191

Description PPDA Invalid Combination: JPDC and JPDS boards present Together.

Possible Cause The PPDA does not allow JPDC and JPDS terminal boards to be mixed. The PPDA has detected both JPDC and JPDS terminal boards connected through ribbon cables to the PDM.

Solution

- Verify that there are only JPDC or JPDS boards present, but not both.
- Verify that the ToolboxST configuration matches the hardware configuration.
- Reboot the PPDA after the hardware connections are corrected.

192

Description PPDA Invalid Combination: More than one JPDF Connected to JPDC board.

Possible Cause The PPDA allows only one JPDF board to be connected to a JPDC as part of the Power Distribution module. The PPDA has detected more than one JPDF boards connected through ribbon cables to the PDM.

Solution

- Verify that only one JPDF terminal board is connected to the PDM through ribbon cables.
- Reboot the PPDA after the hardware connections are corrected.

193

Description PPDA Invalid Combination: More than one JPDB Connected to JPDC board.

Possible Cause The PPDA allows only one JPDB board to be connected to a JPDC as part of the Power Distribution module. The PPDA has detected more than one JPDB boards connected through ribbon cables to the PDM.

Solution

- Verify that only one JPDB terminal board is connected to the PDM through ribbon cables.
- Reboot the PPDA after the hardware connections are corrected.

194

Description PPDA Invalid Combination: JPDC and JPDM boards present Together.

Possible Cause The PPDA does not allow JPDC and JPDM terminal boards to be mixed. The PPDA has detected both JPDC and JPDM terminal boards connected through ribbon cables to the PDM.

Solution

- Verify that there are only JPDC or JPDM boards present, but not both.
- Verify that the ToolboxST configuration matches the hardware configuration.
- Reboot the PPDA once the hardware connections have been corrected.

195

Description JPDG-P28v volt fdbk (JR/JS connector) out of range.

Possible Cause

- The 28 V power supply input is out of range. It should be within ± 5% of 28 V.
- The 28 V power supply has not been connected.
- There may be a power supply problem.

Solution

- The input is not used. Set the PS28v Enable to *Disable*.
- Check the power supply connections (specified connector) to the terminal board.
- From the ToolboxST application JPDG **Inputs** tab, verify that the power supply feedback configuration is within the expected tolerance (± 5%).

196 – 197

Description JPDG-P28v dry contact input [ ] (P3 connector) not OK

Possible Cause

- The power supply contact is open. The power supply is not operating normally.
- The power supply contact feedback is not connected to the specified terminal board connector.
- The power supply dry contact is not used.

Solution

- Verify the status of the power supply contact, and that the power supply is operating correctly.
- Check the connections between the power supply and the specified connector on the JPDG.
- If the input is not used, set the PS28v Enable to Disable.
- If the power supply is used but the dry contact feedback is not connected, set the PS28vEnable to NoDryCnt to disable this alarm. Continue to monitor the 28 V power supply input.

198

Description JPDG fuse FU1 (J1 connector) is blown

Possible Cause The specified fuse is blown.

Solution Replace the fuse.

199

Description JPDG fuse FU2 (J1 connector) is blown

Possible Cause The specified fuse is blown.

Solution Replace the fuse.

200

Description JPDG fuse FU3 (J2 connector) is blown

Possible Cause The specified fuse is blown.

Solution Replace the fuse.

201

Description JPDG fuse FU4 (J2 connector) is blown

Possible Cause The specified fuse is blown.

Solution Replace the fuse.

202

Description JPDG fuse FU5 (J3 connector) is blown

Possible Cause The specified fuse is blown.

Solution Replace the fuse.

203

Description JPDG fuse FU6 (J3 connector) is blown

Possible Cause The specified fuse is blown.

Solution Replace the fuse.

204

Description JPDG fuse FU7 (J4 connector) is blown

Possible Cause The specified fuse is blown.

Solution Replace the fuse.

205

Description JPDG fuse FU8 (J4 connector) is blown

Possible Cause The specified fuse is blown.

Solution Replace the fuse.

206 – 207

Description JPDG ACIn-[ ] [ ]V fdbk (JAC1 connector) out of range

Possible Cause

- The specified ac input is configured to the wrong nominal voltage value.
- The ac input voltage is out of tolerance from the nominal voltage value.
- The ac source voltage is out of range.
- The ac input is not connected.

Solution

- Verify that the nominal ac input voltage matches the value configured in the ACFdbkInVoltage.
- The ac tolerance is set too low. Check that the ACFdbkInTol is set to the proper value.
- Verify that the ac supply is within the specified parameters.
- If the ac input is not used, this diagnostic alarm can be disabled by setting the InputDiagEnab parameter on the associated input (AC_Fdbk#_Volt) to *Disabled*.

208

Description JPDG DC 24V Voltage fdbk mag (JPS1/JPS2 connector) out of range

Possible Cause

- The 24/48 V dc input is less than the DC_24v_Trig_Volt.
- The DC_24v_Trig_Volt is set too high.
- The 24/48 V dc source voltage is out of range.
- The 24/48 V dc input is not connected.

Solution

- Verify that the DC_24v_Trig_Volt is set correctly.
- Check the connections to the specified connector.
- Check the grounding of the dc input signals.
- If 24/48 V dc input is not used, this diagnostic alarm can be disabled by setting the InputDiagEnab parameter on the associated input (DC_24VFdbkMag) to *Disabled*.

209

Description JPDG DC 24V Voltage GND fdbk mag (JPS1/JPS2 connector) out of range

Possible Cause

- The 24/48 V dc ground feedback magnitude is greater than the Gnd_Mag_Trig_Volt.
- The Gnd_Mag_Trig_Volt is set too low.
- Only one side of the 24/48 V dc source voltage is grounded.

Solution

- Verify that the Gnd_Mag_Trig_Volt is set correctly.
- Check the connections to the specified connector.
- Check the grounding of the dc input signals.
- If 24/48 V dc input is not used, this diagnostic alarm can be disabled by setting the InputDiagEnab parameter on the associated input (DC_24VFdbkMag) to *Disabled*.

210 – 211

Description JPDG DC 24V Voltage dry contact input [ ] (P4 connector) not OK

Possible Cause

- The power supply contact is open. The power supply is not operating normally.
- The power supply dry contact feedback is not connected to the terminal board P4 connector.

Solution

- Verify the status of the power supply contact, and that the power supply is operating correctly.
- Check the connections between the power supply and the P4 connector on the JPDG.
- If the 24/48 V dc input is not used, this diagnostic alarm can be disabled by setting the InputDiagEnab parameter on the associated input (DC_24VFdbkMag) to *Disabled*.

212

Description JPDG fuse FU10/FU11 (JFA connector) is blown

Possible Cause The FU10 or FU11 fuse is blown.

Solution

- Replace the fuse.
- If the 24/48 V dc input is not used, this diagnostic alarm can be disabled by setting the InputDiagEnab parameter on the associated input (DC_24VFdbkMag) to *Disabled*.

213

Description JPDG fuse FU12/FU13 (JFB connector) is blown.

Possible Cause The FU12 or FU13 fuse is blown.

Solution

- Replace the fuse.
- If the 24/48 V dc input is not used, this diagnostic alarm can be disabled by setting the InputDiagEnab parameter on the associated input (DC_24VFdbkMag) to *Disabled*.

214

Description JPDG fuse FU14/FU15 (JFC connector) is blown.

Possible Cause The FU14 or FU15 fuse is blown.

Solution

- Replace the fuse.
- If the 24/48 V dc input is not used, this diagnostic alarm can be disabled by setting the InputDiagEnab parameter on the associated input (DC_24VFdbkMag) to *Disabled*.

215

Description JPDG fuse FU16/FU17 (JFD connector) is blown.

Possible Cause The FU16 or FU17 fuse is blown.

Solution

- Replace the fuse.
- If the 24/48 V dc input is not used, this diagnostic alarm can be disabled by setting the InputDiagEnab parameter on the associated input (DC_24VFdbkMag) to *Disabled*.

216

Description JPDG fuse FU18/FU19 (JFE connector) is blown.

Possible Cause The FU18 or FU19 fuse is blown.

Solution

- Replace the fuse.
- If the 24/48 V dc input is not used, this diagnostic alarm can be disabled by setting the InputDiagEnab parameter on the associated input (DC_24VFdbkMag) to *Disabled*.

217

Description JPDG fuse FU20/FU21 (JFF connector) is blown.

Possible Cause The FU20 or FU21 fuse is blown.

Solution

- Replace the fuse.
- If the 24/48 V dc input is not used, this diagnostic alarm can be disabled by setting the InputDiagEnab parameter on the associated input (DC_24VFdbkMag) to *Disabled*.

218

Description JPDG fuse FU22/FU23 (JFG connector) is blown.

Possible Cause The FU22 or FU23 fuse is blown.

Solution

- Replace the fuse.
- If the 24/48 V dc input is not used, this diagnostic alarm can be disabled by setting the InputDiagEnab parameter on the associated input (DC_24VFdbkMag) to *Disabled*.

219

Description Invalid Board Combination with the JPDG

Possible Cause The PPDA has detected invalid board combination connected through the ribbon cables to the JPDG board. The invalid board combination connected to JPDG may be one of the following:

- More than one JPDG board
- JPDS mixed with JPDG
- JPDM mixed with JPDG
- JPDC mixed with JPDG
- More than one JPDE board
- More than one JPDB board
- More than two JPDF boards

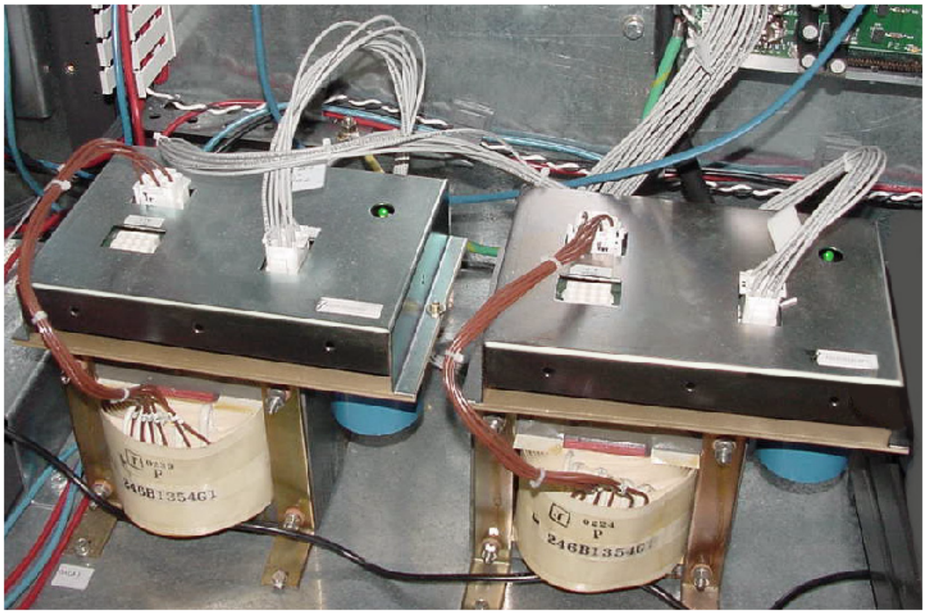
Solution When the PPDA I/O pack is hosted by the JPDG board, verify that the following valid board combination are connected to JPDG:

- Only one JPDE board.
- Only one JPDB board.
- Only two JPDF boards.
- Maximum three auxiliary boards can be connected at any given time.
- Reboot the PPDA after the hardware connections have been corrected.

18.4 DACA AC to DC Power Conversion

The DACA converts 115/230 V ac input power into 125 V dc output power, and the output power rating is approximately 1000 W. It is used when the primary power source for a control system is 125 V dc with or without a battery. In addition to power conversion, DACA provides additional local energy storage to extend the ride-through time whenever there is a complete loss of control power. The DS2020DACAG2 is a drop in replacement for the DS2020DACAG1. It is backward compatible in systems that used the previous version and it should be used as a replacement part for the previous model.

The DS2020DACAG2 model has a higher power rating than the previous module. Also, this new model can be paralleled for greater output current. Due to the higher power rating of the new module, DACAG1 and DACAG2 modules will not share the load equally and cannot be paralleled. When replacing a DACAG1 with a DACAG2 in applications with two DACA modules, both modules must be replaced with the DACAG2 version. The DS2020DACAG2 is recommended for all new panel designs.



DACA Power Conversion Modules

18.4.1 DACA Application Notes

The DACA module provides ac input to 125 V dc output power conversion. This module is typically used when a 125 V dc battery is used as a primary power source and it is desirable to back-up the battery with one or more ac power sources. In addition to power conversion, this module provides additional local energy storage to extend the ride-through time of the Mark VIe control when confronted with a complete loss of control power.

Note Since DACA has local energy storage capability, it takes time to discharge its output in case of loss of ac input if battery is not present in the system.

While using as simple a design as possible for reliability (full wave bridge rectifier plus output capacitance) DACA presents a fairly *dirty* load to the ac source. It should be applied with source filter circuits to prevent distortion of the supply. Appropriate filters are supplied as part of the JPDB ac power module and no additional filtering should be needed. If DACA is used with ac applied directly to the JPDF JAC1 connector then external filters will be required.

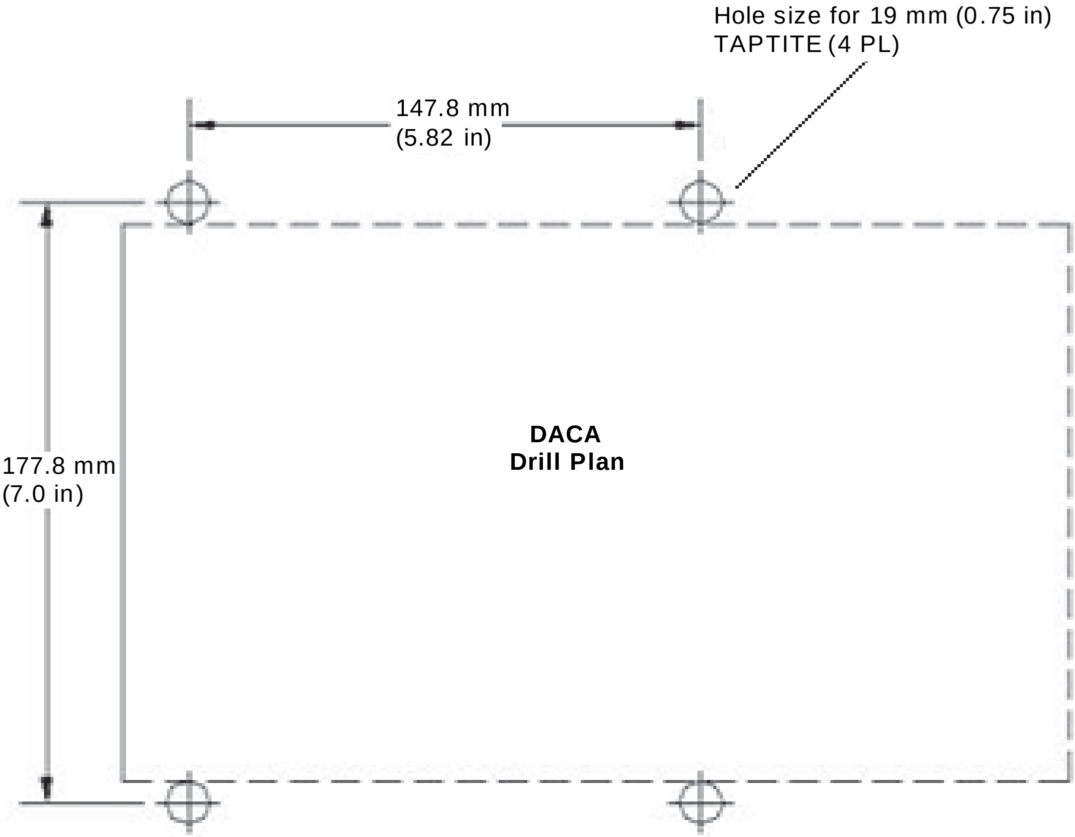
Input to DACA V ac RMS	Output volts no load	Output Voltage Full load	Output current	Input current	Ripple voltage	Output volt step response full load- no load
120 V	130 V	105.6 V	9.2 A	10.5 A	2.92 V P-P	106 V to 132 V dc
240 V	130.6 V	111.8 V	9.3 A	6 A	3.56 V P-P	111 V to 131 V dc

18.4.2 Installation

Caution

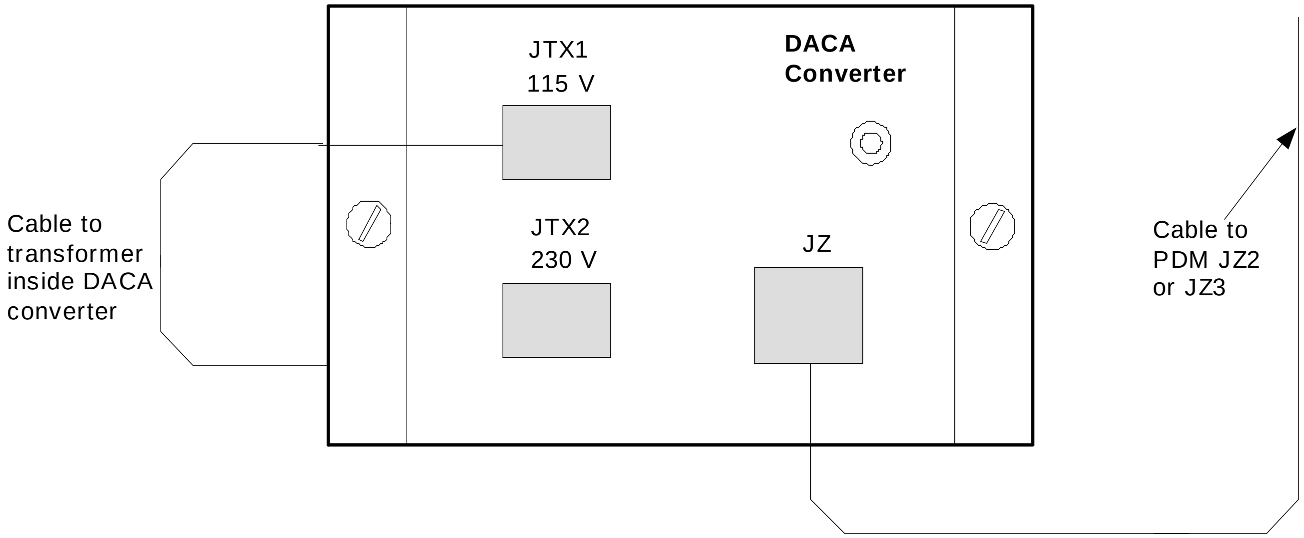
Ensure the proper voltage is selected before power is applied to the equipment.

The DACA module has four mounting holes in its base.



The keep out area is 219.7 mm (8.65 in) x 353.1 mm (13.9 in)

Ac power input and dc output is through a single 12-position connector JZ that is wired into connector JZ2 or JZ3 of the PDM. Selection of 115 V ac or 230 V ac input is made by plugging the DACA internal cable into connector JTX1 for 115 V or JTX2 for 230 V.



DACA Module Wiring

18.4.2.1 DACA Filter Capacitor Wear Out

The electrolytic capacitors in the DACA module wear out over time due to the ambient temperature of the environment where they are used. The following table displays the calculated service life expectancy and recommended replacement schedule for the DACA modules. Refer to the section, *Replacing a DACA*.

DACA Replacement Schedule

Calculated Life Expectancy of DACA Capacitor	**Recommended Replacement Schedule***
At 20°C (68 °F) ambient	100 years
At 45°C (113 °F) ambient	20 years
At 65°C (149 °F) ambient	5 years
At 70°C (158 °F) ambient	3.5 years
* Due to wear out of Electrolytic Capacitor	

18.4.3 Operation

DACA receives ac power through the cable harness that is plugged into connector JZ. DACA uses a full wave bridge rectifier and an output filter capacitor. If needed, the user must provide an input filter to attenuate harmonic currents injected into the incoming line.

Single DACA Module, Maximum Output Current is 9.5 A dc

Input to DACA V ac rms	**Input Current at Max Load**
115 V ac	11 A
230 V ac	6 A

Output Voltage Load = 1 A dc	**Output Voltage Load = 9.5 A dc**
119 V dc	107 V dc

The DACAG2 can be paralleled for greater output current. In parallel operation, current sharing between the two DACAs is critical. Uneven current sharing can cause one of the DACAs to operate beyond its output current rating.

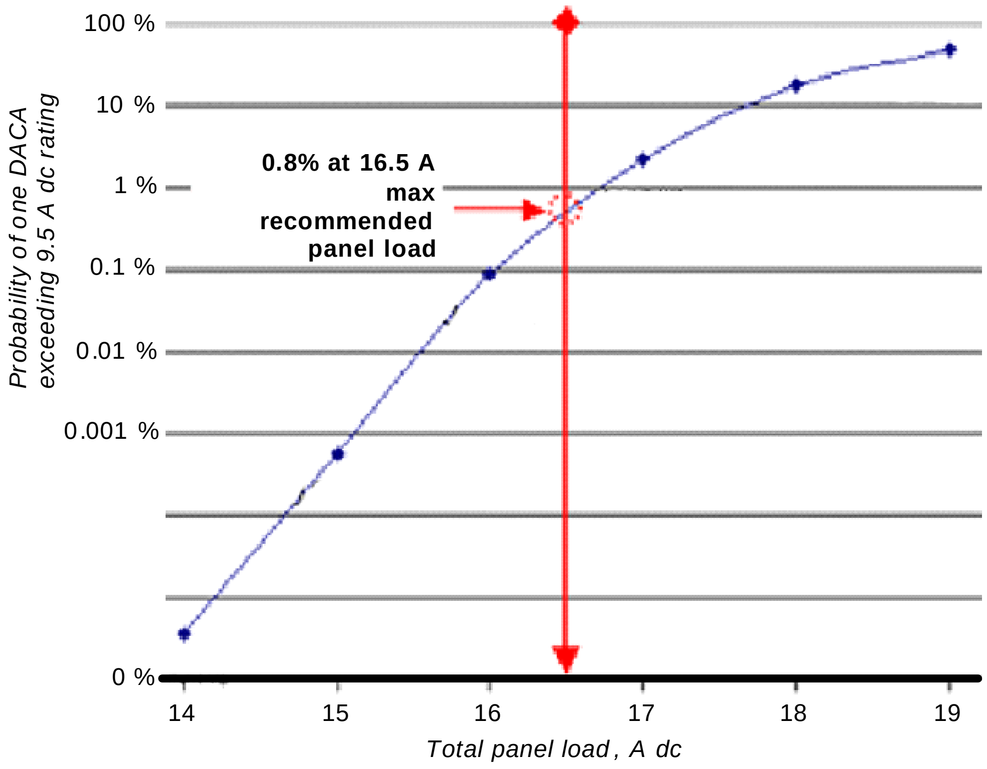
Two DACA Modules with Outputs Paralleled, Maximum Output Current is 16.5 A dc†

Input to DACA V ac rms	**Input Current at Max Load**	**Output Voltage Load = 1 A dc**	**Output Voltage Load = 15 A dc**
115 V ac	20 A	120 V dc	110 V dc
230 V ac	11 A		
† The two paralleled DACAs must be connected to one ac voltage source for even output current sharing.			

For proper implementation of parallel DACAs, the following must be observed:

- The DACAs must be connected to the same ac source to ensure equal input voltages to the DACAs.
- The maximum output current per DACA is derated for parallel operation. This derating accounts for variance in DACA open circuit voltages and variance in DACA output impedances. The following curve should be used. The maximum recommended total panel current is 16.5 A dc.

Probability of overloading one DACA when two DACAs are paralleled; plotted at various panel loads



18.4.4 Specifications

Item	DACA Specification
Input Voltage	105-132 V ac or 210-264 V ac, 47 to 63 Hz
Output Voltage	90 to 140 V dc with a load of 1 to 9.5 A Over the full range of input voltage
Output Current Rating	9.5 A dc, -30 to 45°C (-22 to 113 °F) Linearly derate to 7.5 A dc at 60°C (140 °F)
Output Ripple Voltage	4 V p-p
Discharge Rate	Nominal input of 115 or 230 V ac, no load, discharge to less than 50 V dc within 1 minute of removal of input power.
Hold Up (time for output to discharge to 70 V dc with constant power load)	V in (V ac) 105 115 132 Initial Load (A dc) 9.5 9.5 9.5 Pout (W) 882 974 1131 Hold Up Time (ms) 19.5 29.5 48.8
Ambient Rating for Enclosure Design†	-40 to 70°C (-40 to 158 °F) free convection
Humidity	5 to 95%, non-condensing
Electrical Safety and EMC	UL 508C Safety Standard Industrial Control Equipment CSA 22.2 No. 14 Industrial Control Equipment EN 61010 Section 14.7.2 – Overload Tests EN 61010 Section 14.7.1 – Short Circuit Test EN 61000-4-2 Electrostatic Discharge Susceptibility EN 61000-4-3 Radiated RF Immunity EN 61000-4-4 Electrical Fast Transient Susceptibility EN 61000-4-5 Surge Immunity EN61000-4-6 Conducted RF Immunity EN 50082-2:1994 Generic Immunity Industrial Environment ENV 55011:1991 - ISM equipment emissions IEC 529 Intrusion Protection Codes/NEMA 1/IP 20

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

18.4.5 Configuration

Input voltage selection is made on DACA by plugging the captive cable harness into connector JTX1 for 115 V ac nominal input or connector JTX2 for 230 V ac nominal input.

18.5 JPDA Local AC Power Distribution

18.5.1 Functional Description

The Local ac Power Distribution (JPDA) board provides ac power distribution, power isolation, and branch circuit protection for each control or I/O function requiring ac power. Typical applications include ac relay and solenoid control power, ignition transformer excitation, and contact wetting. Each output includes a fuse, a switch for power isolation, and a lamp to indicate the presence of output voltage.

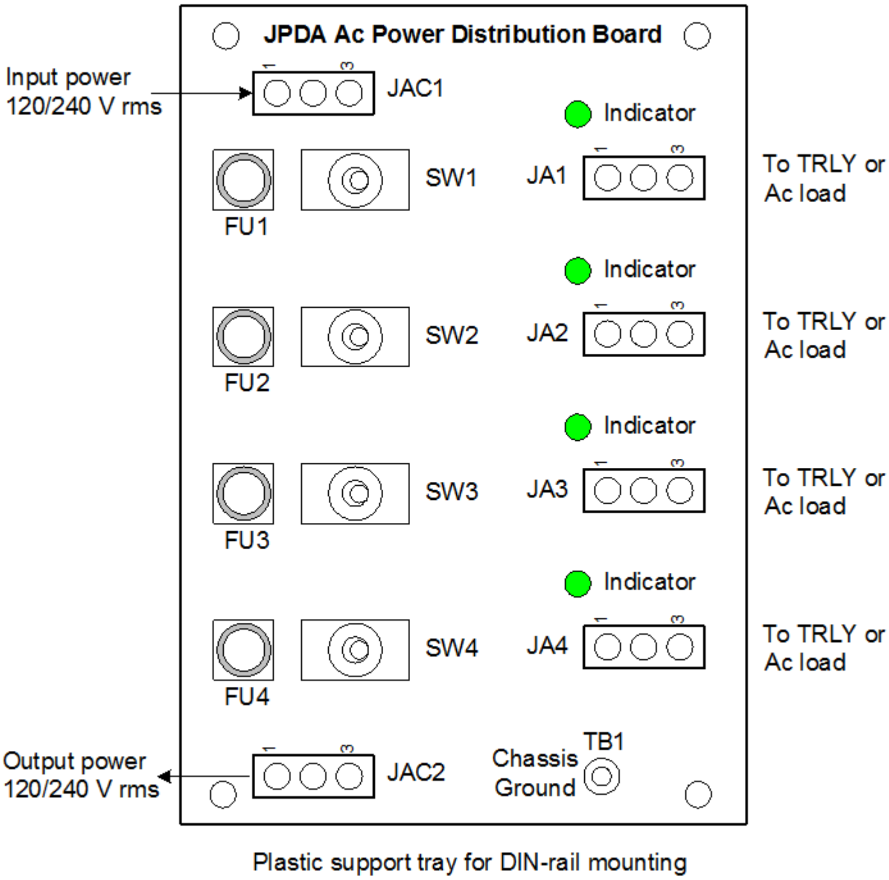
18.5.1.1 Board Versions

Terminal Board	Fusing
JPDAG1	Each circuit provided with 31.75 x 6.35 mm (1.25 x 0.25 in) 15 A 250 V fuse
JPDAG2	Empty fuse holders with black caps accepting 5 x 20 mm (0.20 x 0.79 in) fuses
JPDAG3	Empty fuse holders with grey caps accepting 31.75 x 6.35 mm (1.25 x 0.25 in) fuses

JPDAG1 provides fuses that are coordinated with the rating of the system wiring and connectors. JPDAG2 and G3 are used when fuse ratings coordinated with a specific application are required. Two different fuse sizes are provided for to best accommodate local fuse preferences.

18.5.2 Installation

JPDA mounts in a plastic holder, which fits on a vertical DIN-rail.



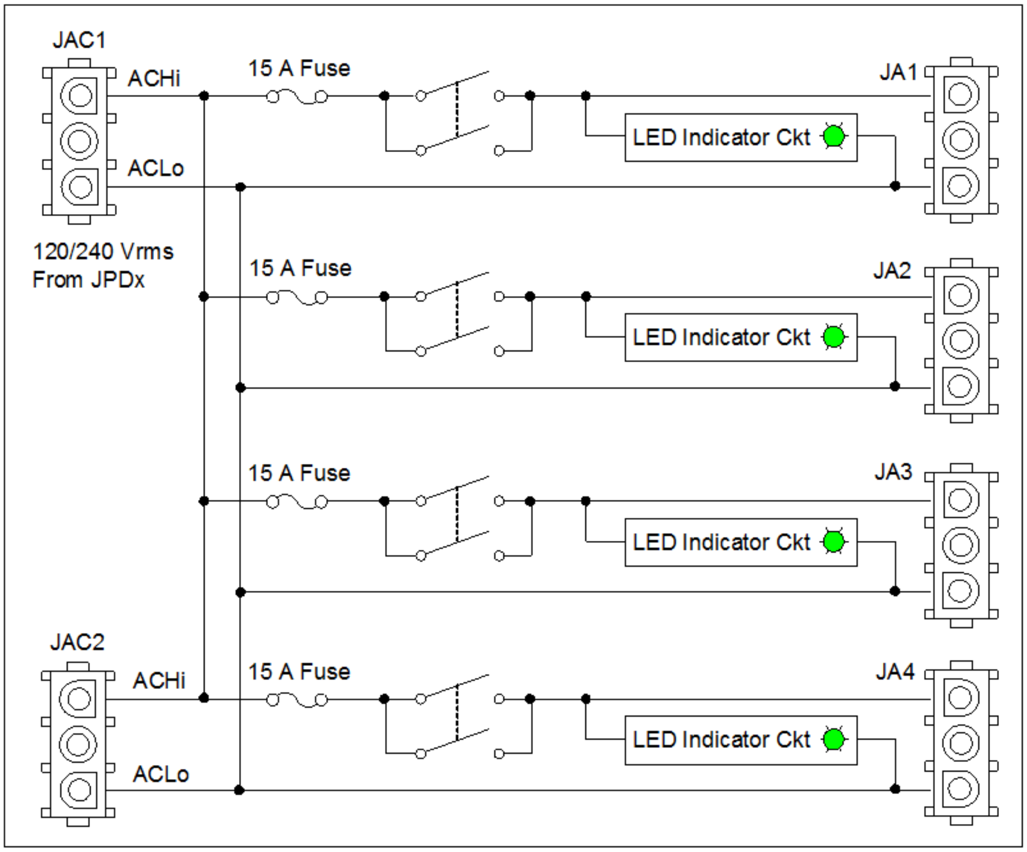
JPDA Cabling

Power input and output cables have three-position Mate-N-Lok connectors. For cable destinations, refer to the circuit diagram.

TB1 is the chassis ground connection. When installing the JPDA it is important to provide a ground lead from TB1 to the system PE. This creates a ground path for the metal switch bodies.

18.5.3 Operation

The following figure explains how the 120/240 V rms power is distributed in JPDA, and how it reaches the TRLY board or ac load.



JPDA Simplified Circuit Diagram

18.5.3.1 Inputs

Multiple JPDA boards receive power from a single JPDM Main Power Distribution Module. This power input is either 120 V rms or 240 V rms, 50/60 Hz.

Two 3-Pin Mate-N-Lok connectors are provided. One connector receives ac input power and the other can be used to distribute ac power to another JPDA board in daisy chain fashion. It is expected that the low or neutral side of the input power is grounded.

18.5.3.2 Outputs

Four output circuits are provided with three-pin Mate-N-Lok connectors. Each output circuit includes branch circuit protection, and a pair of isolation contacts for the non-grounded line. There is also a green lamp to indicate the presence of voltage across the output terminals.

18.5.4 Specifications

Item	**JPDA Specification**	
Inputs	One 3-pin connection for input power from JPDB and JPDC	120 or 240 V rms, 15 A limit
Outputs	Four 3-pin connections for TRLY and ac loads One 3-pin connection for output power to another JPDA board	120 or 240 V rms, fused 15 A 120 or 240 V rms
Fuses Do not use more than a 15 A fuse.	Four fuses, one per output, Bussmann® ABC-15 A typical Refer to the section, *Board Versions*.	
Ambient Rating for Enclosure Design†	-40 to 70ºC (-40 to 158 ºF)	
Board Size	15.875 cm high x 10.795 cm wide (6.25 in x 4.25 in)	
Mounting	DIN-rail, card carrier mounting Base mounted steel bracket, 4 holes	

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

18.5.5 Configuration

There are no jumpers on the JPDA. Check the position of the four output load switches.

It is possible to use other fuse ratings with this board to provide specific branch circuit ratings. A typical series of fuses that work with this board are the Bussmann ABC series of fuses with ratings from .25 A through 15 A. Do not use fuses above 15 A with this board. If alternate fuse ratings are used, configuration of the board requires the insertion of the proper fuse in each branch circuit.

18.6 JPDB AC Power Distribution

18.6.1 Functional Description

The JPDB ac power distribution board conditions, monitors, and distributes ac power. The board contains two line filters and a IS200JPDB circuit board. The module features two separate ac distribution circuits, each rated for 20 A at 115 or 230 V ac. The input circuits should be wired in parallel to avoid PPDA alarms when a single source of ac power is provided.

For each circuit, one fused, and three fused and switched branch circuit outputs are provided. Connection to an optional JPDF 125 V dc distribution module is provided. The IS200JPDB includes passive monitoring circuits for both ac magnitudes as well as status feedback for all fused circuits. The monitoring circuits are on connector P1, compatible with cable connection to a board containing a power diagnostic PPDA I/O pack. IS200JPDB also has a P2 connector for pass-through of monitoring signals from other power distribution system cards.

Two JPDB modules could be cabled into a single PPDA I/O pack when needed.

IS2020JPDBG2 provides an additional connector when an ac source selector is required in a system. The connector intercepts the two ac sources supplied to JPDB and routes them to the JSS1 connector on the board edge. Output of the ac selector is then wired to JSS1 and conducted to the individual branch circuit outputs.

Note Circuit breakers are not provided as part of the basic IS2020JPDB module. Options exist to provide circuit breakers on a mounting plate that fastens to the JPDB sheet metal support. Please refer to job specific documentation for information regarding any circuit breakers attached to JPDB.

18.6.1.1 Compatibility

The IS2020JPDB is compatible with the feedback signal P1/P2 connectors on JPDE, JPDF, JPDS, and JPDM leading to a PPDA I/O pack. Connector JAF2 is compatible with the ac input on the JPDF module of the same name.

Note AC1H should be connected to LINE and AC1L should be connected to NEUTRAL.

18.6.2 Installation

Caution

In 240 V ac applications, do not inadvertently cross-connect the 240 V ac and the dc voltages. The peak voltage will exceed the Transorb rating, resulting in a failure.

Most ac supplies operate with a grounded neutral, and if an inadvertent connection between the 125 V dc and the ac voltage is created, the sum of the ac peak voltage and the 125 V dc is applied to Transorbs connected between dc and ground. However, in 120 V ac applications, the Transorb rating can withstand the peak voltage without causing a failure.

The IS2020JPDB module is base-mounted vertically on a metal back base in a cabinet used by the PDM. A connection must be made between the IS2020JPDB sheet metal and the system Protective Earth.

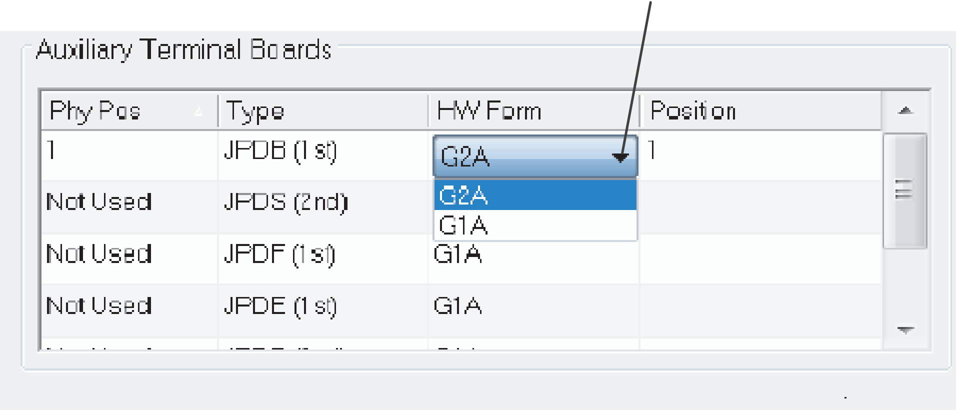
Input power is applied to terminals AC1H (line) and AC1N (neutral) for the first ac circuit, and AC2H (line) and AC2N (neutral) for the second ac circuit. Both ac inputs are required to have grounded neutral connections. Output circuits are connected as documented for the system.

If the power distribution system includes a PPDA power diagnostic I/O pack, a 50-pin ribbon cable is required from JPDB connector P1 to the P2 connector on the board holding PPDA. It is permissible for this connection to pass through other core PDM boards using the P2 connector.

18.6.2.1 Grounding

The Mark VIe and Mark VIeS control systems uses protective earth (PE) and functional earth (FE) grounding. The PE ground must be connected to an appropriate earth connection in accordance with all local standards. The minimum grounding must be capable of carrying 60 A for 60 seconds with no more than a 10 volt drop. The FE ground system must be bonded to the PE ground system at one point.

The JPDB is grounded through metal mounting supports fastened to the underlying sheet metal of a metal module. The ground is applied to the metal switch bodies on JPDB. Additionally, the ground is used as a local reference point when creating the feedback signals appearing on P2. The sheet metal of the module is insulated to the surface upon which it is mounted. This is done specifically to allow definition of the JPDB ground independent of the mounting surface. Typically, JPDB is mounted to a back base grounded to FE. JPDB would be located low in the cabinet and a separate ground wire from the JPDB module would be provided to PE. The minimum length of the ground wire is important to keep impedance low at radio frequencies, this allow the input line filters to function properly.



JPDB may be selected with the G1A or G2A option. During configuration of PDM with JPDB, from the HW Form drop down menu, be sure to select the version that matches the hardware

Auxiliary Terminal Boards

Phy Pos	Type	HW Form	Position
1	JPDB (1st)	G2A	1
Not Used	JPDS (2nd)		
Not Used	JPDF (1st)	G1A	
Not Used	JPDE (1st)	G1A	

18.6.2.2 Physical Arrangement

When JPDB is used with an optional source, the selector should be positioned above the JPDB, thus allowing a short power connection between the two components using the JSS1 connector. When JPDB is used with a JPDF (125 V dc) board, the JAF1 connector provides ac power to JPDF. The best location for JPDF in this arrangement is below the JPDB, to minimize wiring lengths. The P1 and P2 ribbon cable headers on all of the JPDB boards are positioned, so the JPDG and JPDC holding the PPDA I/O pack is best located at the top of the board arrangement. This allows ribbon cables to flow from one card to the next, exiting the top, and entering the bottom of the next card until the PPDA host is reached. Connector P1 transmits feedback signals to a board hosting a PPDA I/O pack. Connector P2 receives feedback from other power distribution boards and passes the signals out of P1 to the PPDA.

18.6.2.3 JPDB Application Notes

When JPDB is used with a single ac input, the two ac inputs should be wired in parallel to the source. All output branch circuits are now live and there can be no diagnostics generated. If only one ac input is used, a diagnostic for loss of ac on the un-switched branch circuit can appear.

With ControlST V03.05 and later, a *InputDiagEnab* configuration bit was added to disable all diagnostics for a specified input (AC1 or AC2). Therefore, wiring the ac input signals in parallel is no longer needed.

18.6.2.4 PPDA Configuration for JPDB Feedback

Input variable *AC_Fdbk#_Volt* is measured from the input line voltage to the potential of local protective earth. If there is a voltage difference between PE and the ac grounded neutral voltage, *ACDiffVoltOff* compensates for the difference. The nominal bus voltage can be entered for each of the two buses and an *ACFdbkInTol* configuration parameter may be selected to operate at 5, 10, or 20% of nominal voltage. Each of the six switched outputs may have their diagnostic feedback disabled by changing the respective value of *FuseDiag* from its default of enabled to disabled. Make this change, if an output is expected to be switched on and off and a nuisance diagnostic alarm is not desired.

18.6.3 Operation

Caution

It is not recommended to use floating ac input with JPDB.

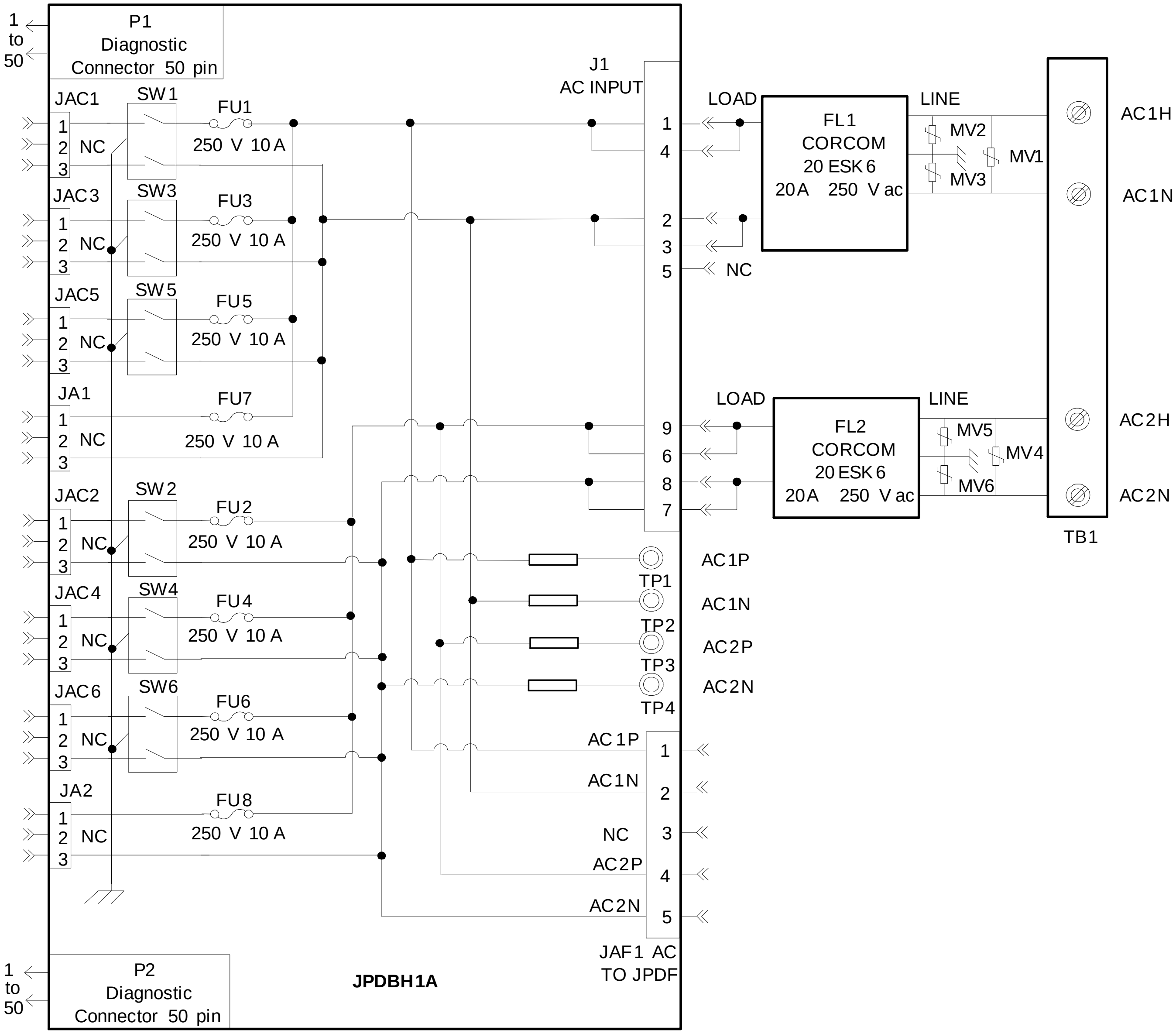
Two sources of ac power are wired to a terminal board on the right side of the JPDB module. The ac power goes to the ac line filter assemblies underneath the IS200JPDB circuit board. A wire harness connects the filter assemblies to the JPDB circuit board J1 connector.

The IS2020JPDBG01 module uses the IS200JPDBH1A circuit board. This board does not provide connection for an ac source selector and J1 ac power is wired directly to the output branch circuits.

The IS2020JPDBG02 module uses the IS200JPDBH2A circuit board. The board is designed for use with an ac source selector. It features the JSS1 connector mounted to the board. External filtered ac from connector J1 is fed to JSS1. The source selector output returns to the JSS1 to supply the branch circuit outputs.

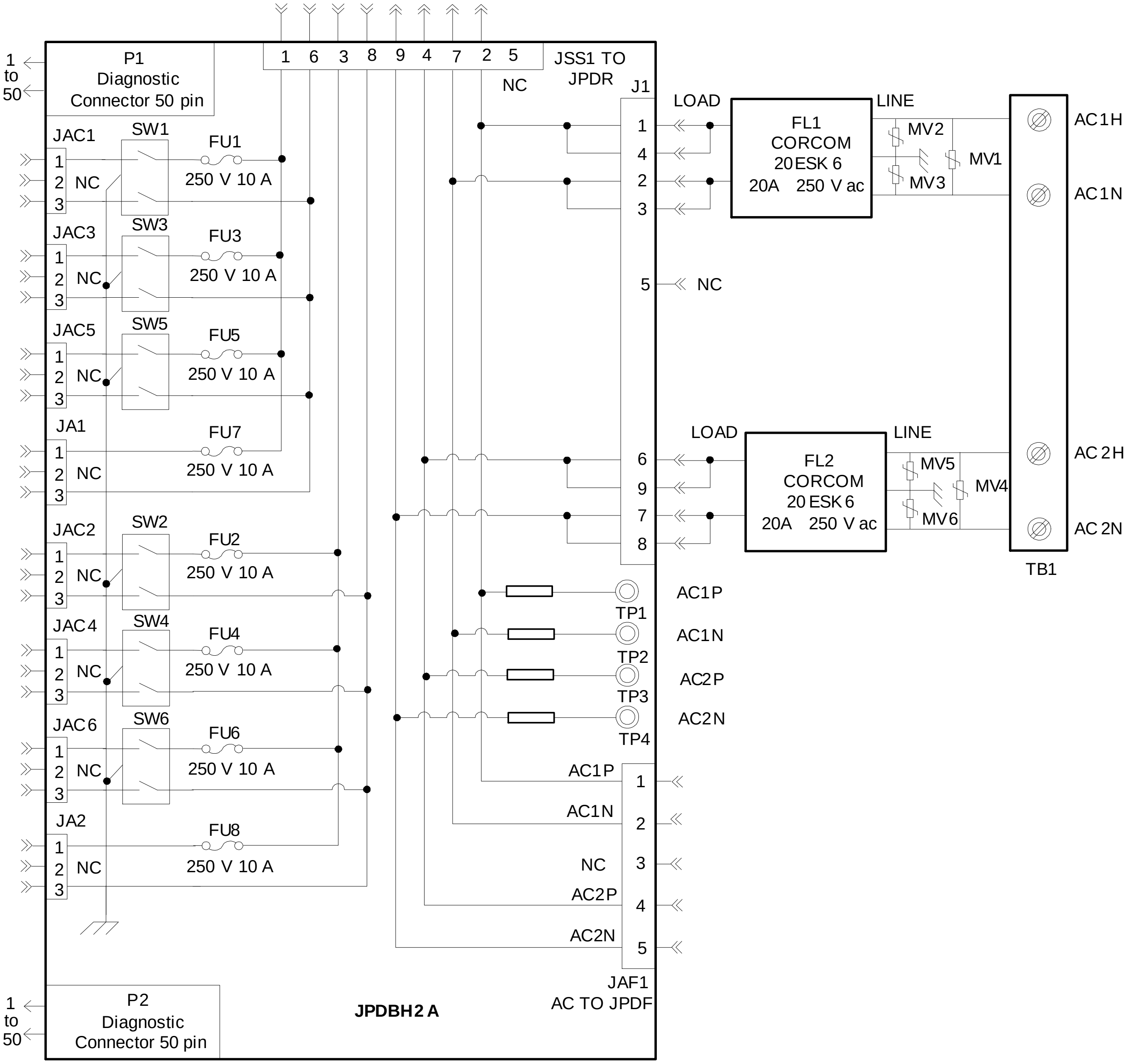
JAF1 feeds power directly from input connector J1 to an adjacent optional JPDF board to power two DACA power conversion modules. The DACA modules convert the ac power to 125 V dc to be used as an ac backup for systems using a 125 V dc battery.

The following figure displays the JPDBG01 module with the JPDBH1A circuit board. The JPDBH1A has jumpers to conduct power from J1 to the output circuits, while maintaining two independent ac circuits.

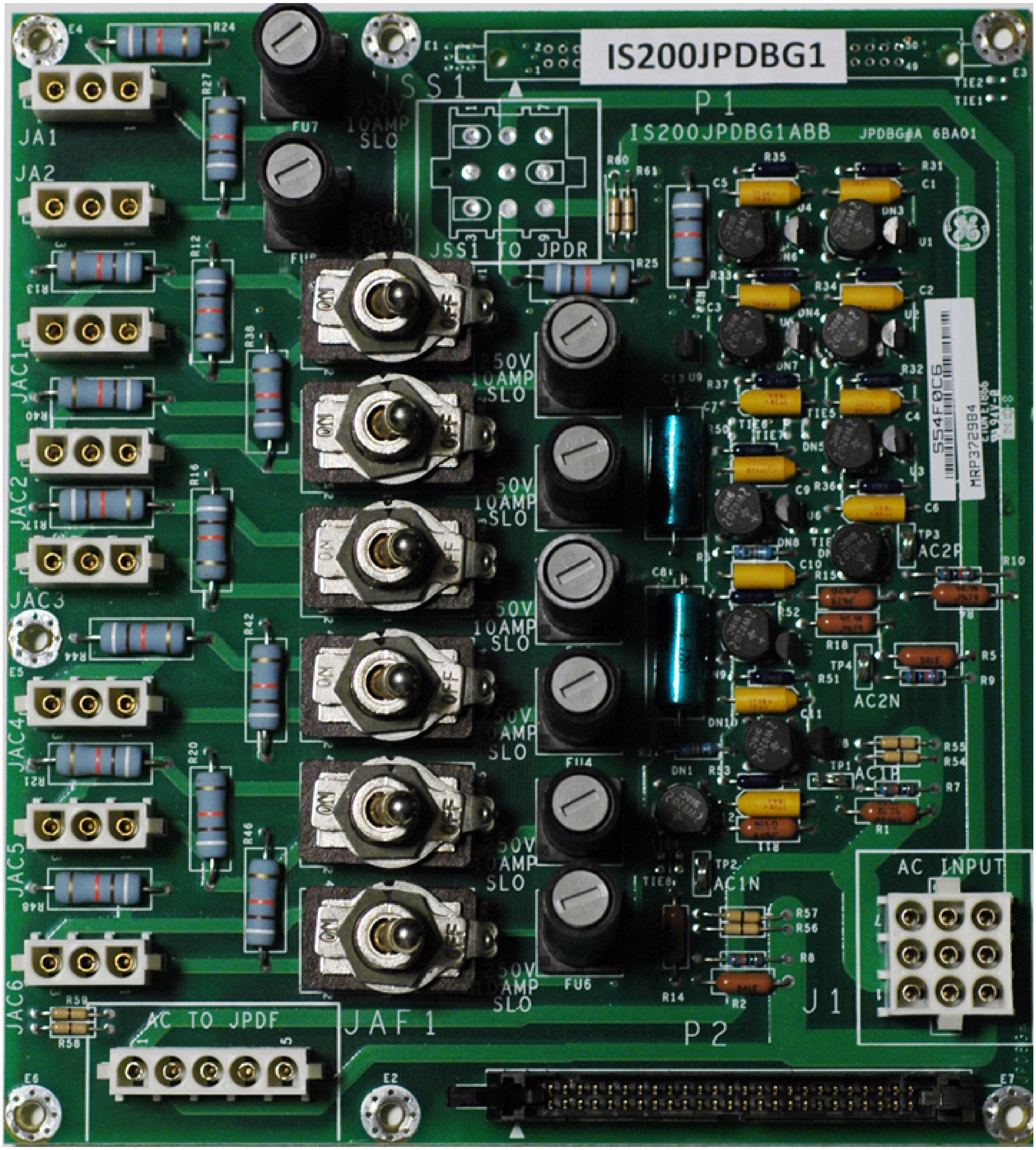


JPDBG01 Module with JPDBH1A Board

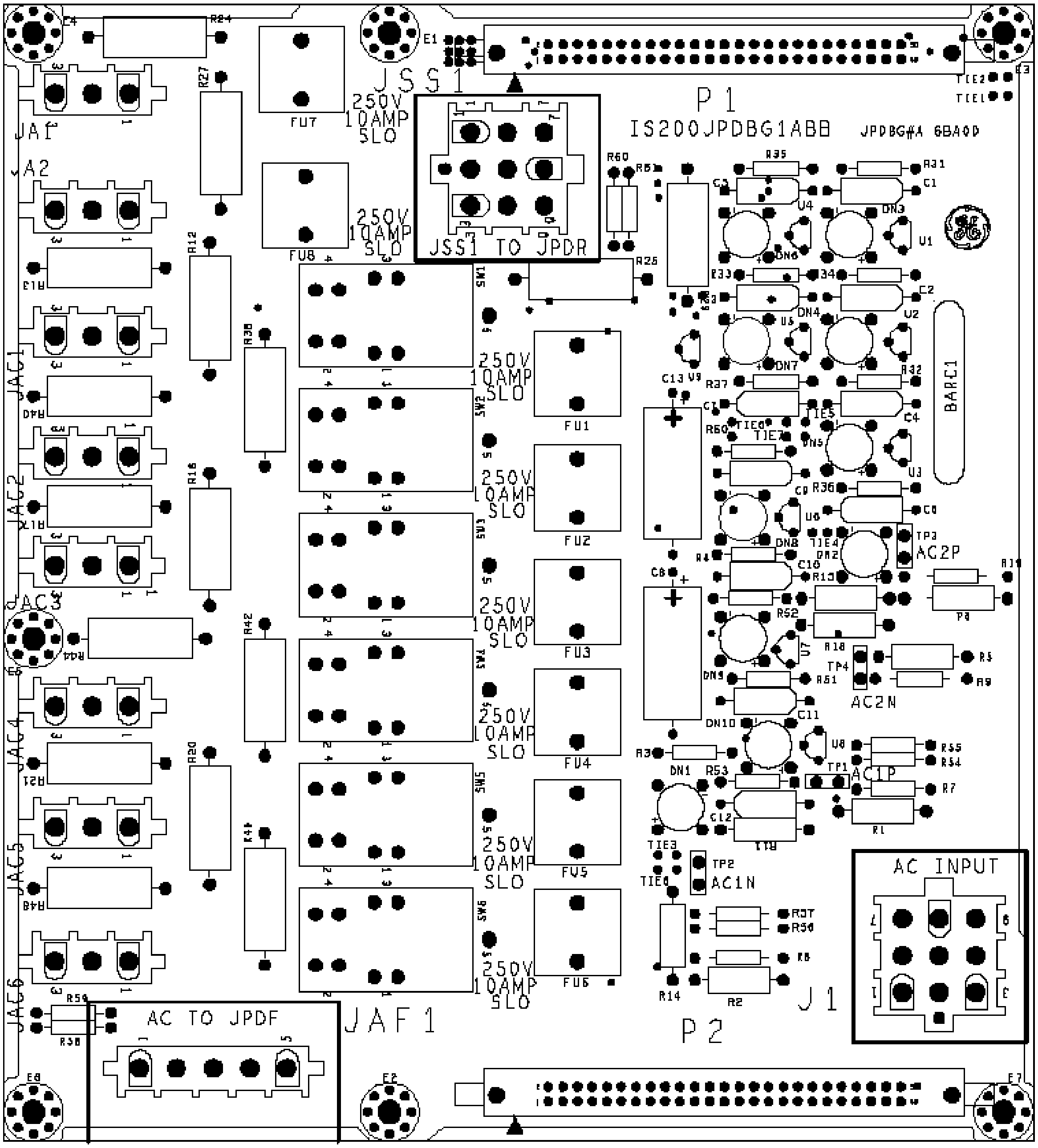
The following figure displays the JPDBG02 module with the JPDBH2A circuit board, including connection for an ac source selector.



JPDBG02 Module with JPDBH2A Board


IS200JPDBG1
IS200JPDBG1ABB
JSS1
JSS1 TO JPDR
P1
P2
J1
JA1
JA2
JAC1
JAC2
JAC3
JAC4
JAC5
JAC6
JAF1
AC TO JPDF
AC INPUT
250V 10AMP SLO
FU4
FU6
FU7
AC1P
AC1N
AC2P
AC2N

JPDB Photo



Mechanical Layout

18.6.3.1 JPDB Connections

- A terminal strip (TB1) mounted with the JPDB module has two ac input screw terminal pairs. These terminals are rated at 20 A RMS. Branch circuit protection can be no larger than a 30 A circuit breaker. The rating for the ac circuits is 100 to 250 V ac, 20 A for each of the two circuits feeding JAF1. The circuits use a grounded neutral connection.
- A nine-position Mate-N-Lok connector, J1, accepts power from line filters into the JPDB board. Dual pins are used for each connection point to support the current rating. J1 comes with a wire harness that is part of the module. Refer to previous wiring diagrams for proper hookup.
- A five-position Mate-N-Lok connector, JAF1, provides direct ac power output. This connector matches the one on the JPDF board. Ac current passes through the JPDF board providing ac to dc conversion using DACA modules.
- A nine-position Mate-N-Lok connector, JSS1, is included on the JPDBH2A board and provides a connection point for an external ac source selector. The JSSI connector is not used on the JPDBH1A board and there is no connection for a source selector.
- Two un-switched ac outputs, JA1 and JA2, are provided with each ac circuit using a three-pin Mate-N-Lok connector to feed optional JPDA branch circuit boards. The circuits are fused and rated at 10 A/250 V.
- Six switched and fused output connectors, JAC1 through JAC6, are provided with each using a three pin Mate-N-Lok connector. Fuses are rated at 10 A/250 V. Additionally these connectors could be used to feed ac/28 V dc power converters making I/O pack control power.
- Two 50-pin diagnostic ribbon cable connectors, P1 and P2, are supplied on the top and bottom of the board. Connector P1 transmits feedback signals to a board hosting a PPDA I/O pack. Connector P2 receives feedback from other power distribution boards and passes the signals out of P1 to the PPDA.

18.6.4 Specifications

Item	JPDB Specification
Board Rating	100 to 250 V ac 50/60 Hz 30 A circuit breaker protection
Total AC Circuit Loading	10 A on JAF1 AC1 plus 20 A total on JA1+JAC1+JAC3+JAC5 10 A on JAF1 AC2 plus 20 A total on JA2+JAC2+JAC4+JAC6
Fuse for Connectors JAC1-JAC6 and JA1-JA2: FU1-FU8	10 A on 250 V, Bussmann MDA-10 typical
Module Dimensions	26.41 cm High x 21.33 cm Wide x 16 cm Deep (10.4 in x 8.4 in x 6.3 in)
Mounting	Four mounting holes, #10 screws
† Ambient rating for enclosure design	-40 to 70°C (-40 to 158 °F)

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

18.6.5 Diagnostics

Diagnostic signals routed into the PPDA through connector P1 include:

- An electronic ID identifying the board type, revision, and serial number
- Two 100 to 250 V ac analog feedbacks
- Six switched/fused ac supply indications yielding six Boolean values after PPDA decodes the signals
- Two fused ac supply indications yielding two Boolean values after PPDA decodes the signals
- A local ground signal for sensing analog signals

Additional core PDM board feedback passes through JPDB using the P2 connector. Test points with 100 k series resistors are provided to allow connection of testing equipment:

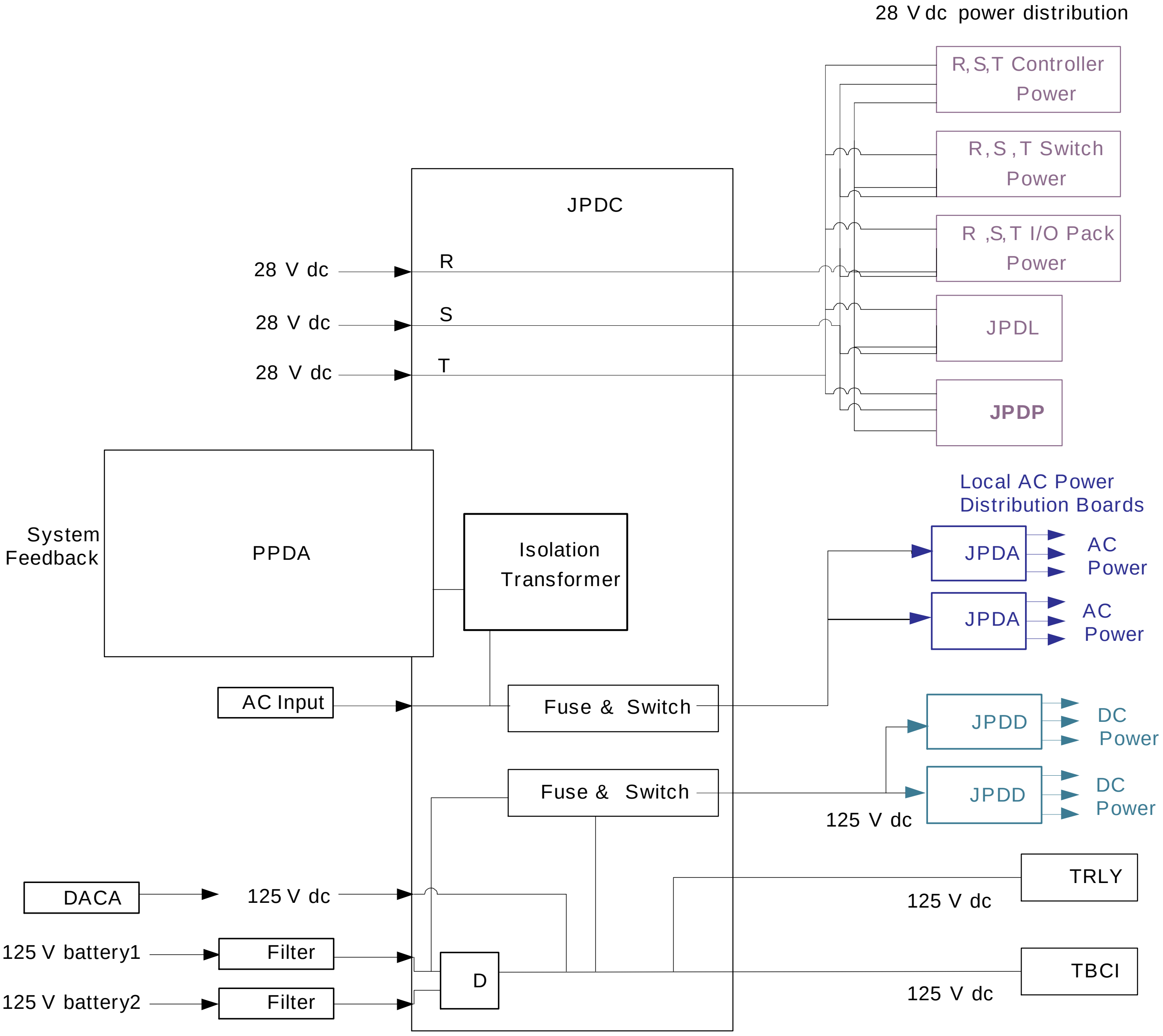
- TP1 is the AC1 line
- TP2 is the AC1 neutral line
- TP3 is the AC2 line
- TP4 is the AC2 neutral line

Note FU1, FU3, FU5, and FU7 are fuses in series with AC1. FU2, FU4, FU6, and FU8 are fuses in series with AC2. A fuse failure diagnostic will not be generated if *InputDiagEnab* on the ac input is set to Disable or ac input is below the lower tolerance limit set for the respective ac 1 or 2 input.

18.7 JPDC Core Power Distribution

18.7.1 Functional Description

The IS2020JPDC Power Distribution Module (JPDC) combines input and output functions from several previous designs to provide distribution of 125 V dc, 115/230 V ac, and 28 V dc to other boards within the control system.



PDM with JPDC Basic Layout

18.7.1.1 Compatibility

JPDC can host a Power Distribution System Feedback (PPDA) pack used in the Mark VIe and Mark VIeS power distribution systems. JPDC can also receive diagnostic feedback signals from other distribution boards and route these signals to the PPDA I/O pack.

The intent is that the PPDA I/O pack should be mounted on the JPDC. Therefore, no provision is made to transmit diagnostic signals from JPDC to another distribution board.

18.7.1.2 JPDC Versions

IS2020JPDCG01: Standard version for most applications.

IS2020JPDCG02: Special version which includes a wire jumper on the D1 diode assembly. The jumper permits the JD2 *Battery B* input connector to be used as an output connector.

The IS2020JPDC module contains the IS200JPDCG1Axx board. Revisions IS200JPDCG1A**DC** and higher have the following changes:

- In the diagnostic signal path, *A5* (AC1 feedback magnitude), a signal isolation transformer is added. This provides galvanic isolation between FE/PE and JAC, the ac line connection.
- With the addition of the isolation transformer, the AC1 feedback signal displayed in the ToolboxST application has a tolerance of ±15%, relative to the reading.

18.7.2 JPDC I/O Characteristics

- 125 V dc power inputs are provided by JD1 and JD2. The connectors use pins 1 and 2 for positive dc, and use pins 3 and 4 for negative dc.
- Three fused and switched two-pin Mate-N-Lok connectors (J1R, J1S, and J1T) are provided to power the 125 V dc to 28 V dc power supplies or other loads. Pin 1 is 125 V, and pin 2 is the return. Fusing is 10 A, sized to protect the wiring. These three connections have an additional dc/dc source select option associated with them. If connector JDB has pin 1 and 2 connected, then the power to J1R, J1S, and J1T is provided after the two dc inputs and DACA module input are combined into a single bus. If the connection is removed from JDB and placed on JDA, the power is taken only from the JD1 power input. There is a specific application choice addressed by this option. If dual dc inputs are used to power JPDC and dual redundant dc/dc power supplies are used for 28 V I/O pack power, then the short on JDB should be used. If a dc battery and ac powered DACA are used to make the 125 V dc, it may make more sense to use one battery fed dc/dc supply and one ac/dc supply to make redundant 28 V. Moving the jumper connector to JDA means the dc/dc supply will not be powered through DACA and the power budget can be much smaller.
- Three two-pin Mate-N-Lok outputs J8A-J8C are provided to operate TBCI contact input boards. Positive power is on pin 1, negative power is on pin 2. The clearances of the TBCI board dictate a known source impedance for the 125 V dc input, provided by resistors in the module. Two 22 Ω resistors provide fault current protection for the system TBCI boards. While 3.15 A fuses are supplied on JPDC, they should never open under fault conditions due to the current limit imposed by the resistors. These outputs are also suitable for powering trip input contacts on TREG or WREA mounted on TRPA.
- Three fused and switched two-pin Mate-N-Lok connectors (J7A, J7B, and J7C) are provided for relay board loads. Pin 1 is 125 V, and pin 2 is the return. Fusing is 10 A, sized to protect the wiring.
- Connector JAC provides ac power input, with pin 1 as the line input, pin 2 no-connect, and pin 3 as neutral.
- One fused ac output JAC2 uses a three-pin Mate-N-Lok connector. Fusing is 10 A 250 V in the line side only. This connector is typically used to feed a JPDA fan-out board where individual branch switches are provided. Pin 1 is the line, Pin 2 is not connected, and Pin 3 is neutral.
- One switched and fused ac output JAC1 is provided, using a three-pin Mate-N-Lok connector. Fusing is 10 A 250 V in the line side only. This connector will typically be used to feed devices such as an ac 28 V dc power converter making I/O pack control power. Pin 1 is the line, Pin 2 is not connected, and Pin 3 is neutral.
- Connector JZ2 is provided for connection of a single DACA ac to dc module. It uses the standard 12 pin connector found on DACA so a 1:1 cable can be used. Pin 1 is ac line, pin 3 is ac neutral, pins 9 and 12 are positive dc, and pins 7 and 10 are negative dc. All other pins are no-connect. No branch circuit protection is included in these signal paths.
- Three power supply inputs are provided on JR, JS, and JT. The connectors use pins 8 and 9 for positive 28 V and pins 1-3 for 28 return, providing 24 A steady state capacity. No branch circuit protection is present in these inputs. The connectors include low-level signals capable of interrogating status switches on each supply and generating a feedback signal to PPDA. Pin 4 provides positive 10 V wetting to the switch with overcurrent protection and return on pin 5. Pins 6 and 7 are not connected.
- Terminal board TB1 provides access to the three 28 V dc power buses. If it is desired to have a single power bus fed by redundant supplies, jumpers may be placed between PR, PS, and PT terminals to tie the positive bus terminals together. Connection is direct without branch circuit protection.
- DC62 connector JA1 is for a PPDA power diagnostic I/O pack. It contains the status feedback signals for JPDC plus up to four additional core power distribution boards.
- P4 is provided to supply power to the PPDA I/O pack. It is a power circuit formed from R, S, and T power using a diode-or arrangement followed by a polysilicon self-resetting fuse (rated at nominal 0.5 A at 20 °C, 0.28 A at 70 °C) to

handle the PPDA power requirements. This ensures that the I/O pack receives power if any of the three 28 V power buses are active.

- When used, the JPDC is the intended location of the PPDA. The JPDC does not have a P1 connector to send its feedback signals to a PPDA on another board.
- Diagnostic daisy chain 50-pin ribbon cable connector P2 is located at one end of the board. It allows connection of other PDM board feedback signals for pass-through to PPDA

- One Mate-N-Lok connector J2 with six pins is provided to supply R, S, and T power to remote JPDP or JPDH boards or directly to JPDL boards when used with the appropriate wire harness. Connector pins 1-3 are 28 V return, pin 4 is 28 R, pin 5 is 28 S, and pin 6 is 28 T. No branch circuit protection is provided in the power outputs.
- One Mate-N-Lok connector JP1 with five pins is provided to supply R, S, and T power to a string of one or more JPDL cards. Connector pins 4 and 5 are 28 V return, pin 1 is +28R, pin 2 is +28S, and pin 3 is _28T. No branch circuit protection is provided in the power outputs.
- A total of 26 two pin mini Mate-N-Lok connectors are provided for I/O pack power output. JR1-10 are on power bus R, JS1-8 are on power bus S, and JT1-JT8 are on power bus T. A polysilicon self-resetting fuse (rated at a nominal 1.6 A at 20 °C, 0.86 A at 70 °C) protects each output.
- Three two-pin Mate-N-Lok connectors are provided for 28 V controller power output. JCR, JCS, and JCT are connected to the R, S, and T power buses with pin 1 positive and pin 2 the return. No branch circuit protection is provided in the power outputs.
- Three two-pin Mate-N-Lok connectors are provided for 28 V Ethernet switch power output. JRS, JSS, and JTS are connected to the R, S, and T power buses with pin 1 positive and pin 2 the return. No branch circuit protection is provided in the power outputs.
- JP2 when closed provides resistive voltage centering for a floating 125 V dc bus. When open, the relationship between 125 V dc and earth must be established elsewhere.

- A row of Euro-style box terminals is located next to the P2 connector on one end of the board. The purpose of these terminals is to provide access to feedback signals if it is desirable to eliminate the PPDA I/O pack in cost sensitive applications. In place of PPDA the signals may be wired into available control voltage input points. The following signals are available:
  - TB2 pin 1 positive 125 V dc feedback voltage relative to functional earth with 0.016667 volts per volt scaling.
  - TB2 pin 2 negative 125 V dc feedback voltage relative to functional earth with 0.016667 volts per volt scaling.
  - TB2 pin 3 ac line voltage feedback relative to functional earth, rectified and filtered with scaling 0.0194 volts dc per volt ac
  - TB3 pin 1 functional earth
  - TB3 pin 3 functional earth.
  - TB4 pin 1 28 V dc bus R feedback relative to functional earth with 0.14286 volt per volt scaling.
  - TB4 pin 2 28 V dc bus S feedback relative to functional earth with 0.14286 volt per volt scaling.
  - TB4 pin 3 28 V dc bus T feedback relative to functional earth with 0.14286 volt per volt scaling.

18.7.2.1 JPDC Diagnostic Features

JPDC is somewhat different than other JPDx power distribution boards. Only one JPDC is supported at a time by a PPDA. In addition, the PPDA must be located on the JPDC because the JPDC does not support output of feedback signals through a P1 diagnostic feedback connector. It is possible to use JPDC with limited status feedback without PPDA using the signals on TB2, TB3, and TB4. The following signals are created by JPDC:

- An electronic ID identifies the board type, revision, and serial number.
- PS28vStat_R, _S, _T are three analog P28 voltage readings for R, S, and T bus. Separate analog feedback signals (parameter PS28vEnable) are used. Accuracy is specified to be ±1% of full scale and calculated accuracy is ±0.2% at 3 sigma.
- There are two analog 125 V dc voltage feedbacks. One for the positive bus with respect to earth, one for the negative bus with respect to earth. PPDA uses these signals to create two different signals: voltage magnitude *DC_125VFdbkMag* (difference between positive and negative) and voltage offset indicative of a system ground. *DC_125VFdbkMag* has parameters *InputDiagEnab* and *DC_125V_Trig_Volt*. *Gnd_125VFdbkMag* has parameter *Gnd_Mag_Trig_Volt*.
- The signal will read near zero volts with an earth centered floating 125 V dc power system. As the power is offset either positive or negative due to a ground fault, the value of *Gnd_FdbkMag* will show the voltage offset. Voltage feedback accuracy is specified at ±1% of 125 V and exceeds ±0.25% of 125 volts or ±0.32 volts. Each of these resistive attenuator strings contributes approximately 1.5 MΩ to the bus centering resistance.
- A problem that can occur in an installation is the possible cross-wiring of ac power and the 125 V dc bus. The system will often continue to operate since the dc is designed to float, but signal quality may be degraded and additional power system fault opportunities exist. The circuits on JPDF include special features to allow PPDA to detect the presence of ac on the dc bus and indicate the condition to the system. Detection is done by driving the positive bus voltage feedback signal to a negative value, a condition that will never occur without ac present. The PPDA I/O pack then detects this voltage and indicates the presence of ac on the dc power bus.
- There is one analog 115/230 V ac voltage feedback with ±5% accuracy of nominal rated voltage once conditioned by the PPDA I/O pack. Due to the slow speed of the PPDA analog inputs, the ac voltage is rectified and filtered to yield a magnitude signal. *AC_Fdbk1_Volt* has parameters *InputDiagEnab*, *ACFdbkInVoltage*, *ACFdbkInTol*, and *ACDiffVoltOff*.
- DryCntStat_R, _S, _T is one dry contact from each of three power supplies yields a single multiplexed dc feedback (1,2,4 weighting of feedback switches in analog value). This provides three Boolean values after PPDA decodes the signal.
- Three dc/dc fuse indications (multiplexed on one analog) yield the following three Boolean values after PPDA decodes the signal with parameter *FuseDiag*:
  - FU1R_FU2R_Stat
  - FU1S_FU2S_Stat
  - FU1T_FU2T_Stat
- Three TRLY fuse indications (multiplexed on one analog) yield three Boolean values after PPDA decodes the signal with parameter *FuseDiag* :
  - FU71_FU72_Stat
  - FU73_FU74_Stat
  - FU75_FU76_Stat
- Two 115 V ac out fuse indications (multiplexed on one analog) yield two Boolean values after PPDA decodes the signal:
  - FU_AC1_Stat
  - FU_AC2_Stat
- A *BAT_STAT* Boolean signal indicates if both 125 V dc sources are present ahead of the diodes, and it is multiplexed with the two ac Boolean values.
- There is a local ground signal for differential sensing of the above mentioned analog signals.

JPDC is a special case for feedback wiring. Due to the large signal count present on this board (8 fuses, 3 contacts, dc status, and 6 bus voltages) a single group of five analog board feedback signals are not adequate to transmit all of the information to PPDA. When JPDC hosts the PPDA I/O pack, it uses two groups of feedback signals limiting the system to a maximum of 4 additional PDM boards.

JPDC provides the following eight test point outputs for connection of external test equipment:

- TP1-ACH
- TP2-ACL
- TP3-PDC
- TP4-NDC
- TP5-28N
- TP6-28PR
- TP7-28PS
- TP8-28PT

The positive side test points include series 10 kΩ current limiting resistors. These allow access to all three 28 V power buses, the common return circuit, ac line and neutral, and both sides of the 125 V dc bus.

There are signals available on Euro-style box terminals that duplicate the information sent to the PPDA connector. When using the JPDC without a PPDA I/O pack, a reduced set of feedback information may be obtained through these signals wired into analog input points on the control.

18.7.2.2 Physical Arrangement

JPDC is designed with a narrow width to enable mounting on the sides of remote junction boxes. JPDC is designed to accept power input from cables into the JR, JS, and JT connectors so it exhibits less mounting position sensitivity than some other boards. It is expected that the mounting surface will be at functional earth potential. If the board hosts a PPDA I/O pack, consideration should be given to visibility of the indicator lights on the top of PPDA.

18.7.2.3 JPDC Application Notes

In TMR systems it is generally desirable to maintain separate R, S, and T power systems throughout the control. When used this way, JPDC will have three power supply inputs and the barrier terminal will not be used to connect the three separate supplies. In dual systems it is common to use dual redundant power supplies for 28 V power. When this is done, it is needed to connect the positive side of the P28 R, S, and possibly T buses using jumpers applied to the barrier terminal strip. It is also possible to use three supplies tied together into a single supply bus if desired.

18.7.2.4 PPDA Configuration for JPDC Feedback

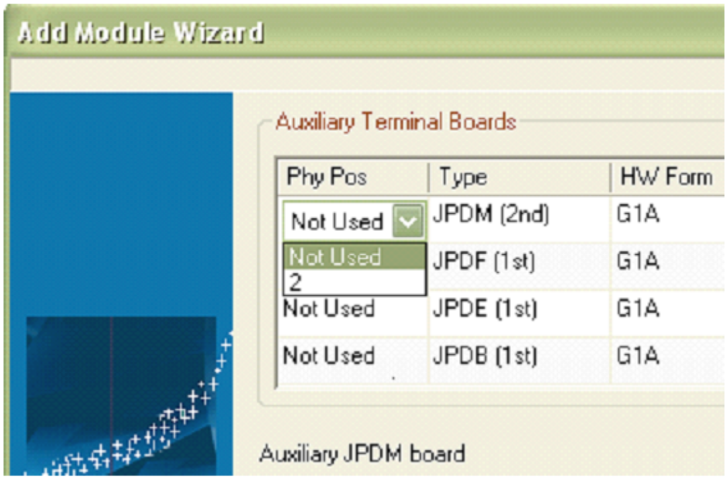
If one or two of the 28 V circuits are not powered, the undervoltage detection for that circuit can be disabled by changing the value of *PS28vEnable*. This also removes the alarm driven by the power supply dry contact monitor associated with that circuit.

18.7.3 Installation

The JPDC module is typically mounted vertically with the 100 to 250 V ac input connector (JAC) at the bottom. It is attached with four screws using the mounting holes located at the top and bottom of the module base. Location within the control cabinet is not critical, however, distribution boards are usually mounted low in the cabinet to facilitate grounding. Refer to the section, Grounding.

The optional PPDA I/O pack is plugged into connector JA1. It is secured to the JPDC base using an angle bracket, held in place with nuts threaded onto studs, that are permanently attached to the base for that purpose.

The JPDM power distribution board consumes two groups of feedback signals with the PPDA I/O pack, so when used, the next available position will be two groups higher.



Phy Pos	Type	HW Form
Not Used	JPDM (2nd)	G1A
	JPDF (1st)	G1A
Not Used	JPDE (1st)	G1A
Not Used	JPDB (1st)	G1A

Diagnostic feedback inputs from other distribution boards are routed to JPDC through a 50-pin ribbon cable attached to connector P2.

Input power connections include:

- Either one or two 125 V dc battery input connections through connectors JD1 and JD2
- 125 V dc DACA module connection made using connector JZ2
- Ac input in the range of 100 to 250 V ac input applied to connector JAC

Up to three separate 28 V dc sources can be made to connectors JR, JS, and JT respectively. The positive sides of these three inputs are isolated from each other and designated as 28PR, 28PS, and 28PT power buses. If only one 28 V dc input is used, the three power buses can be linked together if desired. Refer to the section, Operation.

Attention

To replace a JPDC, replace the entire module. Refer to the section, Replacement. Do not remove the board from its mounting plate.

18.7.3.1 Grounding

Mark VIe and Mark VIeS control systems divides ground into a protective earth (PE) and a functional earth (FE). The PE ground must be connected to an appropriate earth connection in accordance with all local standards. The minimum grounding must be capable of carrying 60 A for 60 seconds with no more than a 10 V drop. The FE ground system must be bonded to the PE ground system at one point.

The FE circuitry on the JPDC board is grounded through metal mounting supports fastened to the underlying sheet metal of the module. The FE ground is used as a local reference point when creating the feedback signals appearing on P2. Typically, the JPDC module is mounted to a back base grounded to FE, completing the path to ground.

The metal switch bodies on the JPDC are tied to PE circuitry on the board. Separate ground wires from the JPDC module, screw connections E5 and or E6 must be connected to the enclosure PE bus.

When input line filters are inserted in line with the JPDC, the filters should be located either on a PE grounded base or near the enclosure PE bus. When PE ground wires are run from the filters to the PE bus, minimum length of the ground wire is important to keep impedance low at radio frequencies, allowing the input line filters to function properly.

18.7.3.2 Physical Arrangement

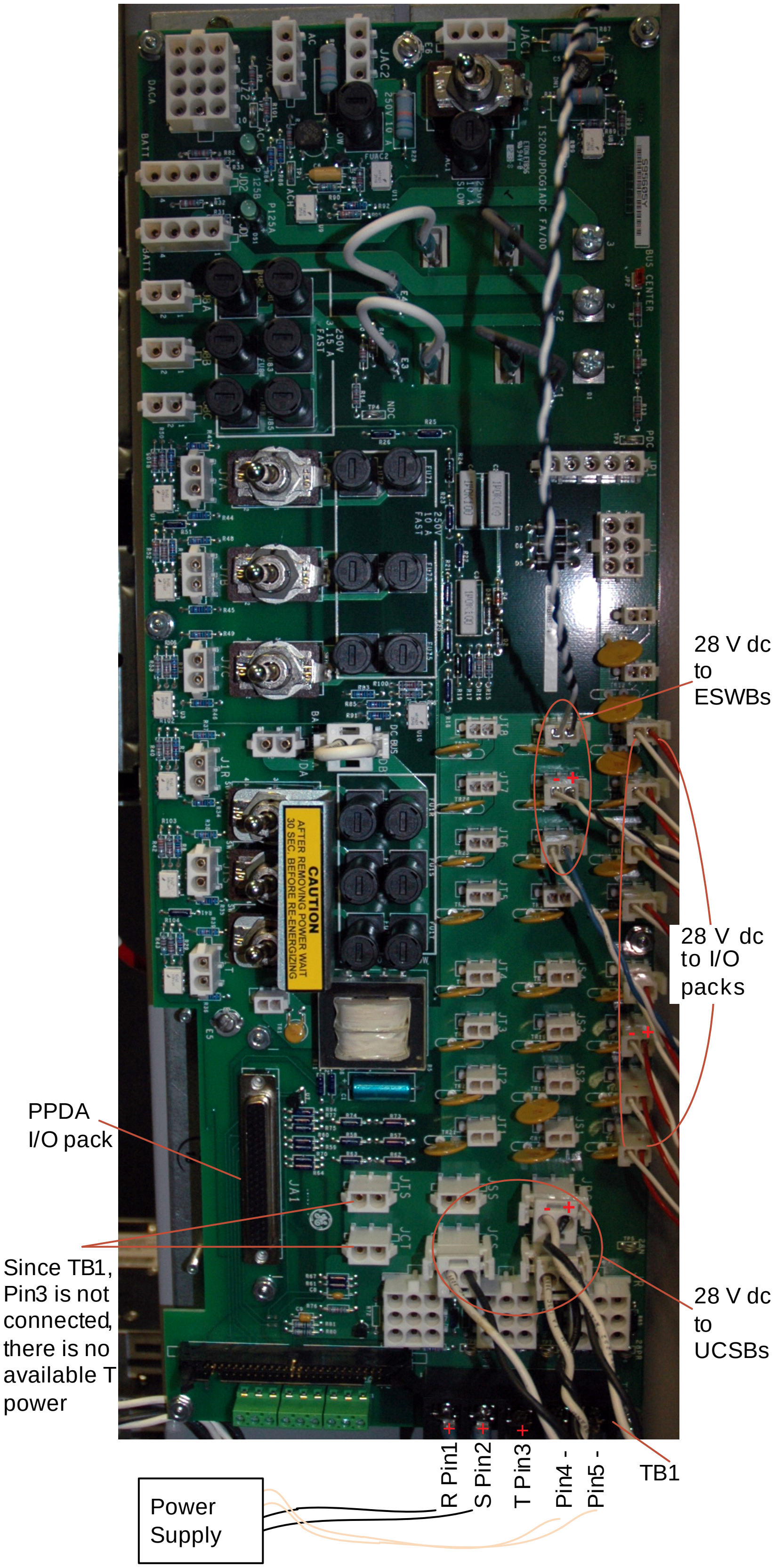
Warning

When using JPDC with JPDF, and if common 125 V dc power supply is being distributed through these boards, make sure that the ground centering jumper(JP1) is only set on one of the boards and not on both.

The IS2020JPDC module consists of a 171.5 x 482.6 mm (6.75 x 19.0 in) IS200JPDC board, a diode assembly, and two resistors mounted on a steel base.

Voltage levels on the JPDC board increase from top to bottom with 28 V dc circuits on the top and left side, 125 V dc in the center and right side, and 115/230 V ac on the bottom.

JPDC Installation Example



PPDA I/O pack

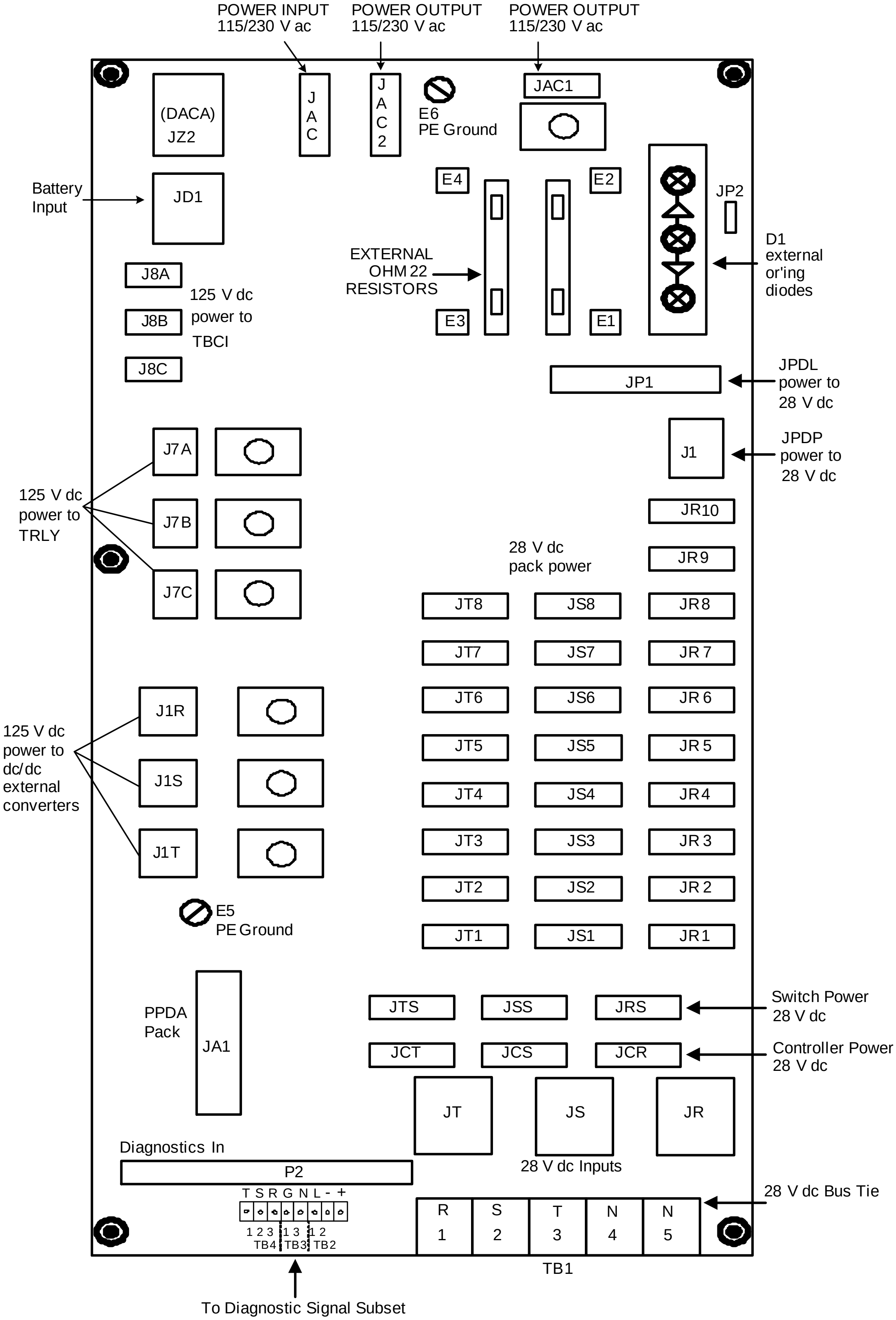
Since TB1, Pin3 is not connected, there is no available T power

28 V dc to ESWBs

28 V dc to I/O packs

28 V dc to UCSBs

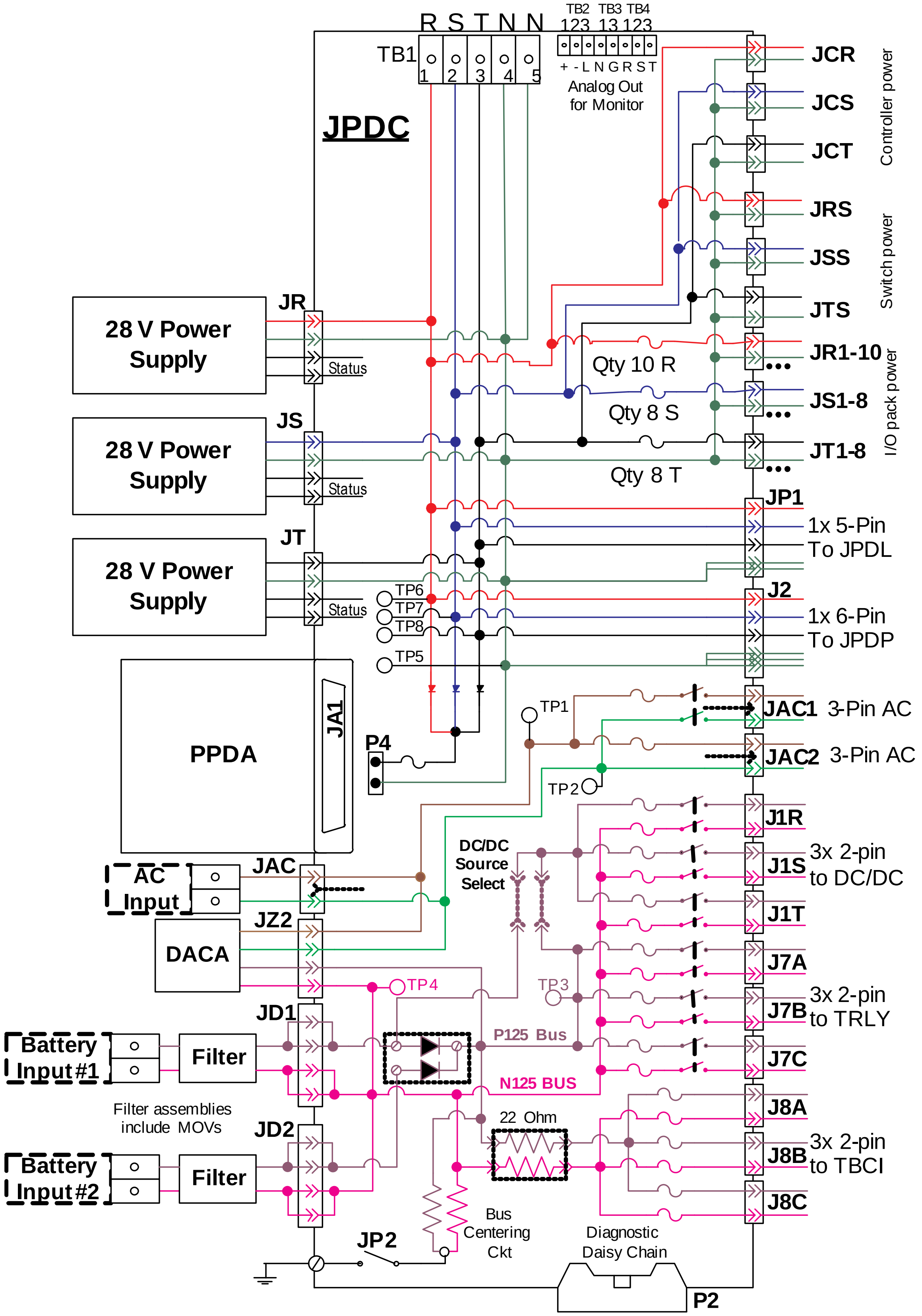
TB1



JPDC Connector Locations

18.7.4 Operation

JPDC provides 125 V dc, 28 V dc, and 100 to 250 V ac power distribution. The following electrical one-line diagram displays the flow of current.



18.7.4.1 AC Power Distribution

An input of 100 to 250 V ac is supplied to JPDC through connector JAC. The maximum allowable current is 12.5 amps rms. AC input is passed through an isolation transformer for sensing.

Two ac outputs are provided. Both are protected by a 10 A time-delay fuse on the high side only (Pin 1 of each connector). The output at JAC1 is controlled by toggle switch SWAC1. The JAC2 output is not switched.

18.7.4.2 125 V DC Power Distribution

JPDC can accept two battery inputs through connectors JD1 and JD2. Provision is also made for a third 125 V dc input from an ac/dc converter such as DS2020DACA through connector JZ2. Each input is typically routed through an external filter. The input voltage range is 90 – 140 V dc.

The two battery inputs are OR'ed together by diode module D1 and are OR'ed with 125 V dc from DACA by a diode on the DACA module. The OR'ed 125 V dc inputs combine on JPDC to form a 125 V dc bus labeled PDC. The return paths of the 125 V dc inputs are connected together and labeled NDC. Total 125 V dc current flow should not exceed 20 A.

All three 125 V dc inputs are floating with respect to ground. When jumper JP2 is installed, each side of the 125 V dc bus is connected to FE ground through approximately 84 k ohms of resistance to provide a means of ground fault detection.

Nine 125 V dc outputs are provided:

- Three outputs J1R, J1S, and J1T provide power to the inputs of three external 125 V dc input / 28 V dc output power supplies which supply JPDC with 28 V dc power. These outputs are fuse-protected and controlled by toggle switches SW1R, SW1S, and SW1T.

Caution

When SW1R, SW1S, and SW1T are switched OFF, wait at least 30 seconds before turning them back ON. This prevents damage to the input circuits of the 28 V dc power supplies.

- Outputs J1R, J1S, and J1T can be powered from either the PDC bus or from Battery A only. Refer to the section, *Configuration*.
- Three outputs J7A, J7B, and J7C are fuse-protected and controlled by toggle switches. They provide output power to the Relay Output (TRLY) terminal board and similar boards.
- Three outputs J8A, J8B, and J8C are only fuse-protected. A 22 W resistor is inserted in series with each side to limit output power. These outputs supply power to boards such as the Contact Input (TBCI) terminal board, which require a source with limited short circuit capability to meet agency requirements.

18.7.4.3 28 V DC Power Distribution

JPDC provides for TMR or Simplex 28 V dc power distribution. Three separate 28 V input connectors; JR, JS, and JT are provided. On each connector, two pins are connected in parallel to increase current-carrying capacity.

Eight output connectors do not have fuse protection: J1, JP1, JCR, JCS, JCT, JRS, JSS, and JTS. Output current should not exceed 12.5 A.

Twenty-six outputs have 1.6 A at 20 °C (derated to 0.86 A at 70 °C) polyfuse protection. In TMR configuration, ten of these, JR1 through JR10, provide 28 PR power, eight provide 28 PS power, and eight provide 28 PT power.

P4 output has 0.5 A at 20 °C (derated to 0.28 A at 70 °C) polyfuse protection and provides power to the PPDA I/O pack. In response to overcurrent, the polyfuse latches off. Cycle power to the polyfuse to reset it.

18.7.5 JPDC Specifications

Item	JPDC Specification	Rating
28 V dc Inputs	Three 9-pin Mate-N-Lok connectors for 28 V dc Power Supply inputs: (JR, JS, JT)	19 A max each
	One 50-pin ribbon cable with diagnostic data from upstream boards (P2)	15 V max
	One 5-screw terminal block for daisy chaining power distribution boards	35 A max per screw
28 V dc Outputs	One 6-pin Mate-N-Lok connector for a JPDP board (J1)	13 A max per pin
	One 5-pin Mate-N-Lok connector for a JPDL board (JP1)	13 A max per pin
	Three 2-pin Mate-N-Lok connectors for CPCI control rack power (JCR, JCS, JCT)	13 A max per pin
	Three 2-pin Mate-N-Lok connectors for LAN switch power (JRS, JSS, JTS)	13 A max per pin
	Twenty six 2-pin mini-Mate-N-Lok connections fused, for auxiliary devices (JR1-JR10), (JS1-JS-8), (JT1-JT8)	1.6 A at 20 °C, 0.85 A at 70 °C polyfuse
	One 5-screw terminal block for daisy chaining power distribution boards (TP1)	35 A max per screw
	One 2-pin connection for 28 V dc power to the PPDA I/O pack (P4)	0.5 A at 20 °C, 0.28 A at 70 °C polyfuse
	One 62-pin D-shell connection for PPDA I/O pack (JA1)	15 V max
115/230 V ac Input	One 3-pin Mate-N-Lok connector (JAC)	13 A max
	Board Rating	100 to 250 V ac 50/60 Hz 30 A circuit breaker protection
115/230 V ac Output	Two 3-pin Mate-N-Lok connectors (JAC1, JAC2)	10 A max each
	Fuses for connectors JAC1-JAC2 and FUAC1-FUAC2: FU1-FU8	10 A, 250 V, Littelfuse® 218010 is typical
125 V dc battery Inputs	Two 4-pin Mate-N-Lok connectors (JD1, JD2)	20 A max total current
125 V dc DACA Input	One 12-pin Mate-N-Lok connector (JZ2)	10 A max
	Board Rating	125 V dc nominal, 140 V dc maximum, 30 A circuit breaker protection
	Impedance to ground	JP2 jumper in place >75 kΩ JP2 jumper removed > 1500 kΩ
	Fuses for connectors J1R: FU1R- FU2R, J1S: FU1S-FU2S, J1T: FU1T-FU2T	10 A 250 V, Littelfuse 218010 is typical
	Fuses for connectors J7A: FU71-FU72, J7B: FU73-FU74, J7C: FU75-FU76	10 A 250 V, Littelfuse 217010 is typical
	Fuses for connectors J8A: FU81-FU82, J8B: FU83-FU84, J8C: FU85-FU86	3.15 A 250 V, Littelfuse 2173.15 is typical
	Temperature Range	-40 to 70 °C (-40 to 158 °F)
	Board Size	17.2 cm Wide x 48.26 cm High (6.75 in x 19.0 in)
	Module Size	17.78 cm Wide x 51.81 cm High x 7.62 cm Deep (7.0 in x 20.4 in x 3 in)
	Mounting	Back-panel mounting, adjacent to other power distribution boards
Ambient Rating for Enclosure Design†	-40 to 70 °C (-40 to 158 °F) *† Refer to GEH-6721_Vol_I, the chapter Technical Regulations, Standards, and Environments.*	

18.7.6 Diagnostics

JPDC provides for the connection of a PPDA I/O pack for power distribution feedback to the IONet. The PPDA I/O pack mounts on the JPDC. JPDC uses two feedback signal groups on the PPDA I/O pack connector comprised of the diagnostic signals listed in the following table.

Signal	Description
FDBK_A1	Attenuated voltage difference from PDC bus to ground (volts to earth magnitude) V_A1/VPDC = 0.033316 V/V
FDBK_A2	Attenuated voltage difference from NDC bus to ground (volts to earth magnitude) V_A1/VPDC = -0.033316 V/V
FDBK_A3	Multiplexed feedbacks from J1S-T and J7A-C (requires PPDA I/O pack) (125 V dc outputs)
FDBK_A4	
FDBK_A5	Attenuated AC input voltage (AC1 feedback magnitude) V_A5 / VAC is approximately 0.01885 V/V
FDBK_B1	Multiplexed feedbacks from Battery 1 (BATT1) input, Battery 2 (BATT2) input, JAC1 output, and JAC2 output (requires PPDA I/O pack)
FDBK_B2	Attenuated 28 V dc R inputs (feedback magnitude) Attenuation ratio = Vfeedback/Vin = 0.143 V/V
FDBK_B3	Attenuated 28 V dc S inputs (feedback magnitude). Attenuation ratio = Vfeedback/Vin = 0.143 V/V
FDBK_B4	Attenuated 28 V dc T inputs (feedback magnitude) Attenuation ratio = Vfeedback/Vin = 0.143 V/V
FDBK_B5	Multiplexed feedbacks from external 28 V dc power supplies R, S, T, P, S contacts (requires PPDA I/O pack)

Note Fuses 71 to 76 and fuses R,S,T are on the 125 V dc input. Fuse AC1 and AC2 are on the ac input. A fuse failure diagnostic will not be generated if *InputDiagEnab* on the respective input is set to Disable or the input is below the lower tolerance limit set on them. Lower tolerance limit for 125 V dc is pre fixed at 42 V. The lower tolerance limit for ac is the configuration parameter.

- There are no feedback signals provided for the three fused TBCI terminal board outputs (J8A, J8B, and J8C) since each TBCI terminal board has its own voltage monitoring circuit.
- A P1 connector is not provided to feed JPDC diagnostic signals to another location.
- Feedbacks also include an electronic ID identifying the board type, revision, and serial number.
- A 50-pin ribbon cable connector (P2) is used to daisy chain the diagnostic signals from other distribution boards to JPDC. Up to four additional boards may be cabled into JPDC for PPDA I/O pack reception. In a JPDC-based PDM system, the PPDA I/O pack must be mounted on JPDC.
- Three terminal boards (TB2, TB3, and TB4) are mounted end to end at the top of JPDC. These provide access to the non-multiplexed signals and the analog diagnostic feedback signals without the need for a PPDA I/O pack.

Terminal Board	Pin #	Attenuation Ratio
TB1		
PDC_FDBK_A1	1	0.033316 V/V
NDC_FDBK_A2	2	-0.033316 V/V
AC1_FDBK_A5	3	0.01885 V/V
TB2		
FDBK_AG	1	Ground Reference for AC feedback

Terminal Board	Pin #	Attenuation Ratio
NCTB2	2	No connect
FDBK_BG	3	Ground reference for DC feedback
TB3		
28PR_FDBK_B2	1	0.143 V/V
28PS_FDBK_B3	2	0.143 V/V
28PT_FDBK_B4	3	0.143 V/V

18.7.6.1 Diagnostic Circuits

Test rings TP1 and TP2 are connected to ACH and ACL respectively of the ac input line to allow monitoring ac bus voltage. Each has a 30.1 K buffer resistor in series. Test rings TP3 and TP4 are connected to positive and negative sides respectively of the 125 V dc bus. Each has a 30.1 K buffer resistor. Test ring TP5 is connected to the negative or return side of all three 28 V dc inputs. (No buffer resistor is provided). Test rings TP6, TP7, and TP8 are connected to 28PR, 28PS, and 28PT respectively. These are the positive lines of the three 28 V dc TMR power inputs. (No buffer resistors are provided).

18.7.7 Configuration

18.7.7.1 28 V DC TMR Configuration

- Separate power inputs are received through connectors JR, JS, and JT.
- The positive sides of the three inputs are connected to separate power buses, designated as 28PR, 28PS, and 28PT respectively. The return sides of the three inputs are connected together and designated as 28N.
- Output power is distributed from the three buses through separate R, S, and T output connectors.

18.7.7.2 28 V DC Simplex Configuration

- One, two, or three 28 V dc power inputs can be received through connectors JR, JS, and JT.
- The three power buses can be connected into a single bus by inserting jumpers between terminals 1, 2, and 3 of terminal board TB1.
- All output connectors are fed from the single 28 V dc bus.

18.7.7.3 125 V DC Outputs to External 125 V DC or 28 V DC Power Supplies

Caution

Never connect jumper JDA and JDB at the same time.

- Two options are provided for the selection of power outputs through connectors J1R, J1S, and J1T.
- For normal operation, a shorting plug is inserted in connector JDB. This configuration selects 125 V dc power from the entire P125 bus, which is fed by both battery inputs and the DACA input.
- A second mode of operation allows the user to replace the DACA supply with an ac/dc converter of lower power rating. In such a case the shorting plug should be moved to connector JDA. This configuration selects power for connectors J1R, J1S, and J1T from Battery A only and allows the lower-rated ac/dc converter to supply power only to the other 125 V dc outputs.

18.8 JPDD DC Power Distribution

The JPDD dc power distribution board provides dc power distribution, power isolation, and branch circuit protection for control or I/O functions requiring 125 V dc, 48 V dc, or 24 V dc power. Typical applications include dc relay and solenoid control power, and contact wetting. Each output includes a fuse, a switch, and a lamp to indicate the presence of output voltage. JPDD is not intended for power distribution to the I/O packs.

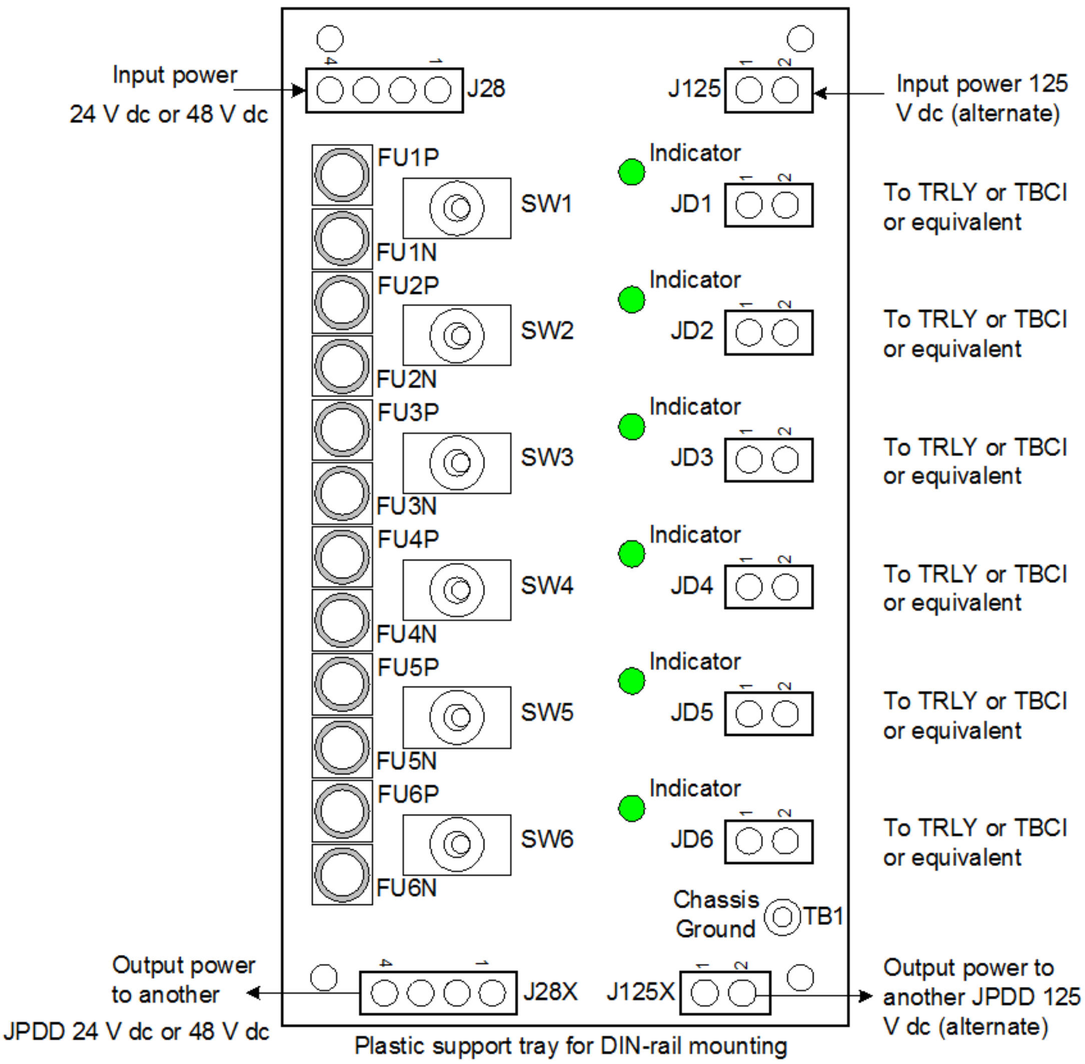
Board version JPDDG1 provides fuses that are coordinated with the rating of the system wiring and connectors. JPDDG2, G3, and G4 have fuse ratings coordinated for specific applications. Two different fuse sizes are provided to accommodate local fuse preferences.

JPDD Board Versions

Terminal Board	Fuses
JPDDG1A	Each circuit provided with 31.75 x 6.35 mm (1.25 x 0.25 in) 15 A 250 V fuse
JPDDG2A	Empty fuse holders with black caps accepting 5 x 20 mm (0.20 x 0.79 in) fuses
JPDDG3A	Empty fuse holders with grey caps accepting 31.75 x 6.35 mm (1.25 x 0.25 in) fuses
JPDDG4A	Each circuit provided with 31.75 x 6.35 mm (1.25 x 0.25 in) 0.5 A fuses for wire protection

18.8.1 Installation

JPDD is held in a plastic holder, which mounts on a vertical DIN-rail. When installing the JPDD, it is important to provide a ground lead from TB1 to the system ground. This creates a ground path for the metal switch bodies.



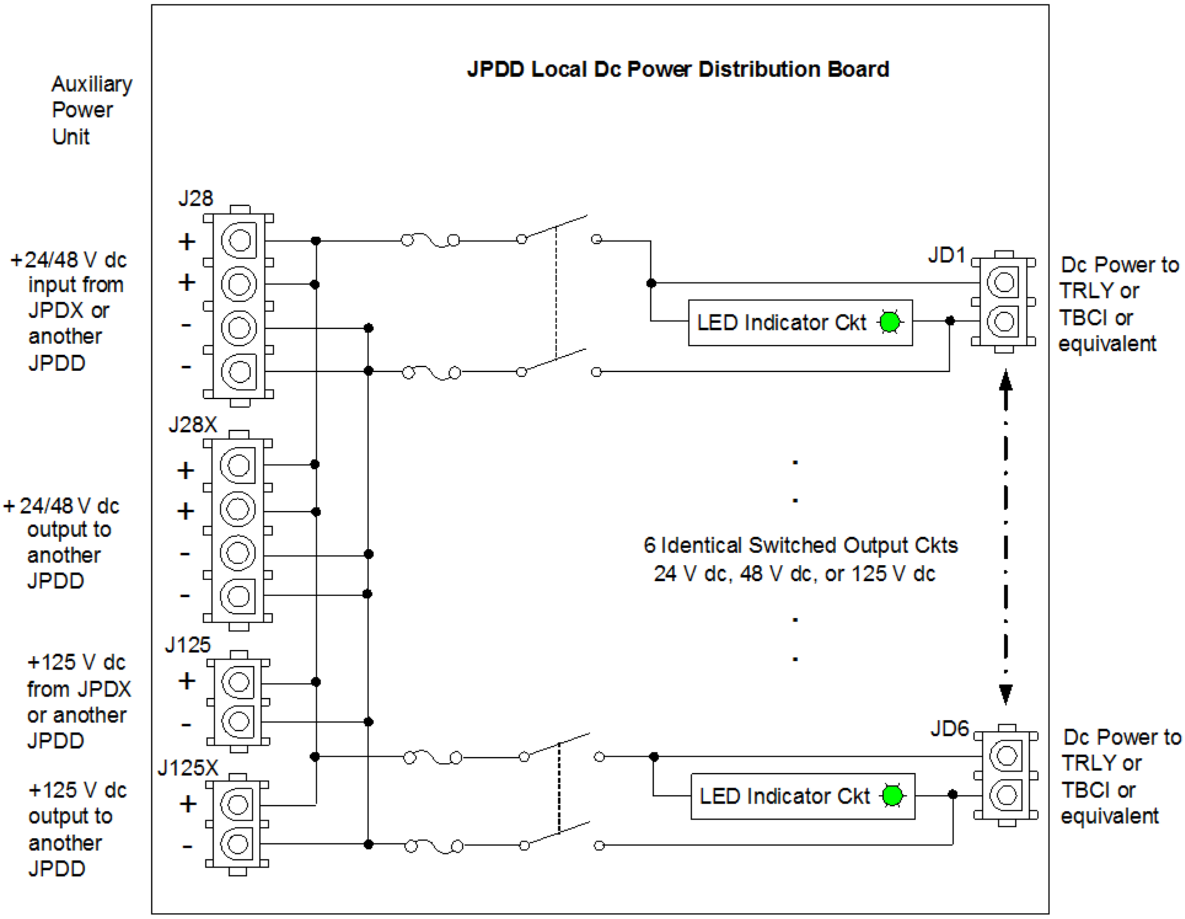
JPDD Dc Power Distribution Board

JPDD Cabling

Power input can be 24 V dc, 48 V dc, or 125 V dc, but only one voltage level at any given time. Do not mix voltages. For cable destinations, refer to the circuit diagram. TB1 should be connected to system ground.

18.8.2 Operation

The following figure explains how the 125 V dc, 48 V dc, or 24 V dc power is distributed in JPDD, and how it reaches the TRLY and TBCI boards.


JPDD Local Dc Power Distribution Board
Auxiliary Power Unit
J28
+24/48 V dc input from JPDX or another JPDD
J28X
+ 24/48 V dc output to another JPDD
J125
+125 V dc from JPDX or another JPDD
J125X
+125 V dc output to another JPDD
+
+
-
-
JD1
Dc Power to TRLY or TBCI or equivalent
LED Indicator Ckt
6 Identical Switched Output Ckts
24 V dc, 48 V dc, or 125 V dc
JD6
Dc Power to TRLY or TBCI or equivalent
LED Indicator Ckt

JPDD Simplified Circuit Diagram

18.8.2.1 Inputs

Multiple JPDD boards can receive power from a single Main Power Distribution Module branch circuit. Power input can be either 125 V dc, 48 V dc, or 24 V dc nominal.

Caution

Both inputs share a common electrical path. Only a single voltage (24, 48, or 125) can be applied at one time to both inputs.

Two 2-Pin Mate-N-Lok connectors are provided for 125 V dc power. One connector receives input power and the other can be used to distribute 125 V dc power to another JPDD board in daisy chain fashion.

Two 4-pin Mate-N-Lok connectors are provided for 24/48 V dc power. These perform functions similar to those of the 2-pin connectors above. The 4-pin connector permits parallel connection of two pin-pairs for increased current capacity. It is expected that neither side of the dc power input is grounded.

18.8.2.2 Outputs

Six identical output circuits are provided. Each output circuit includes two fuses, a switch with a pair of isolation contacts in each side of the output, and a green lamp to indicate the presence of voltage across the output terminals. The provision of a fuse and switch contact in each side of the dc path allows use of this board with floating power sources.

18.8.3 Specifications

Item	JPDD Specification	
Inputs	One 2-pin connection for input power from JPDx or another JPDD One 4-pin connection for input power from JPDx or another JPDD	125 V dc, 15 A 24 or 48 V dc, 30 A
Outputs	Six 2-pin connections for power to TRLY or TBCI One 2-pin connection for output power to another JPDD One 4-pin connection for output power to another JPDD	24 V dc or 125 V dc, fused 125 V dc 24 or 48 V dc
Fuses	Refer to the table, *JPDD Board Versions*.	
Ambient Rating for Enclosure Design†	-40 to 70ºC (-40 to 158 ºF)	
Board Dimensions	23.495 cm high x 10.795 cm wide (9.25 in x 4.25 in)	
Mounting	DIN-rail, card carrier mounting Base mounted steel bracket, 4 holes	

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

18.8.4 Configuration

There are no jumpers on JPDD. Check the position of the six output load switches.

It is possible to use other fuse ratings with this board to provide specific branch circuit ratings. A typical series of fuses that work with this board are the Bussmann ABC series of fuses with ratings from ¼ A through 15 A. Fuses above 15 A shall not be used with this board. If alternate fuse ratings are used, configuration of the board requires the insertion of the proper fuse in each branch circuit.

18.9 JPDE DC Battery Power Distribution

18.9.1 Functional Description

The dc Battery Power Distribution (JPDE) board receives dc power from a battery or power supplies and distributes it to terminal boards and other system loads. JPDE supports a floating dc bus that is centered on earth using resistors and provides voltage feedback through PPDA to detect system ground faults. It provides inputs for two power supplies. JPDE is able to operate at either 24 V dc or 48 V dc. JPDE integrates into the PDM system feedback offered through the PPDA I/O pack.

This board is limited by the current that can be passed through it using conventional board construction. JPDE does not supply power to bulk 500 W - 24 V input/28 V output power supplies providing I/O pack control power.

JPDE is the PDM element that receives dc power from a battery or power supplies and distributes it to I/O such as relay and contact input boards. JPDE supports a floating battery bus that is centered on earth using resistors, and provides voltage sensing to detect system ground faults. It provides inputs for two power supplies including their associated status contact feedback. The design is compatible with applications using either 24 V or 48 V dc.

The current that can be passed through the board (using conventional board construction techniques) limits the amperage capabilities of this board. For this reason, the JPDE is not intended to supply power to bulk 500 W 24 V input / 28 V output power supplies providing I/O pack control power. Each one of these supplies will consume approximately 25 A at full load. A set of three for R, S, and T would then use 75 A, exceeding the conventional capability of circuit boards. While special board construction is possible to address the high current, the resulting high product cost would exceed the cost of using more simple and readily available commercial components.

When power distribution is needed for I/O, it is more functional to have a board that provides centering resistors for a floating bus, voltage feedback for magnitude and ground detection, status feedback from dc power supplies, and fused output monitoring. The JPDE addresses these needs.

18.9.2 JPDE I/O Characteristics

- For JPDE battery applications, four battery input screw terminals located adjacent to the board on a barrier terminal strip are used. Nominal rating of the dc input path is 30 A, and the voltage is not expected to exceed 60 V. Protection of the branch circuit (supplying power to this input) is expected to be no greater than a 30 A breaker. This is the primary power input.
- JD1 is a six pin Mate-N-Lok connector that accepts the power input from external dc power sources such as a battery when a wire harness is to be used.Three connector pins are used for each side of the dc input to provide adequate current rating.
- Two power supply inputs are provided on JPS1 and JPS2. The connector uses pins 8 and 9 for positive 24 V or 48 V. Pins 1-3 are used for 24 return, providing 24 A steady state capacity. These connectors include low level signals capable of detecting status switches on each supply and generating a feedback signal to PPDA. Pin 4 provides positive 10 V wetting to the switch, and the return is on pin 5.
- There are three fused, switched, four-pin Mate-N-Lok output connectors: JS1, JS2, and JS3. Positive power is on pins 1 and 2, negative power is on pins 3 and 4. This matches the pin use on JPDD J28 and J28X. Fuse rating is 7 A.
- There are three fused four pin Mate-N-Lok output connectors JFA, JFB, and JFC. Positive power is on pins 1 and 2, negative power is on pins 3 and 4. This matches the pin use on JPDD J28 and J28X. Fuse rating is 15 A.
- Ground reference jumper JP1. The dc bus is normally operated without a hard ground connection. It is desirable to center the dc on earth as part of the ground fault detection scheme. In normal 24 V operation, the dc positive terminal would measure ½ * 24 V above ground, while the negative terminal would measure the same magnitude below ground potential. The resistors to center the bus on earth may either be supplied external to the JPDE, or on-board resistors may be used by closing jumper JP1.
- Diagnostic daisy chain 50 pin ribbon cable connectors P1 and P2 on top and bottom of the board for pass-through of the diagnostic signals are discussed in the next section.

18.9.2.1 Diagnostic Features

The signals that will be routed into PPDA through P1 for diagnostics include:

- An electronic ID is used to identify the board type, revision, and serial number.
- There are two analog dc voltage feedbacks. One is used for the positive bus with respect to earth, and one is used for the negative bus with respect to earth (2 analogs). PPDA uses these signals to create two signals with *DC_24VFdbkMag* indicating total magnitude (difference between positive and negative) and *DC_24VGnd_FdbkMag* indicating voltage offset for a system ground. Voltage feedback accuracy is specified at ±1% of 48 V and exceeds ±0.25% of 48 V or ±0.12 V.
- Each fused output drives an optocoupler circuit. The optocouplers are combined into two multiplexed fuse indications (multiplexed on two analog signals). They yield six Boolean values after PPDA decodes the signal.
- Test points HW1 and HW2 provide impedance limited connections to the positive and negative dc power for voltage measurements.
- Two dc power converter output status dry contact indications (multiplexed on one analog) yield two Boolean values after PPDA decodes the signal. These may be used to identify that one of two redundant power supplies has failed and requires attention.

Other core PDM board feedback may pass through JPDE using the P2 connector.

18.9.2.2 JPDE Grounding

Mark VIe control systems separate ground into a functional earth (FE) and a protective earth (PE). The protective earth is intended for power distribution functions such as JPDE, while functional earth is used for *quiet* uses such as the control electronics and field signals.

Grounding of the JPDE takes place through metal mounting standoffs. The ground is applied to the metal switch bodies on JPDE. In addition, the ground is used as a local reference when creating the magnitude feedback signals appearing on P2.

18.9.2.3 JPDE Physical Arrangement

JPDE is designed to accept power input from the right hand side and deliver power output from the left hand side. The P1 and P2 ribbon cable headers on all of the JPDx boards are designed so the JPDS or JPDM holding the PPDA I/O pack is best located at the top of the arrangement. This allows ribbon cables to flow from one to the next, exiting the top and entering the bottom of the next until the PPDA host is reached.

18.9.2.4 PPDA Configuration for JPDE Feedback

An alarm is generated if the value of *DC_24V FdbkMag* drops below the voltage specified by *DC_24v_Trig_Volt*. The value of *DC_24 V_Trig_Volt* should be coordinated with the application voltage and expectations for voltage regulation. An alarm is generated if the value of *DC_24VGnd_FdbkMag* exceeds the voltage specified by *Gnd_Mag_Trig_Volt*. This sets up the sensitivity of the ground fault detection. To disable fuse monitoring in the three switched output circuits, change the *FuseDiag* from the default **Enable** to **Disable**. These setting changes are needed for battery-powered applications.

18.9.3 Installation

The IS200JPDE board is compatible with the feedback signal P1/P2 connectors on JPDB, JPDF, JPDS, JPDM, JPDC, and JPDG leading to a PPDA I/O pack. The JPDE is base-mounted vertically on a metal bracket in a cabinet used by the PDM. Refer to the wiring diagrams for power input and output routing. There is a 50-pin diagnostic connector mounted on the top and bottom of the board.

18.9.3.1 Grounding

The IS200JPDE board is grounded through the sheet metal bracket to the underlying back base. In most cases, this is the system FE.

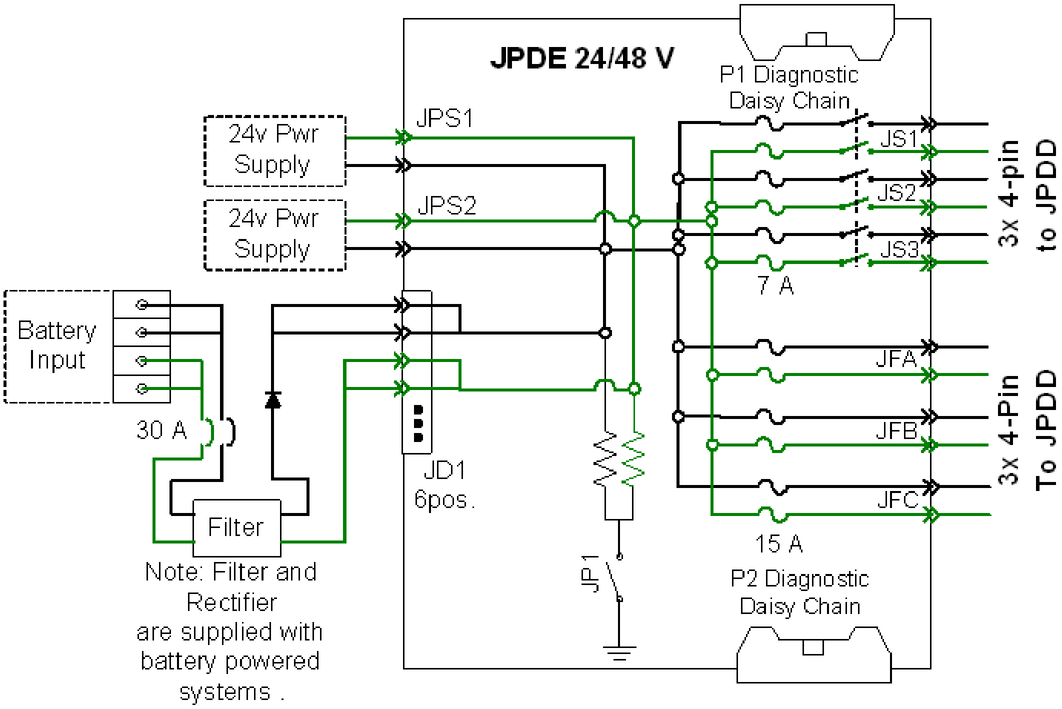
18.9.3.2 Physical Arrangement

The location of JPDE is not critical in a panel. Connector P1 transmits feedback signals to a board hosting a PPDA I/O pack. Connector P2 receives feedback from other power distribution boards and passes the signals out of P1 to the PPDA. If a cable connection from JPDE to a board containing PPDA is planned, consideration should be given to the feedback cable routing between JPDE P1 and the P2 connector on the board receiving the feedback cable.

18.9.3.3 Application Notes

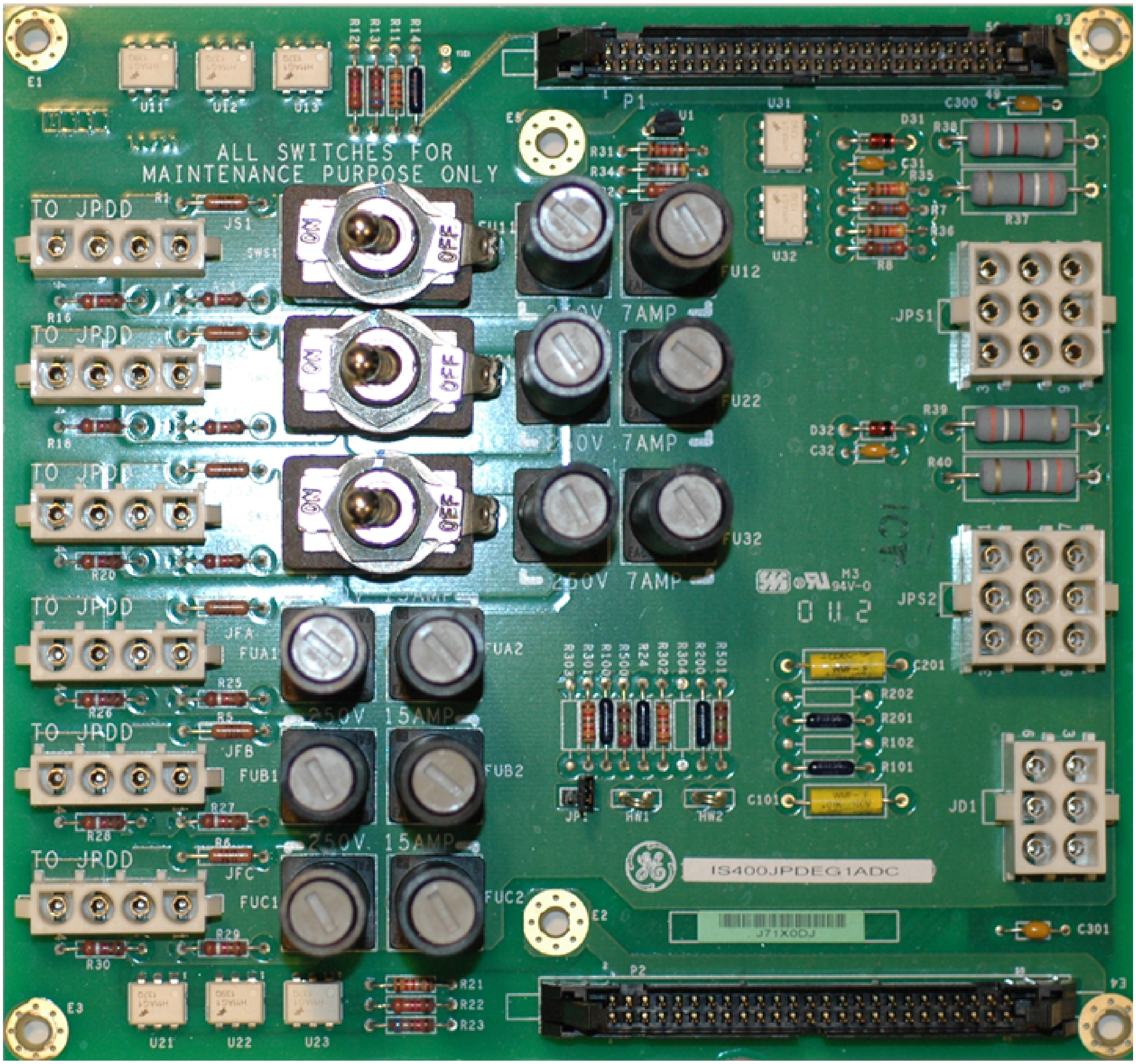
JPDE can be used with one or two power supplies to create a dc power system for terminal boards and other system loads. When this is done, float the dc power system and use the grounding resistors on JPDE to center the bus on earth. This permits detection of ground faults through the PPDA bus voltage feedback. Jumper JP1 is required to be in place, connecting the centering resistors to earth. When JPDE is used to distribute battery power, it is supplied with a dc circuit breaker and a 30 A input filter.

18.9.4 Operation



Note: Filter and Rectifier are supplied with battery powered systems .

JPDE Simplified Electrical Diagram


ALL SWITCHES FOR MAINTENANCE PURPOSE ONLY
TO JPDD
ON
OFF
250V 7AMP
250V 15AMP
FU11
FU12
FU22
FU32
FUA1
FUA2
FUB1
FUB2
FUC1
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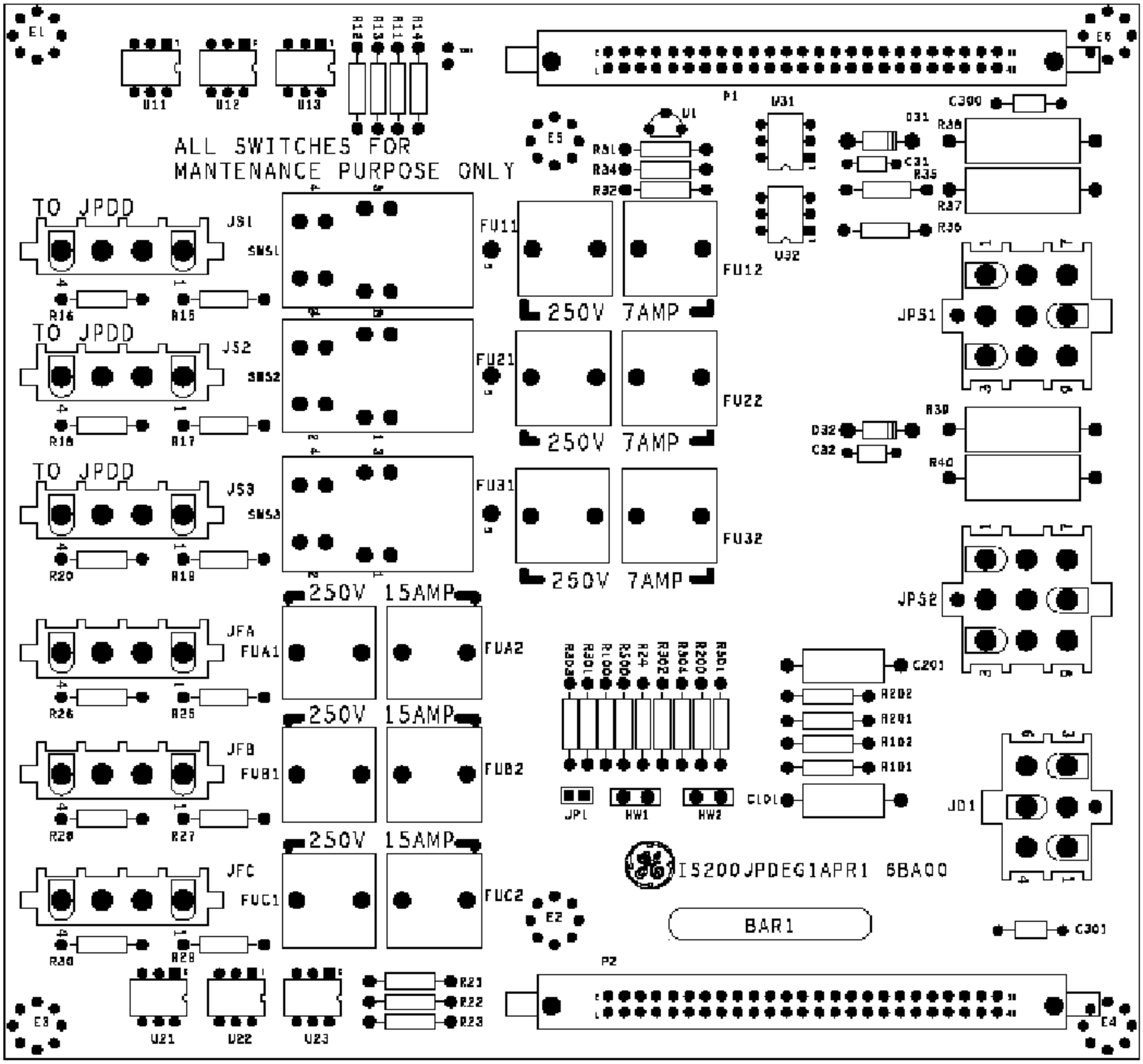
JD1
P1
P2
IS400JPDEG1ADC

JPDE Photo



JPDE Mechanical Layout

18.9.4.1 JPDE Connections

- JD1 is a 6-pin Mate-N-Lok connector that accepts power input from a battery. Three connector pins each are used for positive and negative connections to provide adequate current rating.
- JFA, JFB, and JFC are fused four-pin Mate-N-Lok output connectors. Positive power is on pins 1 and 2, and negative power is on pins 3 and 4. This matches the pin use on JPDD J28 and J28X. These connectors have a fuse rating of 15 A.
- JP1 is the ground reference jumper. The dc bus is normally operated without a hard ground connection. The dc bus is centered on earth as part of the ground fault detection scheme. Normally, the 24 V operation of the dc positive terminal would measure ½ * 24 V above ground and the negative terminal has the same magnitude below ground potential. Resistors to center the bus on earth are supplied externally to the JPDE, or on-board resistors can be used by closing jumper JP1.
- JPS1 and JPS2 are nine-pin Mate-N-Lok connectors used for power supply input. The connector uses pins 8 and 9 for positive 24/48 V dc and pins 1-3 for 24 V return providing 24 A steady state capacity. Pin 4 provides positive 10 V dc wetting to a supply status feedback switch and pin 5 provides the return.
- JS1, JS2, and JS3 are fused and switched four-pin Mate-N-Lok output connectors. Positive power is on pins 1 and 2, and negative power is on pins 3 and 4. This matches the pin use on JPDD J28 and J28X. The fuse rating for these switched connectors is 7 A.
- Two 50-pin diagnostic ribbon cable connectors, P1 and P2, are supplied on the top and bottom of the board. Connector P1 transmits feedback signals to a board hosting a PPDA I/O pack. Connector P2 receives feedback from other power distribution boards and passes the signals out of P1 to the PPDA.

18.9.5 Specifications

Item	JPDE Specification
Total Board Rating	30 A total dc current from all branch circuits 50 V maximum nominal voltage
Fuse for Connectors JS1-JS3: FU11-12, FU21-22, FU31-32	7 A, 250 V, Bussmann ABC-7 typical
Fuse for Connectors JFA, JFB, JFC: FUA1-2, FUB1-2, FUC1-2	15 A 250 V, Bussmann ABC-15 typical
Board Dimensions	16.51 cm High x 17.8 cm Wide (6.5 in x 7 in)
Mounting	six mounting holes
Ambient Rating for Enclosure Design†	-40 to 70°C (-40 to 158 °F)

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

18.9.6 Diagnostics

Diagnostic signals routed into PPDA through connector P1 include:

- An electron|ic ID identifying the board type, revision number, and serial number
- Two analog battery voltage feedbacks. One is for positive bus and one is for negative bus. Voltage feedback accuracy is ±1%.
- Three switched/fused dc branch circuit status signals
- Two dc power converter output status dry contact status signals
- Three fused branch circuit status signals
- Two test points with series 2.15 kΩ resistors are provided on the 24/48 V dc bus for external test equipment. HW1 is connected to the positive bus and HW2 is connected to the negative bus.

Note Fuse and dry contacts failure diagnostics will not be generated if *InputDiagEnab* on the dc input is set to Disable or the dc input is below 42 V.

18.9.7 Configuration

When jumper JP1 is in place, the JPDE provides 6 kΩ voltage-centering resistors from positive and negative dc to the local earth connection. When JP1 is removed, the connection to earth is opened. Insert JP1 when a floating dc bus needs to be centered on earth.

18.10 JPDF 125 V DC Power Distribution

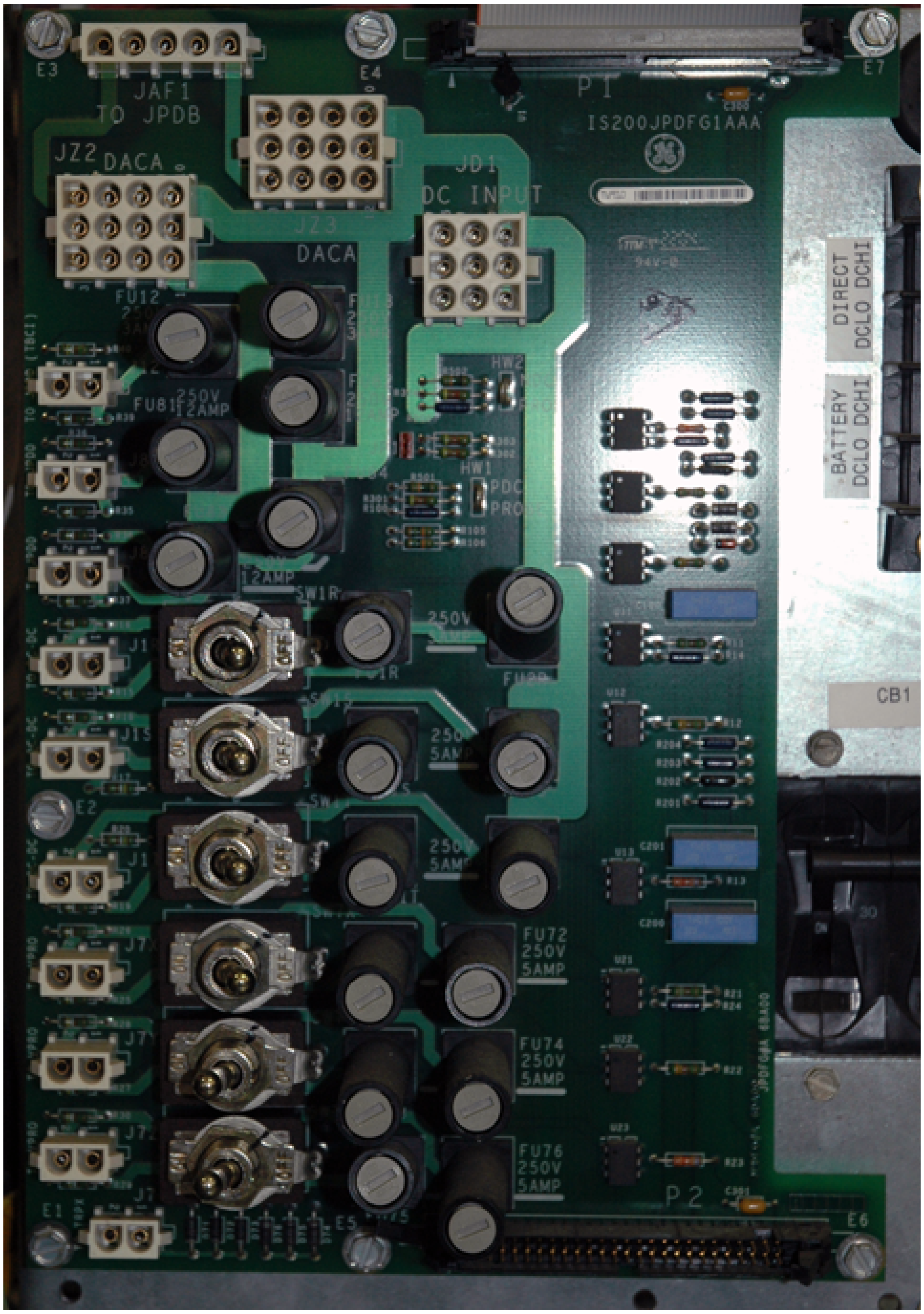
18.10.1 Functional Description

The JPDF 125 V dc power distribution board accepts redundant 125 V dc power inputs and distributes power to other system boards. JPDF works with a floating dc bus that is centered on earth rather than with a grounded system. This permits detection of a system ground fault and carries a non-hazardous live 125 V dc rating.

Input 125 V dc battery power is connected to a terminal board on the IS2020JPDF module. The power is then routed through a 125 V dc 30 A circuit breaker and line filter before being connected to the IS200JPDF board through the J1 connector. Dc voltage is then routed to three fused, non-switched outputs and six fused, switched outputs.

Ac power is routed through the board to the DACA modules where it is converted to dc power. Dc power returns to JPDF where it is combined with the battery power input. JPDF can operate with any combination of one or more inputs active creating a high-reliability source of 125 V dc power for the control system.

The IS2020JPDF module provides full status feedback using a connection to a PPDA I/O pack. Feedback includes bus magnitude, ground fault detection, and detection of excessive ac voltage on the dc bus. Each fused branch circuit is monitored to indicate the presence of output power. Two hardware test rings, with series 100 kΩ resistors, are provided for attaching test equipment. HW1 is labeled PDC Probe and HW2 is labeled NDC Probe.



JPDF Photo

18.10.1.1 Compatibility

The IS2020JPDF is compatible with the feedback signal connectors, P1/P2, on JPDB, JPDE, JPDS, JPDM, JPDC, and JPDG leading to a PPDA I/O pack. Connector JAF1 is compatible with the ac power output on the IS2020JPDB module. Connectors JZ2 and JZ3 are compatible with the connectors on the DS2020DACA module.

18.10.2 JPDF I/O Characteristics

- Two battery input screw terminals are located to the right of the board on a barrier terminal strip. Nominal rating of the dc input path is 20 A, and the voltage is expected to never exceed 145 V. Protection of the branch circuit supplying power to this input is expected to be no greater than a 30 A breaker, supplied by default as part of the module. This is the primary power input.
- Two dc output screw terminals are located on the same barrier terminal strip. This connection point is after the diode-or has taken place between power from the battery and DACA modules. These terminals are typically not used, but are provided for times when two JPDF boards are desired to work in parallel. Another use is when designing redundant 125 V dc distribution for extreme reliability systems. Rating is 20 A.
- JD1 is a nine pin Mate-N-Lok connector that accepts the power input from the components that are mounted under the JPDF board and is best understood by reviewing the electrical one-line diagram. This connector comes populated with a wire harness that is part of the JPDF module assembly and should never need attention from a user.
- JAF1 is a five pin Mate-N-Lok designed to accept ac input from an adjacent JPDB board. The ac is passed to the JZ2 and JZ3 connectors. Rating of the connector supports the full rated capacity of the DACA module.
- Two DACA compliant connectors- DACA is an ac in, dc out module that is already part of the Mark V and Mark VI controls. These connectors, JZ2 and JZ3, are electrically the same as the connectors in the Mark VI PDM module. The ac on the connectors comes from JAF1, and the dc output is wired to the redundant bus.
- Three fused, switched two pin Mate-N-Lok output connectors J1R, J1S, and J1T are provided for powering 125 V dc/28 V dc converters where 28 V dc is the control power for I/O packs. Fuse rating is 10 A. Positive power is on pin 1, negative power is on pin 2.
- There are three fused, switched two pin Mate-N-Lok output connectors J7X, J7Y, and J7Z for powering VPRO modules. While VPRO has been replaced by PPRO in Mark VIe control systems it was felt important to preserve the ability to power VPRO for retrofit opportunities. Positive power is on pin 1, negative power is on pin 2. Fuse rating is 5 A. The VPRO has tight mechanical clearances and the power supplies are designed into the module. There is not enough space to include electrical clearances for a high fault current dc input to VPRO, so the JPDF module provides defined source impedance. Two 1 W resistors mounted under the board define the minimum source impedance that is required by VPRO.
- A special two pin Mate-N-Lok output is provided to supply power to the system trip boards using connector J7. Positive power is on pin 1, negative power is on pin 2. It is formed using a diode-or of the three VPRO power outputs. As such it works any time at least one VPRO branch circuit is still working and is removed if all three VPRO outputs contain blown fuses.
- There are two fused dc two pin Mate-N-Lok outputs on J8A and J8B that typically feed remote JPDD boards to provide individual switched / fused circuits to points of load such as TRLY boards. Positive power is on pin 1, negative power is on pin 2. These outputs are fused for 12 A.
- A final two-pin Mate-N-Lok output J12 is provided to operate TBCI contact input boards. Positive power is on pin 1, negative power is on pin 2. Again the clearances of the board dictate a known source impedance for the 125 V dc input, provided by resistors in the module. Two 22 Ω resistors under the JPDF provide fault current protection for the system TBCI boards. While 3 A fuses are supplied on JPDF, they should never open, even under fault conditions due to the current limit imposed by the resistors. Remote JPDD boards providing individual branch circuit switching, fusing, and indication typically power TBCI.
- Ground Reference Jumper JP1. The dc bus is normally operated without a hard ground connection. It is desirable to center the dc on earth as part of the ground fault detection scheme. In normal operation, the dc positive terminal would measure ½ * 125 V above ground, while the negative terminal would measure the same magnitude below ground potential. The resistors to center the bus on earth may either be supplied external to the JPDF, or on-board resistors may be used by closing jumper JP1
- Diagnostic Daisy Chain 50 pin ribbon cable connectors P1 and P2 on top and bottom of the board for pass-through of the diagnostic signals are discussed below.

18.10.2.1 JPDF Diagnostic Features

The signals that will be routed into PPDA through connector P1 for diagnostics include:

- An electronic ID identifies the board type, revision, and serial number.
- There are two analog 125 V dc voltage feedbacks: one for the positive bus with respect to earth, one for the negative bus with respect to earth. PPDA uses these signals to create two different signals: voltage magnitude *DC_1285VdbkMag* (difference between positive and negative) and voltage offset *Gnd_FdbkMag* indicative of a system ground. The signal *Gnd_FdbkMag* will read near zero volts with an earth centered floating 125 V dc power system. As the power is offset either positive or negative due to a ground fault, the value of *Gnd_FdbkMag* will show the voltage offset. Voltage feedback accuracy is specified at ±1% of 125 V and exceeds ±0.25% of 125 V or ±0.32 V. Each of these resistive attenuator strings contributes approximately 1.5 MΩ to the bus centering resistance.
- A problem may occur in an installation if the ac power and the 125 V dc bus is cross-wired. The system will often continue to operate since the dc is designed to float, but signal quality may be degraded and additional power system fault opportunities exist. The circuits on JPDF include special features to allow PPDA to detect the presence of ac on the dc bus and indicate the condition to the system. Detection is done by driving the positive bus voltage feedback signal to a negative value, a condition that will never occur without ac present. The PPDA I/O pack then detects this voltage and indicates the presence of ac on the dc power bus by generating a diagnostic alarm..
- Three fuse indications (multiplexed on one analog) provides three Boolean values after PPDA decodes the signal. These signals and the two following signals are created using opto-isolators so they operate correctly on the floating dc bus and do not contribute to the bus centering resistance.
- Three dc/dc fuse indications (multiplexed on one analog) yielding three Boolean values after PPDA decodes the signal.
- Two 125 V out fuse indications (multiplexed on one analog) yielding two Boolean values after PPDA decodes the signal.
- A local ground signal for differential sensing of the above mentioned analog signals.

There is no feedback of the 22 W impedance-limited outputs. These outputs go to contact input boards for contact wetting. The contact input boards have wetting voltage feedback as part of their reported data, so the branch circuit has system feedback through that path. Other core PDM board feedbacks may pass through JPDF using the P2 connector.

Two hardware test rings are provided on JPDF for connection of test equipment. They both feature series 100 kΩ resistors. HW1 is connected to the positive redundant dc bus and is labeled PDC Probe. HW2 is connected to the negative redundant dc bus and is labeled NDC Probe.

18.10.2.2 JPDF Grounding

Mark VIe control systems separate ground into a functional earth (FE) and a protective earth (PE). The protective earth is intended for power distribution functions such as JPDF, while functional earth is used for *quiet* uses such as the control electronics and field signals.

The JPDF mounts to a metal module. Grounding of the JPDF takes place through metal mounting supports fastened to the underlying sheet metal. The ground is applied to the metal switch bodies on JPDF. In addition, the ground is used as a local reference when creating the magnitude feedback signals appearing on P2. The sheet metal of the module is not electrically conductive to the surface upon which it is mounted. This is done specifically to allow definition of the JPDF ground independent of the mounting surface. A typical design can have JPDF mounted to a back-base that is grounded to FE. JPDF can be located low in the cabinet and a separate ground wire from the JPDF module can be provided to PE. Minimum length of this ground wire is essential to keep impedance low at radio frequencies, allowing the input line filters to do their job. In designs where multiple core PDM modules are used, the most desirable ground arrangement involves bonding the sheet metal of adjacent modules together using jumper straps and wire from the point that is near PE.

18.10.2.3 JPDF Physical Arrangement

JPDF is designed to accept power input from the right hand side and deliver power output from the left hand side. When JPDB is used with JPDF, the JAF1 connector provides ac power to JPDF. In this case, the best location for JPDF is underneath JPDB to minimize the JAF1 power wiring. The JPDF with any associated boards should be mounted to allow a minimum length of grounding wire between the module sheet metal and the nearest PE connection point. The P1 and P2 ribbon cable headers on all of the JPDx boards are designed so the JPDS or JPDM holding the PPDA I/O pack is best located at the top of the arrangement. This allows ribbon cables to flow from one to the next, exiting the top and entering the bottom of the next.

18.10.3 JPDF Application Notes

18.10.3.1 JPDF with TBCI

The 125 V contact input terminal board TBCIH1 features 24 circuits in a fairly small space. There are circuit board layout guidelines that define required spacing on the board as a function of voltage level and source impedance. If the unlimited impedance clearance for 125 V is used the spacing required exceeds what is available on TBCI. As a result the decision was made to design TBCI for a *known and controlled* source impedance allowing closer spacing on the board. The source impedance is provided by a pair of 22 ohm resistors in the 125 V dc output of the PDM. In JPDF this is done for connector J12 with the large power resistors mounted underneath the JPDF board in the metal mounting assembly. When TBCI boards are powered from JPDF they should be powered from connector J12. It is entirely appropriate to power these through a JPDD fan-out board as the JPDD fuses are rated for current far in excess of what is available when shorted through the 22 ohm resistors.

18.10.3.2 JPDF with TRPG / TREG

When Mark VIe control trip boards are used in a system there are specific JPDF outputs that should be used. With the TRPG / TREG board pair the power input to the trip solenoids is through the J1 connector on TRPG. The J2 cable between TRPG and TREG then conducts the power to the TREG and solenoids are wired between the boards. Because the power to this board pair is critical to system operation the JPDF has a special output connector to supply this power. J7 is the diode-or of three fused switched branch circuits. It is used specifically to power TRPG J1 so the power to the trip solenoids is from three parallel fused paths.

The TREG board has power input connector JH1 that provides contact wetting voltage to seven optional trip interlock contacts. The board artwork on TREG for the contact inputs is designed with the same clearances described above for TBCI and should be powered from the JPDF J12 connector to use the series 22 ohm resistors.

18.10.3.3 PPDA Configuration with JPDF

The bus voltage feedback is *DC_125VFdbkMag*. The undervoltage diagnostic may be set with **DC_125v_Trig_Volt**. Default is 100 V. The voltage level on *Gnd_FdbkMag* that causes declaration of a ground fault may be specified with **Gnd_Mag_Trig_Volt**. Default is 30 V. Each of the six switched outputs may have their fuse diagnostic disabled by changing the respective value of **FuseDiag** from the default Enable to Disable.

The fuse status can be monitored with:

- FUIR_FU2R_Stat
- FUIS_FU2S_Stat
- FUIT_FU2T_Stat
- FU71_FU72_Stat
- FU73_FU74_Stat
- FU75_FU76_Stat
- FU81_FU82_Stat
- FU83_FU84_Stat
- FU12_FU13_Stat

18.10.4 JPDF Installation

Caution

In 240 V ac applications, do not inadvertently cross-connect the 240 V ac and the dc voltages. The peak voltage will exceed the Transorb rating, resulting in a failure.

Most ac supplies operate with a grounded neutral, and if an inadvertent connection between the 125 V dc and the ac voltage is created, the sum of the ac peak voltage and the 125 V dc is applied to Transorbs connected between dc and ground. However, in 120 V ac applications, the Transorb rating can withstand the peak voltage without causing a failure.

The IS2020JPDF module is base-mounted vertically on a metal back base in a cabinet used by the PDM. A connection must be made between the IS2020JPDF sheet metal and the system protective earth (PE).

Input battery power is applied to terminals DCHI and DCLO. If one or two DACA modules are used, ac power is applied to JAF1, typically from an IS2020JPDB module. DACA modules connect to JPDF through connectors JZ2 and JZ3.

Output circuits are connected as documented for the system.

A power distribution system featuring a PPDA power diagnostic I/O pack requires a 50-pin ribbon cable from JPDF connector P1 to the P2 connector on the board holding PPDA. This connection can pass through other core PDM boards using the P2 connector.

18.10.4.1 Grounding

Warning

When using two JPDF or JPDF boards with JPDC, and if common 125 V dc is used for power distribution, make sure that ground centering jumper(JP1) is set only on one of these boards and not both.

The Mark VIe and Mark VIeS control systems divides ground into a protective earth (PE) and a functional earth (FE). The PE ground must be connected to an appropriate earth connection in accordance with all local standards. The minimum grounding must be capable of carrying 60 A for 60 seconds with no more than a 10 V drop. The FE ground system must be bonded to the PE ground system at one point.

The JPDF is grounded through metal mounting supports fastened to the underlying sheet metal of a metal module. The ground is applied to the metal switch bodies on JPDF. Additionally, the ground is used as a local reference point when creating the feedback signals appearing on P2. The sheet metal of the module is insulated to the surface upon which it is mounted. This is done specifically to allow definition of the JPDF ground independent of the mounting surface. Typically, JPDF is mounted to a back base grounded to FE. JPDF would be located low in the cabinet and a separate ground wire from the JPDF module would be provided to PE. The minimum length of the ground wire is important to keep impedance low at radio frequencies allowing the input line filters to function properly.

18.10.4.2 Physical Arrangement

The JPDF accepts dc power input from the right side of the board and delivers dc power out of the left side. When JPDB is used with JPDF, the JAF1 connector provides ac power to JPDF. JPDF should be physically located beneath JPDB minimizing the length of the JAF1 power wiring. JPDF is mounted to allow a minimum length of grounding wire between the module sheet metal and the nearest PE connection point. Connector P1 transmits feedback signals to a board hosting a PPDA I/O pack. Connector P2 receives feedback from other power distribution boards and passes the signals out of P1 to the PPDA. The P1 and P2 ribbon cable headers on all of the core boards are mounted so the JPDS or JPDM, holding the PPDA I/O pack, is located at the top of the board arrangement. This allows ribbon cables to flow from the top of one board and into the bottom of the next board until the PPDA host is reached.

18.10.4.3 JPDF Ground Fault Detection

Warning

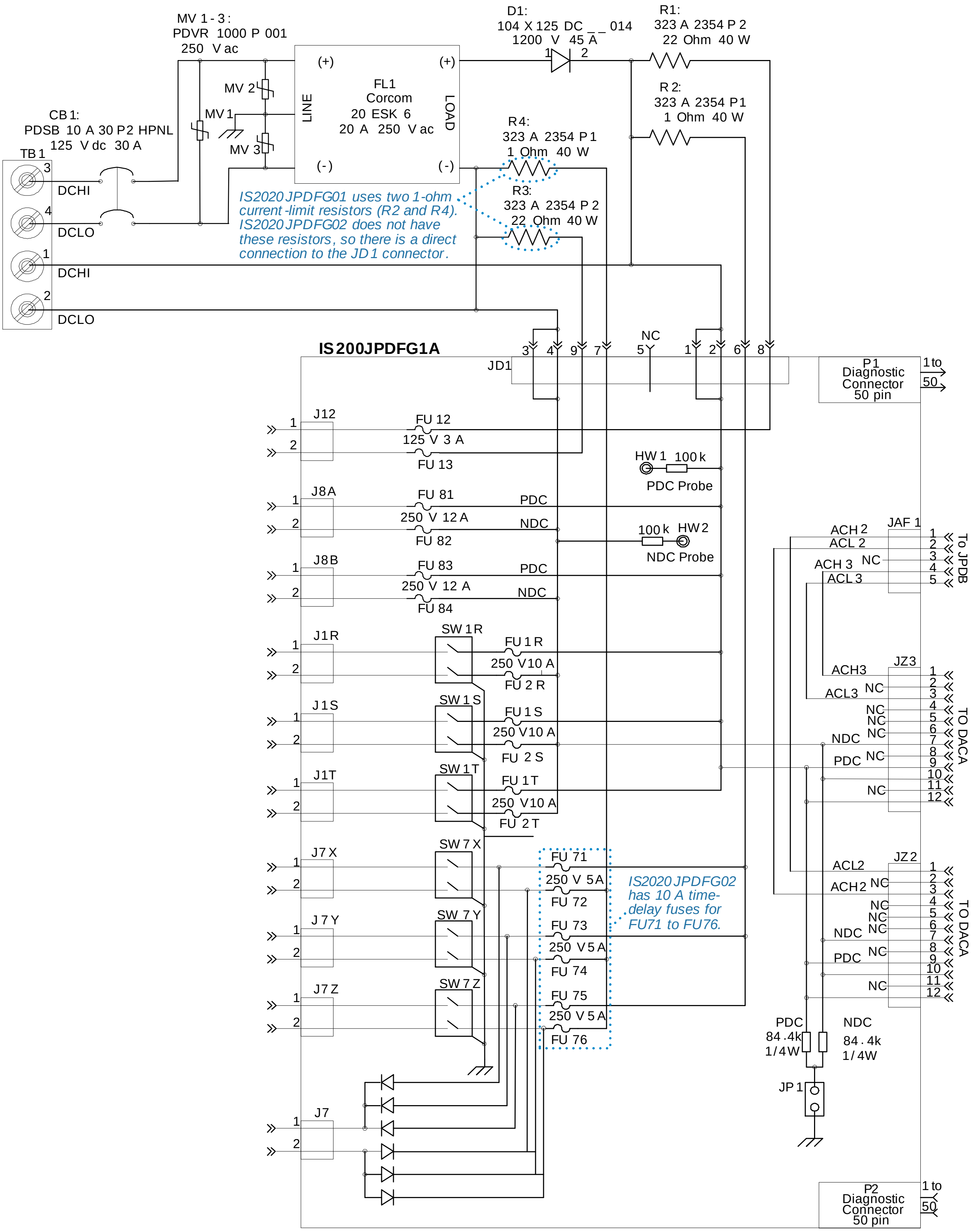
When using two JPDF or JPDF boards with JPDC, and if common 125 V dc is used for power distribution, make sure that ground centering jumper(JP1) is set only on one of the boards and not both.

The IS2020JPDF module supports the use of a dc bus that is centered on ground potential by a high resistance. This arrangement allows the detection of a ground fault when the positive bus or negative bus voltage goes to ground potential. In support of this arrangement, the IS2020JPDF includes separate voltage feedback sensing for positive and negative power with respect to ground. When the feedback is cabled into a PPDA I/O pack detection of ground faults is provided to the system.

The resistance used centering the dc bus on ground sets the ground detection sensitivity and ground fault currents that can flow. IS2020JPDF contains centering resistors selected by jumper JP1. Should centering resistance be provided elsewhere, then the jumper on JPDF should be open. JPDF is designed to then insert minimal centering resistance in the system. If JPDF is providing the centering function, JP1 should be closed.

18.10.5 JPDF Operation

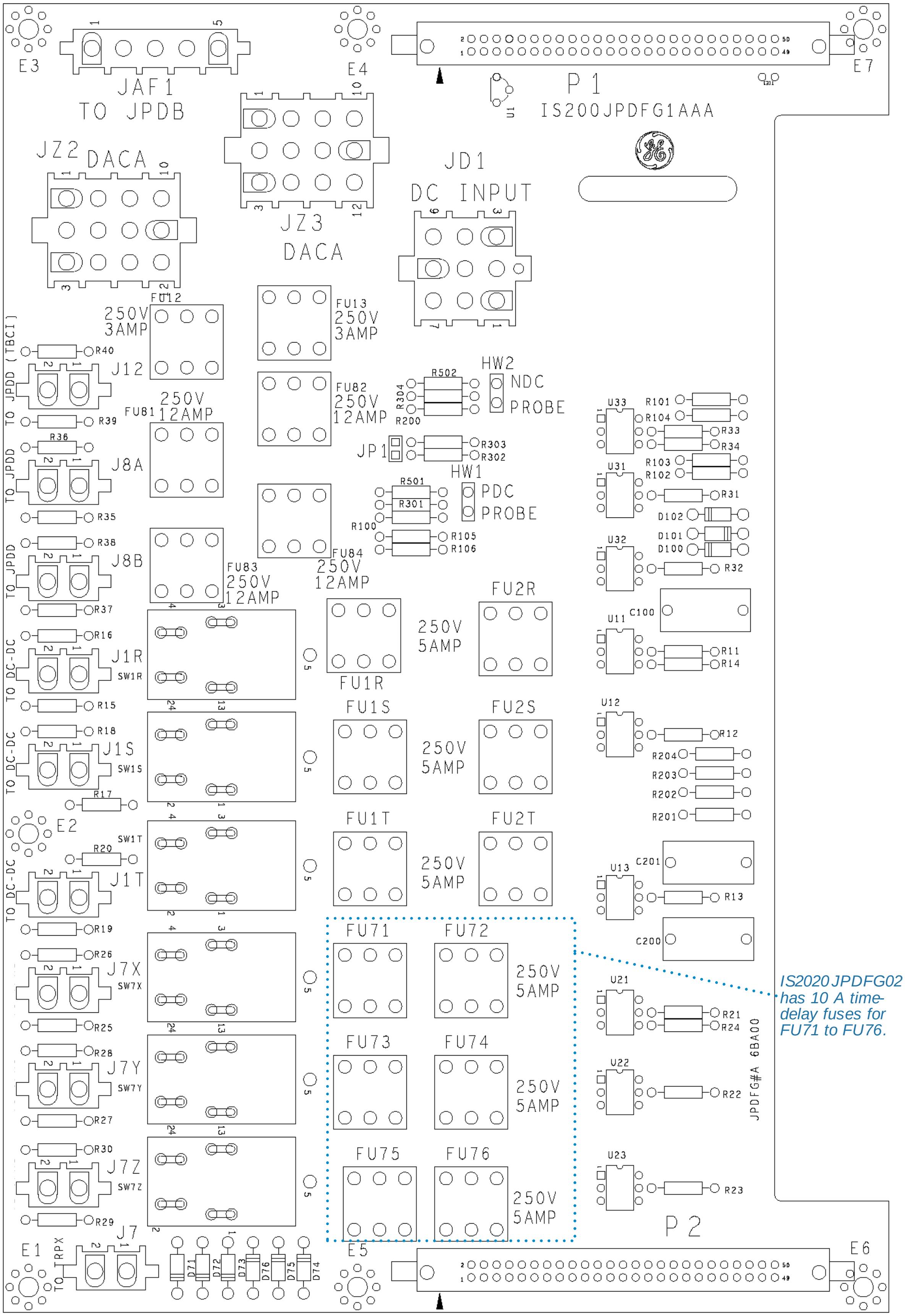
Dc battery power is applied to terminals DCHI and DCLO. It then goes through a 30 A dc circuit breaker into a filter assembly located under the IS200JPDF circuit board. Filtered output is then passed through a series diode to the JPDF circuit board. Ac power is applied to the JAF1 connector. The 115/230 V ac is routed to two connectors, JZ2 and JZ3, and out to two DACA modules. The DACA modules convert the ac power to 125 V dc. The dc power returns to JPDF through different conductors on the same JZ2 and JZ3 connectors.



IS2020JPDFG01 uses two 1-ohm current-limit resistors (R2 and R4). IS2020JPDFG02 does not have these resistors, so there is a direct connection to the JD1 connector.

IS2020JPDFG02 has 10 A time-delay fuses for FU71 to FU76.

JPDF Electrical Diagram



IS2020 JPDFG02 has 10 A time-delay fuses for FU71 to FU76.

JPDF Mechanical Board Layout

18.10.5.1 JPDF Connections

- The JPDF module has a barrier terminal strip containing two battery input screw terminals located on the right side of the circuit board. The dc input is rated at 30 A, and the voltage should never exceed 140 V dc. Protection of the Branch circuit protection supplying power to this input is a 30 A circuit breaker, supplied by default as part of the module. This is the primary power input.
- Two dc output screw terminals, located on the same barrier terminal strip, are not normally used, but are provided to allow two JPDF boards to work in parallel.
- JD1 is a nine-pin Mate-N-Lok connector that accepts the power input from the components that are mounted under the JPDF board. JD1 uses a wire harness that is part of the JPDF module assembly.
- JAF1 is a five-pin Mate-N-Lok connector that accepts the 115/230 V ac input from the JPDB board. The 115/230 V ac is routed to two connectors, JZ2 and JZ3, and out to two DACA modules. The DACA modules convert the ac power to 125 V dc.
- Two 12-pin Mate-N-Lok connectors, JZ2 and JZ3, pass ac power to two DACA modules. The DACA modules convert 115/230 V ac to 125 V dc. Dc power returns through the JZ2 and JZ3 connectors.
- Three fused and switched two-pin Mate-N-Lok output connectors, J1R, J1S, and J1T, are provided for powering 125 V dc/28 V dc power supplies. The 28 V dc is the control power for I/O packs. Positive power is on pin 1 and negative power is on pin 2. The fuses are rated at rated 250 V ac / 125 V dc, 10 A, time delay.
- Three fused and switched two-pin Mate-N-Lok output connectors (J7X, J7Y, and J7Z) with positive power on pin 1, and negative power on pin 2
  - With IS2020JPDFG01, were used for powering up to the legacy Mark VI VPROs, the fuse rating is 250 V ac / 125 V dc, 5 A, fast-acting and two 1 Ω current limit resistors mounted under the board define the minimum source impedance for these circuits
  - With IS2020JPDFG02, are used to power the 125 V dc / 28 V dc converters, the fuse rating is 250 V ac / 125 V dc, 10 A, time delay and there are no current limit resistors for these circuits
- or with IS2020JPDFG01 the 125 V dc / 28 V dc converters. Positive power is on pin 1, negative power is on pin 2, and fuse rating is 5 A. Two 1 Ω resistors mounted under the board define the minimum source impedance for these circuits.
- A two-pin Mate-N-Lok output connector, J7, is provided to supply power to the system trip boards. Positive power is on pin 1 and negative power is on pin 2. The output power comes from the circuits associated with J7X, J7Y, and J7Z. The output power is combined through diodes and is only lost when all three circuits have blown fuses or open switches.
- There are two 12 A fused two-pin, Mate-N-Lok output dc connectors on both J8A and J8B. They feed remote JPDD boards to provide individual switched/fused circuits to TRLY boards and other system loads. Positive power is on pin 1 and negative power on pin 2.
- A two-pin Mate-N-Lok output connector, J12, is provided specifically to operate TBCI contact input boards. Two 22 Ω resistors mounted under the JPDF board define the minimum source impedance for this circuit. Positive power is on pin 1 and negative power is on pin 2.
- The ground reference jumper is JP1. The dc bus is normally operated without a hard ground connection, but it is desirable to center the dc on earth as part of the ground fault detection scheme. In normal operation, the positive terminal would measure ½ *125 V above ground and the negative terminal would measure the same magnitude below ground potential. The resistors used to center the bus on earth can be supplied externally to the JPDF, or on-board resistors can be used by closing jumper JP1.
- Two 50-pin diagnostic ribbon cable connectors, P1 and P2, are supplied on the top and bottom of the board. Connector P1 transmits feedback signals to a board hosting a PPDA I/O pack. Connector P2 receives feedback from other power distribution boards and passes the signals out of P1 to the PPDA.

18.10.6 JPDF Specifications

Item	JPDF Specification
Board Rating	125 V dc nominal, 140 V dc maximum 30 A circuit breaker protection
Impedance to Ground	With JP1 jumper in place > 75 kΩ With JP1 jumper removed > 1500 kΩ
Fuse for Connectors J1R, J1S, J1T - FU1R, FU2R, FU1S, FU2S, FU1T, FU2T	Bussmann MDA-10 or Littelfuse 326010 (250 Vac / 125 V dc, 10 A, time delay, ceramic cartridge, 6.3 x 32mm)
Fuse for Connectors J7X, J7Y, J7Z - FU71-FU76	IS2020JPDFG01: Bussmann ABC-5 or Littelfuse 314005 (250 V ac / 125 V dc, 5 A, fast-acting, ceramic cartridge, 6.3 x 32 mm) IS2020JPDFG02: Bussmann MDA-10 or Littelfuse 326010 (250 Vac / 125 V dc, 10 A, time delay, ceramic cartridge, 6.3 x 32 mm)
Fuse for Connectors JBA, JBB - FU81-FU84	Bussmann ABC-12 or Littelfuse 314012 (250 V ac / 125 V dc, 12 A, Fast-Acting, ceramic cartridge, 6.3 x 32 mm)
Fuse for Connector J12: FU12 - FU13	Bussmann ABC-3 or Littelfuse 314003 (250 V ac / 125 V dc, 3 A, Fast-Acting, ceramic cartridge, 6.3 x 32 mm)
Module Dimensions	30.48 cm High x 21.33 cm Wide x 16 cm Deep (12 in x 8.4 in x 6.3 in)
Mounting	Four mounting holes, #10 screws
Ambient Rating for Enclosure Design†	-40 to 70°C (-40 to 158 °F)

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

18.10.7 JPDF Diagnostics

Diagnostic signals routed into PPDA through connector P1 include:

- An electronic ID identifying the board type, revision, and serial number
- Two 125 V dc voltage feedbacks for voltage magnitude determination, ground fault detection, and ac signal present detection
- Six switched/fused dc supply indications for J1R, J1S, J1T, J7X, J7Y, and J7Z
- Three fused dc supply indications for J8A, J8B, and J12
- Fuse and dry contacts failure diagnostics will not be generated if *InputDiagEnab* on the dc input is set to Disable or the dc input is below 10 V.

18.10.8 JPDF Configuration

JP1 should be in place if JPDF is providing bus voltage centering resistors for ground fault detection. JP1 should be omitted if another location is providing centering resistance.

TBCI boards, when powered by JPDF, should use connector J12 using a JPDD fan-out board. The 44 Ω source impedance is coordinated with the circuit ratings on TBCI.

TRPG/TREG board pair, critical to system operation, should be powered by the J7 connector.

18.11 JPDG Core Power Distribution

The IS200JPDG Power Distribution board provides distribution of 28 V dc (control power) and 48 V / 24 V dc (wetting power) to other boards within the control system. It also provides sensing circuitry for two channels of ac distribution. The JDPG 28 V dc distribution section is designed to accept two separate power supply inputs through external diodes. With the PPDA I/O pack, the JPDG integrates into the PDM system feedback. JPDG can support sensing and diagnostic for two ac signals, which are distributed outside this board.

For control power distribution, the JPDG board receives 28 V dc input power from external ac/dc or dc/dc converters and distributes power to the control system. The JPDG provides fuse protection for all 28 V dc outputs. For wetting power distribution, the JPDG is able to operate at either 24 V dc or 48 V dc. The board receives dc power from two power supplies through external diodes and distributes it to terminal boards and other system loads.

The JPDG does not supply power to bulk 500 W - 24 V input / 28 V output power supplies that provide I/O pack control power. The JPDG supports a floating dc wetting power bus that is centered on earth by using resistors. It provides voltage feedback through the PPDA to detect system ground faults.

18.11.1 Compatibility

The JPDG can host a Power Distribution System Feedback (PPDA) I/O pack. It can also receive diagnostic feedback signals from up to three other distribution boards and route these signals to the PPDA I/O pack. Since the PPDA I/O pack is mounted on the JPDG module, there is no need to transmit diagnostic signals from JPDG to other power distribution boards.

The following table lists all valid combinations of the JPDG with other power distribution boards.

Main Board	Auxiliary Board Supported			
JPDG	JPDE1 24 V	JPDF1 125 V	JPDF2 125 V	JPDB1 ac
Y	N	N	N	N
Y	N	N	N	Y
Y	N	Y	N	N
Y	N	Y	N	Y
Y	N	Y	Y	N
Y	N	Y	Y	Y
Y	Y	N	N	N
Y	Y	N	N	Y
Y	Y	Y	N	N
Y	Y	Y	N	Y
Y	Y	Y	Y	N

Two JPDGs cannot be used in the diagnostic daisy chain for the power distribution system, and JPDS, JPDM or JPDC cannot be used along with JPDG. Only one JPDB can be used along with the JPDG. Two JPDBs are not allowed with the JPDG in the power distribution scheme. Only one JPDE can be used along with JPDG. Two JPDEs are not allowed with JPDG in the power distribution scheme. Two JPDFs can be used along with JPDG. Three JPDFs are not allowed with JPDG in the power distribution scheme.

18.11.2 JPDG Specifications

Item	JPDG Specification	Rating
28 V dc Control Power Inputs	Two 6-pin Mate-N-Lok connectors for 28 V dc power supply inputs: (JR, JS)	Total bus capacity 40 A max steady state at 55°C (131 °F) / 30 A at 70°C (158 °F)
	One 50-pin ribbon cable with diagnostic data from upstream boards (P2)	15 V max
	One 4-pin connector for power supply status contact input (P3)	10 V
28 V dc Control Power Outputs	Four 4-pin Mate-N-Lok connectors for a JPDP/JPDH board (J1-J4)	13 A max per pin connector capacity, 10 A slow blow fuse in positive line, typically Bussmann MDA-10 7 A continuous at 70°C (158 °F)
	Four 2-pin Mate-N-Lok connectors for network switch (JC1-JC4)	Fused with self-resetting fuse 1.875 A; 1.5 A continuous at 70°C (158 °F); 2.0 A continuous at 55°C (131 °F)
	Five 2-pin Mate-N-Lok connectors for I/O packs and controller (JD1-JD5)	Fused with self-resetting fuse 0.8 A; 0.5 A continuous at 70°C (158 °F); 0.9 A continuous at 55°C (131 °F)
	One 62-pin D-shell connection for the PPDA I/O pack (JA1)	
24/48 V dc Wetting Power Inputs	Two 9-pin Mate-N-Lok connectors for 24/48 V dc power supply inputs: (JPS1, JPS2)	Total bus capacity 40 A max steady state, accepts 24 V dc or 48 V dc
	One 4-pin connector for power supply status contact input (P4)	10 V
	Impedance to ground from positive and return line	JP1 jumper in place; 12 kΩ
24/48 V dc wetting power outputs	Seven 2-pin Mate-N-Lok connectors for a wetting power distribution for contact I/Os board (JFA-JFG)	There is a 15 A fuse in both lines, typically Bussmann ABC-15 or Littelfuse 314015P. The maximum current drawn through each connector must not exceed 10 A at 55°C (131 °F); 8 A at 70°C (158 °F).
Inputs for AC Sensing	One 4-pin Mate-N-Lok connector, 2 channels (JAC1)	Only for sensing feedback, no ac distribution through JPDG board
Vibration Protection	JPDGH1A provides standard Mark VIe circuit board vibration protection rating, and should be used for most applications JPDGH2A is enhanced to provide more vibration protection for use in some GE Drilling applications. The purchase price is higher for this version.	
Ambient Rating for Enclosure Design†	-40 to 70ºC (-40 to 158 ºF)	
Board Dimensions	16.51 cm High x 17.8 cm Wide (6.5 in x 7.0 in)	
Mounting	DIN-rail mounting	
	Base mounted steel bracket	

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

18.11.3 Installation

The JPDG is base-mounted vertically on a metal bracket in a cabinet used by the PDM. There is a 50-pin diagnostic connector, P2, mounted on the bottom of the board. JPDG is attached with four screws using the mounting holes located at the top and bottom of the module base. Location within the control cabinet is not critical, however, distribution boards are usually mounted low in the cabinet to facilitate grounding.

The PPDA I/O pack is plugged into connector JA1. It is secured to the JPDG base using an angle bracket, and held in place with nuts threaded onto studs that are permanently attached to the base for that purpose. Diagnostic feedback inputs from other distribution boards are routed to JPDG through a 50-pin ribbon cable attached to connector P2.

Input power connections include:

- Either one or two 28 V dc control power input connections through connectors JR and JS. The JPDG has a common 28 V dc bus.
- 115 or 230 V ac input applied to connector JAC1 only for sensing and diagnostic purpose. The ac voltage is not distributed on the JPDG.
- One or two 24 V dc wetting power input connections or one or two 48 V dc input connections through connectors JPS1 and JPS2. The JPDG has a common 24/48 V dc wetting voltage bus.

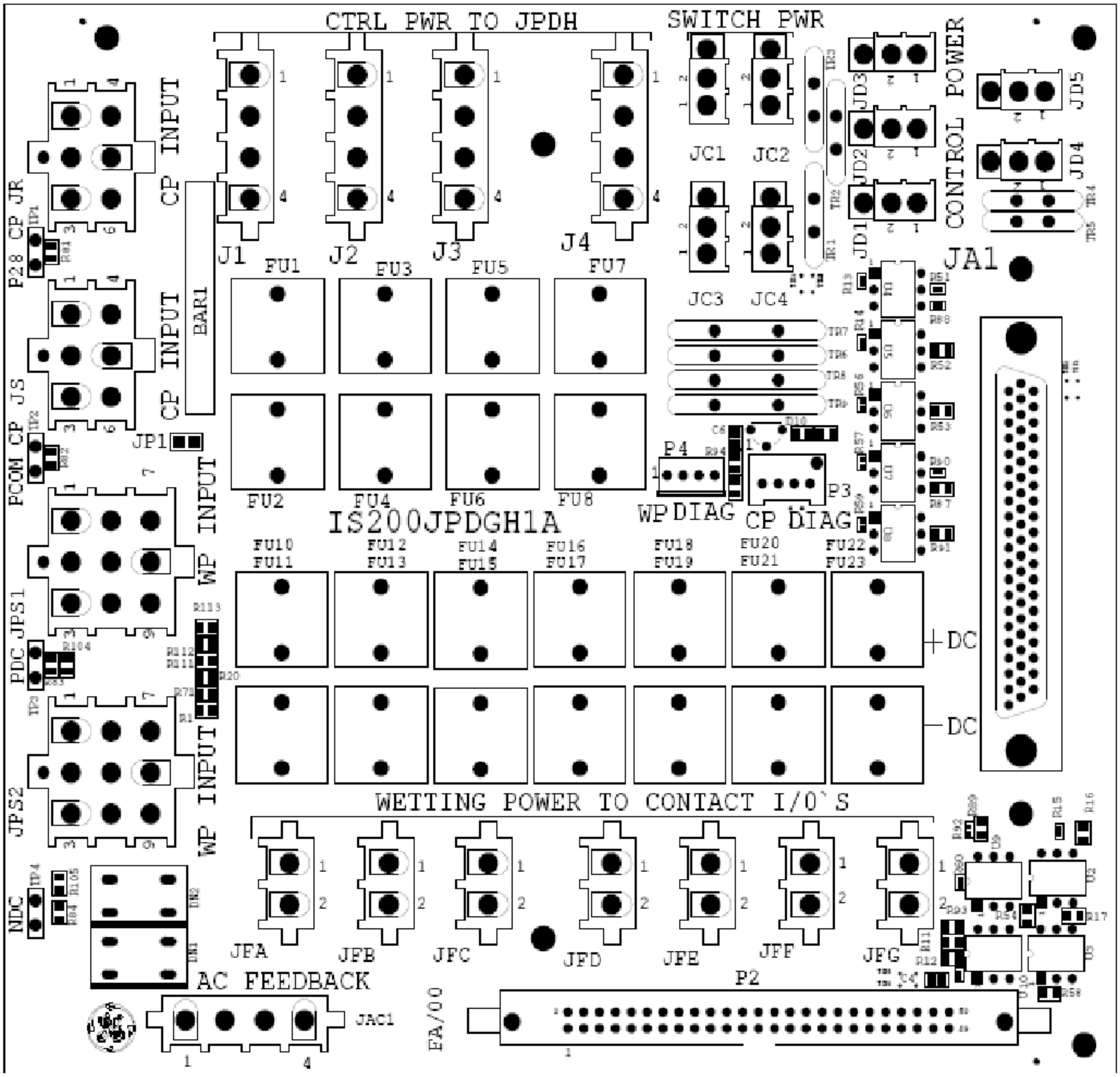
Caution

There is a common electrical bus. Only a single voltage (either 24 V dc to both inputs or 48 V dc to both inputs) can be applied at one time to both inputs through JPS1 and JPS2, through ORed diodes.

Attention

If two dc supplies are connected, external diodes must be used upstream. If external diodes are not used and the voltage levels between the two supplies differ, one supply can drag down the other supply. If one supply fails shorted, then the power bus is likely to also be shorted. Diodes are external to JPDG and may be inside the power supplies or an external assembly.

Note A battery connected directly as wetting voltage is not supported by the JPDG. If a battery needs to be connected with the JPDG for wetting power, the required filter, upstream fuse, and rectifier (the same as that used for the JPDE) must be installed in the panel with proper connections.



JPDG Mechanical Board Layout

18.11.3.1 Grounding

The Mark VIe and Mark VIeS control system divides grounding into protective earth (PE) and functional earth (FE). The PE ground must be connected to an appropriate earth connection in accordance with all local standards. The minimum grounding must be capable of carrying 60 A for 60 seconds with no more than a 10 volt drop. The FE grounding must be bonded to the PE grounding at one point or connected to an independent functional earth grounding system according to local regulations.

The IS200JPDG board is grounded through the sheet metal bracket to the underlying back base. In most cases, this is FE grounding. The FE ground is used as a local reference point when creating the feedback signals appearing on P2. The use of functional earth as a ground reference does not affect the accuracy of the ac voltage detection on JAC1.

18.11.3.2 Physical Arrangement

The cabinet location of the JPDG is not critical. Connector P2 receives feedback from other power distribution boards and passes the signals to the PPDA. The JPDG is vertically mounted, and the PPDA I/O pack is connected to the right side of the JPDG. All the indicator lights on PPDA I/O pack are easily visible.

18.11.3.3 Ground Fault Detection

The JPDG board supports the use of a wetting voltage dc bus that is centered on ground potential by a high resistance. This arrangement allows the detection of a ground fault when the positive bus or negative bus voltage goes to ground potential. In support of this arrangement, the JPDG includes separate voltage feedback sensing for positive and negative power with respect to ground. When the feedback is provided by a PPDA I/O pack, detection of ground faults is provided to the control system.

The resistance used to center the dc bus on ground sets the ground detection sensitivity and the flow of ground fault currents. The JPDG contains centering resistors selected by jumper JP1. If centering resistance is provided elsewhere, this jumper should be open. The JPDG is designed to insert minimal centering resistance in the system. If JPDG is providing the centering function, JP1 should be closed. If a JPDE is also used for distribution of the same wetting power along with a JPDG, only one of the two should have a closed JP1 jumper.

18.11.4 JPDG Operation

18.11.4.1 JPDG Control Power Distribution 28 V DC

The following I/O characteristics apply to the 28 V dc distribution section of the JPDG:

- Two six-pin connectors (JR and JS) are used for input. Each connector uses pins 1-3 for 28 V dc return and pin 4-6 for positive 28 V dc to provide steady state current capacity of 40 A at 55°C (131 °F) / 36 A at 70°(158 °F). Two redundant power supplies feed a single power bus through external ORed diodes.
- Four fused Mate-N-Lok connectors (J1, J2, J3, and J4 having four pins each) are provided to supply 28 V dc power to remote JPDP or JPDH boards. They can also supply power to JPDL boards when using the proper wire harness. Pins 1-2 are 28 V dc return, pin 3 and 4 are positive 28 V dc. Each positive output is fused for 10 A to protect the circuits downstream.
- Five fused Mate-N-Lok connectors (JD1-JD5 with self-resetting fuses of 1.6 A in positive lines) are provided to supply the 28 V power to I/O packs (including PPDA), controllers, and other loads. Pin 1 is positive 28 V dc, and pin 2 is 28 V dc return. The self resetting fuse rating is temperature dependent. It is 1.6 A at 20 °C, 0.9 A at 55°(131 °F), 0.5 A at 70°C (158 °F)ambient temperatures.
- Four Mate-N-Lok connectors (JC1-JC4 with self-resetting fuses of 3.75 A in positive lines) are provided to supply the 28 V power to network switches. Pin 1 is positive 28 V dc, and pin 2 is 28 V dc return. The self resetting fuse rating is temperature dependent. It is 3.75 A at 20°C (68 °F) ambient and derated to 2.0 A at 55°C (131 °F) and 1.5 A at 70°C (158 °F) ambient temperature.
- Connector P3 is used to connect low-level signals capable of monitoring status switches on each 28 V dc power supply and sending feedback signals to the PPDA. Pin 1 provides +10 V dc wetting to the status switch for supply 1. The return is on pin 3. For status switch on power supply 2, pin 2 provides +10 V dc wetting, and the return is on pin 4.
- A DC-62 connector, JA1, is for connection of a PPDA I/O pack. The I/O pack contains status feedback signals for up to three power distribution boards along with JPDG.
- 50-pin diagnostic ribbon cable connector P2 is supplied at the bottom of the board. When connected, P2 receives feedback from another power distribution board and passes the signals to the PPDA.

28 V DC Control Power Distribution

Serial #	Connector name	Function	Pins	Notes/Fuses
1	JR	28 V dc input 1	Pin 1–3 common / return, Pin 4–6 – positive	These connectors are rated for 50 A under fault conditions with current limiting provided by the power source
2	JS	28 V dc input 2	Pin 1–3 common / return, Pin 4–6 – positive	
3	J1	28 V dc output 1 to JPDH/JPDP	Pins 1–2 dc return, pin 3–4 positive	Pin 3 through FU1, Pin 4 through FU2. 10 A replaceable fuses
4	J2	28 V dc output 2 to JPDH/JPDP	Pins 1–2 dc return, pin 3–4 positive	Pin 3 through FU3, Pin 4 through FU4. 10 A replaceable fuses
5	J3	28 V dc output 3 to JPDH/JPDP	Pins 1–2 dc return, pin 3–4 positive	Pin 3 through FU5, Pin 4 through FU6. 10 A replaceable fuses
6	J4	28 V dc output 4 to JPDH/JPDP	Pins 1–2 dc return, pin 3–4 positive	Pin 3 through FU7, Pin 4 through FU8. 10 A replaceable fuses
7	JD1	28 V dc output 1 to I/O pack, Controller	Pin 2 dc return, pin 1 positive	Pin 1 through TR1, 0.8 A self-resetting fuse
8	JD2	28 V dc output 2 to I/O pack, Controller	Pin 2 dc return, pin 1 positive	Pin 1 through TR2, 0.8 A self-resetting fuse
9	JD3	28 V dc output 3 to I/O pack, Controller	Pin 2 dc return, pin 1 positive	Pin 1 through TR3, 0.8 A self-resetting fuse

28 V DC Control Power Distribution (continued)

Serial #	Connector name	Function	Pins	Notes/Fuses
10	JD4	28 V dc output 4 to I/O pack, Controller	Pin 2 dc return, pin 1 positive	Pin 1 through TR4, 0.8 A self-resetting fuse
11	JD5	28 V dc output 5 to I/O pack, Controller	Pin 2 dc return, pin 1 positive	Pin 1 through TR5, 0.8 A self-resetting fuse
12	JC1	28 V dc output 1 to network switch	Pin 2 dc return, pin 1 positive	Pin 1 through TR6, 1.875 A self-resetting fuse
13	JC2	28 V dc output 2 to network switch	Pin 2 dc return, pin 1 positive	Pin 1 through TR7, 1.875 A self-resetting fuse
14	JC3	28 V dc output 3 to network switch	Pin 2 dc return, pin 1 positive	Pin 1 through TR8, 1.875 A self-resetting fuse
15	JC4	28 V dc output 4 to network switch	Pin 2 dc return, pin 1 positive	Pin 1 through TR9, 1.875 A self-resetting fuse
16	P3	28 V dc Power supply status inputs	Pin 1 10 V output for supply 1 status contact Pin 2 10 V output for supply 2 status contact Pin 3 return for supply 1 status contact Pin 4 return for supply 2 status contact	
17	TP1	28 V dc Test point	Positive	
18	TP2	28 V dc Test point	Common / return	

18.11.4.2 Wetting Power Distribution 24/48 V DC

The following I/O characteristics apply to the 24/48 V dc wetting power distribution section of the JPDG:

- Two 9-pin connectors (JPS1 and JPS2) are used for input. Each connector uses pins 1-4 for return and pins 6-9 for positive 24/48 V dc to provide steady state current capacity of maximum 40 A. Pin 5 is not connected. Two redundant power supplies feed a single power bus through external ORed diodes. A directly connected battery as wetting voltage input is not supported. If a battery needs to be connected with the JPDG for wetting power, the required filter, upstream fuse, and rectifier (all are the same used for the JPDE) must be properly installed and used.
- JP1 is the ground reference jumper. The dc bus is normally operated without a hard ground connection. The dc bus is centered on earth as part of the ground fault detection scheme. Normally the 24 V dc positive terminal measures 12 V above ground, and the negative terminal has the same magnitude below ground potential. Close jumper JP1 to use onboard resistors to center the bus on earth, or JP1 is open when resistors are supplied externally to the JPDG or when the JPDE is used with its JP1 jumper closed.
- There are seven (JFA through JFG) fused 2-pin Mate-N-Lok output connectors. They are fused for 15 A in both the lines. Positive power is on pins 1 and negative power is on pins 2. Even though the fuses are of 15 A capacity, the actual current drawn through each branch must not be more than 10 A at 55°C (131 °F); 8 A at 70°C (158 °F). The total current drawn from JFA through JFG must not exceed 40 A steady state.
- Connector P4 is used to connect low-level signals capable of monitoring status switches on each 24/48 V dc power supply and sending feedback signals to the PPDA. Pin 1 provides +10 V dc wetting to the status switch for supply 1, and the return is on pin 3. For status switch on power supply 2, Pin 2 provides +10 V dc wetting, and the return is on pin 4.

24/48 V DC Wetting Power Distribution

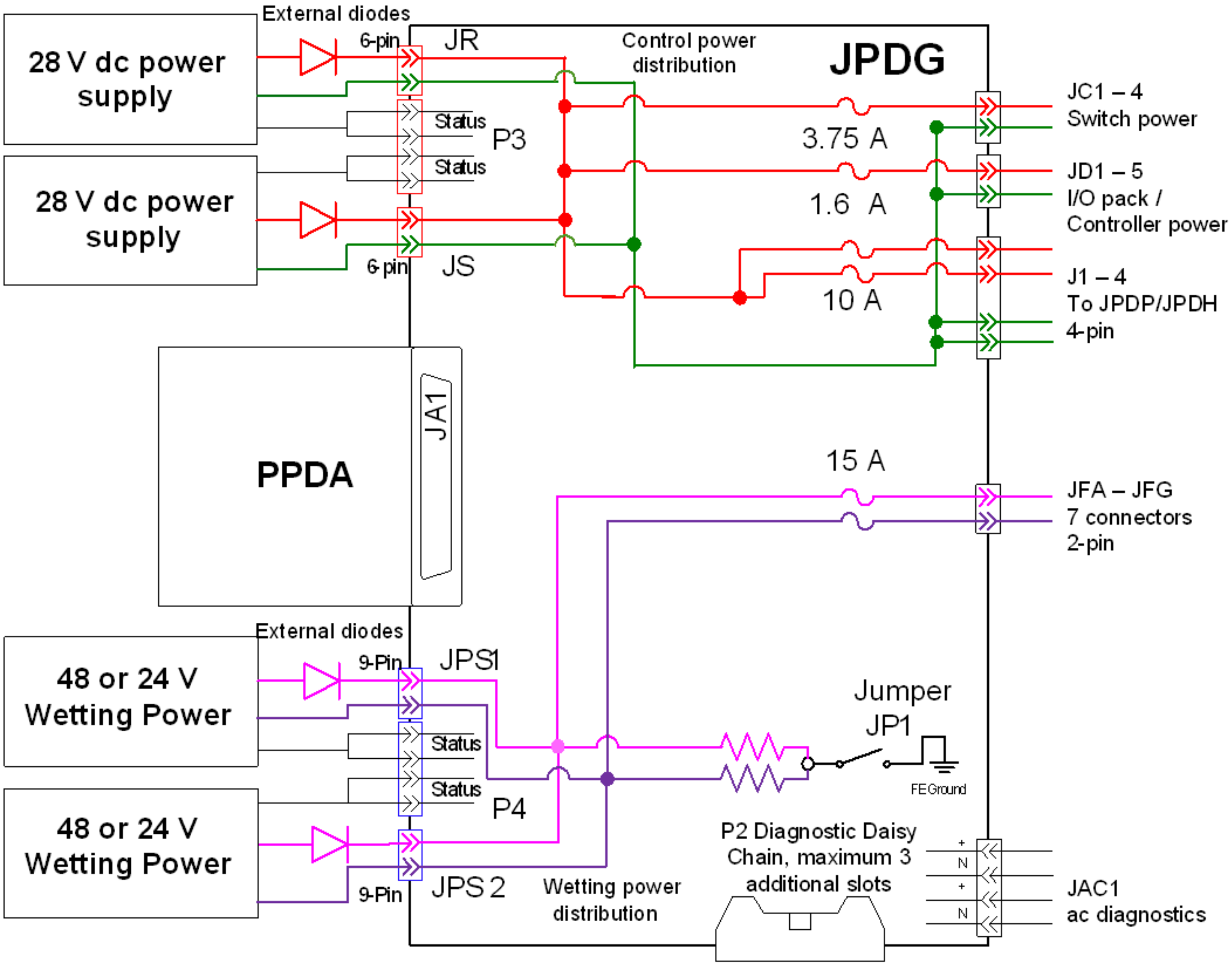
Serial #	Connector Name	Function	Description — Pin numbers	Fuses*
1	JPS1	24/48 V dc input 1	Pin 1–4 — Return, Pin 6–9 — positive	
2	JPS2	24/48 V dc input 2	Pin 1–4 Return, Pin 6–9 — positive	
3	JFA	24/48 V dc output 1	Pin 2 dc return, pin 1 positive	Pin 1 goes through FU10. Pin 2 goes through FU11.
4	JFB	24/48 V dc output 2	Pin 2 dc return, pin 1 positive	Pin 1 goes through FU12. Pin 2 goes through FU13.
5	JFC	24/48 V dc output 3	Pin 2 dc return, pin 1 positive	Pin 1 goes through FU14. Pin 2 goes through FU15.
6	JFD	24/48 V dc output 4	Pin 2 dc return, pin 1 positive	Pin 1 goes through FU16. Pin 2 goes through FU17.
7	JFE	24/48 V dc output 5	Pin 2 dc return, pin 1 positive	Pin 1 goes through FU18. Pin 2 goes through FU19.
8	JFF	24/48 V dc output 6	Pin 2 dc return, pin 1 positive	Pin 1 goes through FU20. Pin 2 goes through FU21.
9	JFG	24/48 V dc output 7	Pin 2 dc return, pin 1 positive	Pin 1 goes through FU22. Pin 2 goes through FU23.
10	P4	24/48 V dc power supply status inputs	Pin 1 is 10 V output for supply 1 status contact Pin 2 is 10 V output for supply 2 status contact Pin 3 is return for supply 1 status contact Pin 4 is return for supply 2 status contact	
11	TP3	24/48 V dc Test point	Positive	
12	TP4	24/48 V dc Test point	Return	

* These are 15 A replaceable fuses, however the actual current drawn through each of these branches must not be more than 10 A.

18.11.4.3 AC Power Diagnostic

An input of either 115 V ac or 230 V ac (distributed external to the JPDG) is supplied to the JPDG through connector JAC1. The JPDG does not distribute the ac power but provides only the diagnostics for two channels of ac. The low or neutral side of the input power should be grounded. Neutral is not grounded on the JPDG.

Serial #	Connector Name	Function	Description — Pin Numbers	
1	JAC1	Two inputs for ac sensing	Pin 1 — Channel 1 phase Pin 2 — Channel 1 neutral Pin 3 — Channel 2 phase Pin 4 — Channel 2 neutral	No ac power distribution, only diagnostics



JPDG Electrical One-line Diagram

18.11.5 Diagnostics

The feedback wiring on the JPDG is different from the other PDM core boards. Using the JA1 connector, the JPDG hosts the PPDA I/O pack. The P1 connector is not there on JPDG. The P2 connector provides feedback signals from other core PDM boards. The following signals are created by the JPDG:

- An electronic ID identifying the board type, revision, and serial number
- Control voltage (28 V dc) measurement reading with accuracy specified at ±1% of full scale
- Fuse feedback status for FU1-FU8 in 28 V dc power distribution section
- Two dc power converter output status (dry contact status) signals for two (28 V dc) power supplies in control power distribution section
- Two testpoints with series 10 kΩ resistors are provided on the 28 V dc bus for external test equipment. TP1 is connected to the positive bus and TP2 is connected to the negative bus. They are used by external test equipment to measure the 28 V power voltage.
- Two analog 24/48 V dc voltage feedbacks are provided. One is for positive bus and one is for negative bus, with the dc bus centered on earth as part of the ground fault detection scheme. Voltage feedback accuracy is ±1%.
- Fuse feedback status for FU10-FU23 in 24/48 V dc power distribution section
- Two dc power converter output (dry contact) status signals for two 24/48 V dc power supplies in wetting power distribution section
- Two testpoints with series 10 kΩ resistors are provided on the 24/48 V dc bus for external test equipment. TP3 is connected to the positive bus and TP4 is connected to the negative bus.
- Two ac supply measurement readings with accuracy specified at ±4% of full scale.

Note Due to a large signal count present on the JDPG, a single set of board feedback signals is not adequate to transmit the signals to a PPDA I/O pack. Each JPDG consumes three sets of feedback signals out of the six available sets.

Note FU1 to 8 and DryCnt1 and 2 are on the 28 V dc input. FU10 to 21 are on the 24 V dc input. Fuse and dry contacts failure diagnostics will not be generated if *InputDiagEnab* on the respective dc input is set to Disable or the dc input is below the low limit threshold. The low limit threshold on 28 V is pre-fixed at 5 V. The low limit threshold on 24 V is pre-fixed at 10 V.

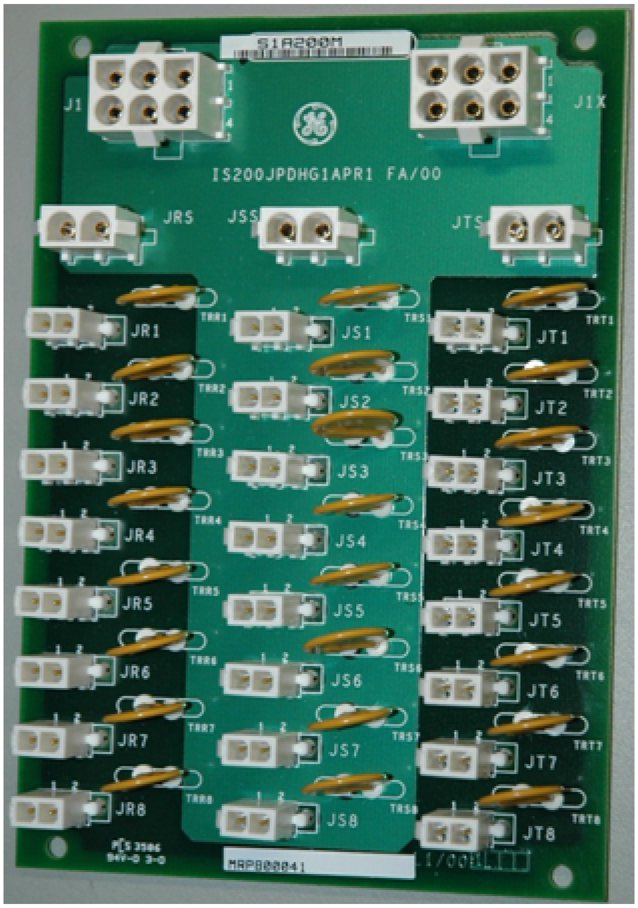
Also, dry contact diagnostics will not be generated if the user selects *NoDryCnt* on the input on which a dry contact exists.

18.11.6 Configuration

When jumper JP1 is in place, the JPDG provides 12 kΩ voltage-centering resistors from positive and negative dc to the local earth connection. When JP1 is removed, the connection to earth is opened. Insert JP1 when a floating dc bus needs to be centered on earth.

18.12 JPDH High Density Power Distribution

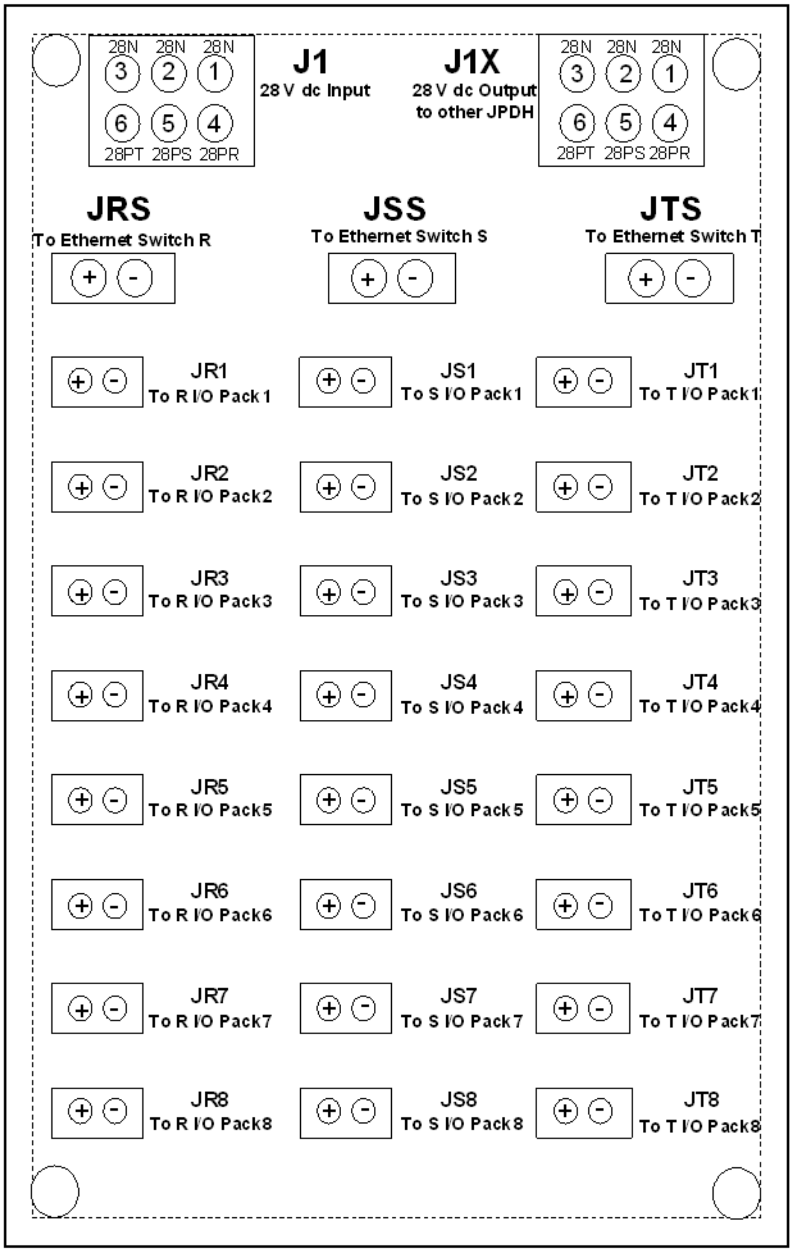
The High Density Power Distribution (JPDH) board provides 28 V dc power to 24 Mark VIe I/O modules and three Ethernet switches from a 28 V dc supply. Additional JPDHs can be connected in a daisy-chain arrangement to provide power to more I/O modules as required. The circuit for each I/O module connector is protected with a positive temperature coefficient fuse device.



JPDH Power Distribution Board

18.12.1 Installation

Mount JPDH on a vertical surface by inserting #6 machine screws through the mounting holes at each corner of the board. Insert Mate-N-Lok connectors as described in the following figure. The 6-pin and larger 2-pin connectors have a nominal rating of 600 V and 13 A, while the smaller two-pin connectors have a nominal rating of 600 V and limited by fuse rating to 0.8 A max.



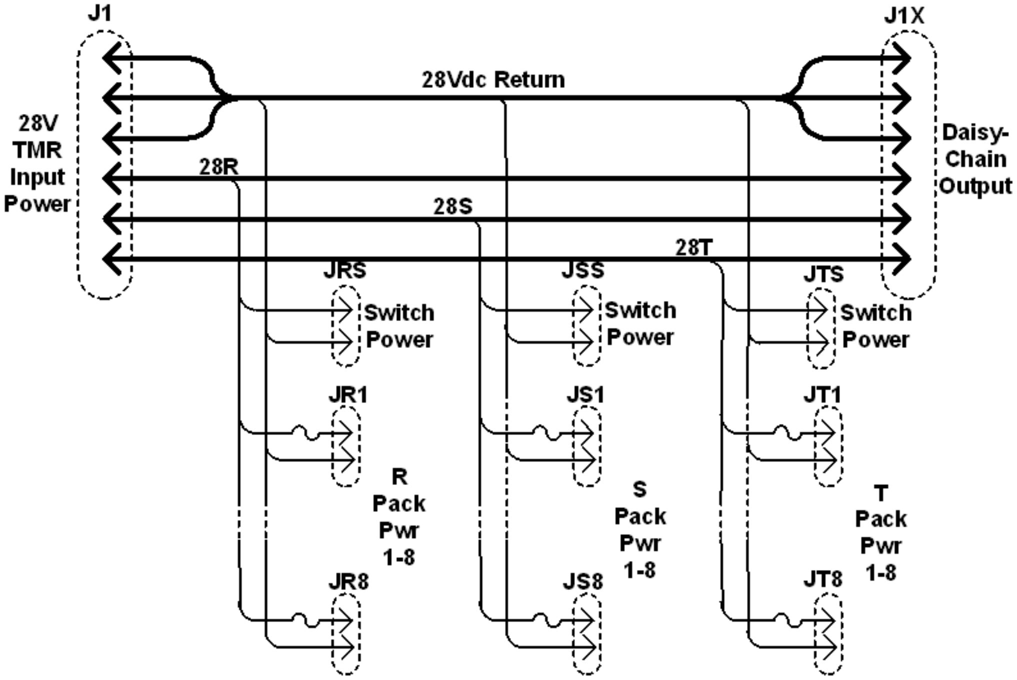
JPDH Connections

18.12.2 Operation

JPDH is designed to provide TMR I/O packs with adequate 28 V dc power distribution while taking up as little space as possible. Additional JPDHs can be connected in a daisy-chain arrangement through the unfused J1X connector.

Note The user must provide suitable branch circuit protection when connecting multiple JPDHs. Each pin is rated at 13 A.

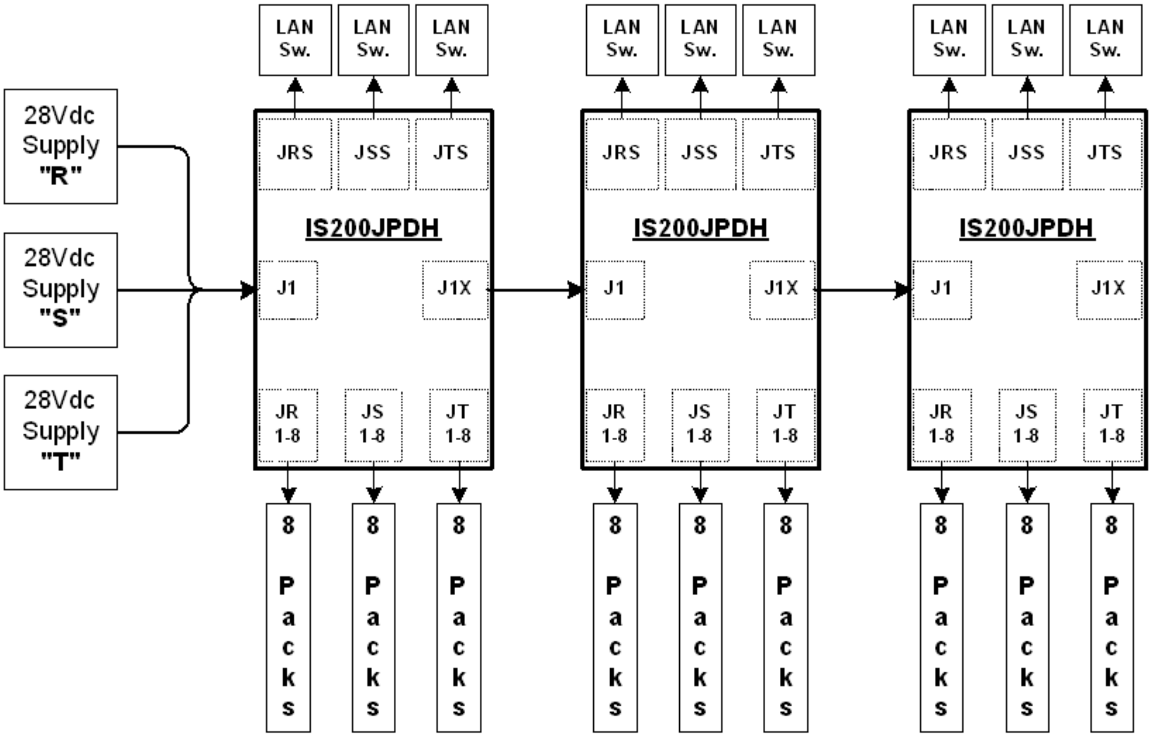
The 6-pin J1 connector brings in three separate 28 V dc feeds on three different pins for triple redundancy. The return current is common among the TMR and daisy-chain feeds and is brought in on the remaining three pins. The following figure explains how the R, S, and T 28 V dc power is distributed by JPDH to the I/O packs and Ethernet switches.



JPDH Power Flow

JPDH has 24 identical output circuits to provide power to the individual I/O packs. The R, S, and T feeds each provide power to eight circuits. Each I/O pack circuit includes a positive temperature coefficient fuse device for branch circuit protection. The board also has three identical unfused output circuits to provide power to each Ethernet switch.

The following figure displays an example application with 72 I/O packs and nine Ethernet switches powered through three daisy-chained JPDH boards.



JPDH Application Example

18.12.3 Specifications

Item	JPDH Specification
Inputs	One 6-pin connection for 28 V dc power input Mate-N-Lok 600 V, 13 A
Outputs	Three 2-pin connections for Ethernet switches Mate-N-Lok 600 V, 13 A Twenty-four 2-pin connections for I/O packs Mate-N-Lok 600 V, 0.8 A at 70 °C
Output Fuses	1.6 A at 20 °C (derated to 0.8 A at 70 °C) positive temperature coefficient fuse or equivalent on each I/O pack output
Ambient Rating for Enclosure Design†	-40 to 70ºC (-40 to 158 ºF)
Relative Humidity	5 – 95% non-condensing
Safety Standards	UL 508A Safety Standard Industrial Control Equipment CSA 22.2 No. 14 Industrial Control Equipment EN 61010-1 Safety of Electrical Equipment, Industrial Machines (Low Voltage Directive)
Board Dimensions	15.875 cm high x 10.795 cm wide (6.25 in x 4.25 in)
Mounting	DIN-Rail, card carrier mounting Base mounted steel bracket, 4 holes

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

18.13 JPDL Local Pack DC Power Distribution

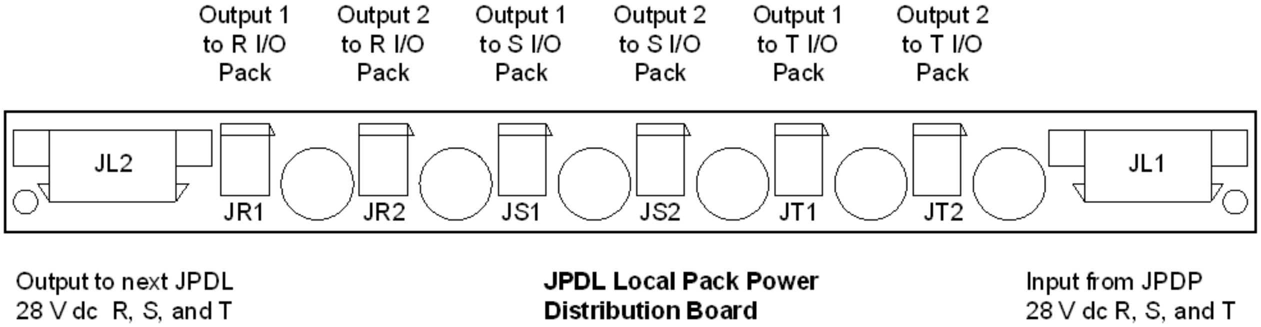
18.13.1 Functional Description

The Local I/O Pack Dc Power Distribution (JPDL) board provides dc power distribution between the source of control power (possibly JPDP, JPDS, JPDM, JPDC, or JPDG) and multiple I/O packs, as well as provides daisy chain style connections for multiple downstream JPDL boards. Branch circuit protection is provided for each I/O pack connection with positive temperature coefficient fuse devices.

The board is designed to make it easy to maintain up to three isolated control power distribution circuits to complement control hardware redundancy. In a TMR system, it will be common to have separate control power for R, S, and T hardware. By providing for three separate power circuits on one board JPDL allows organized separation of the control power.

18.13.2 Installation

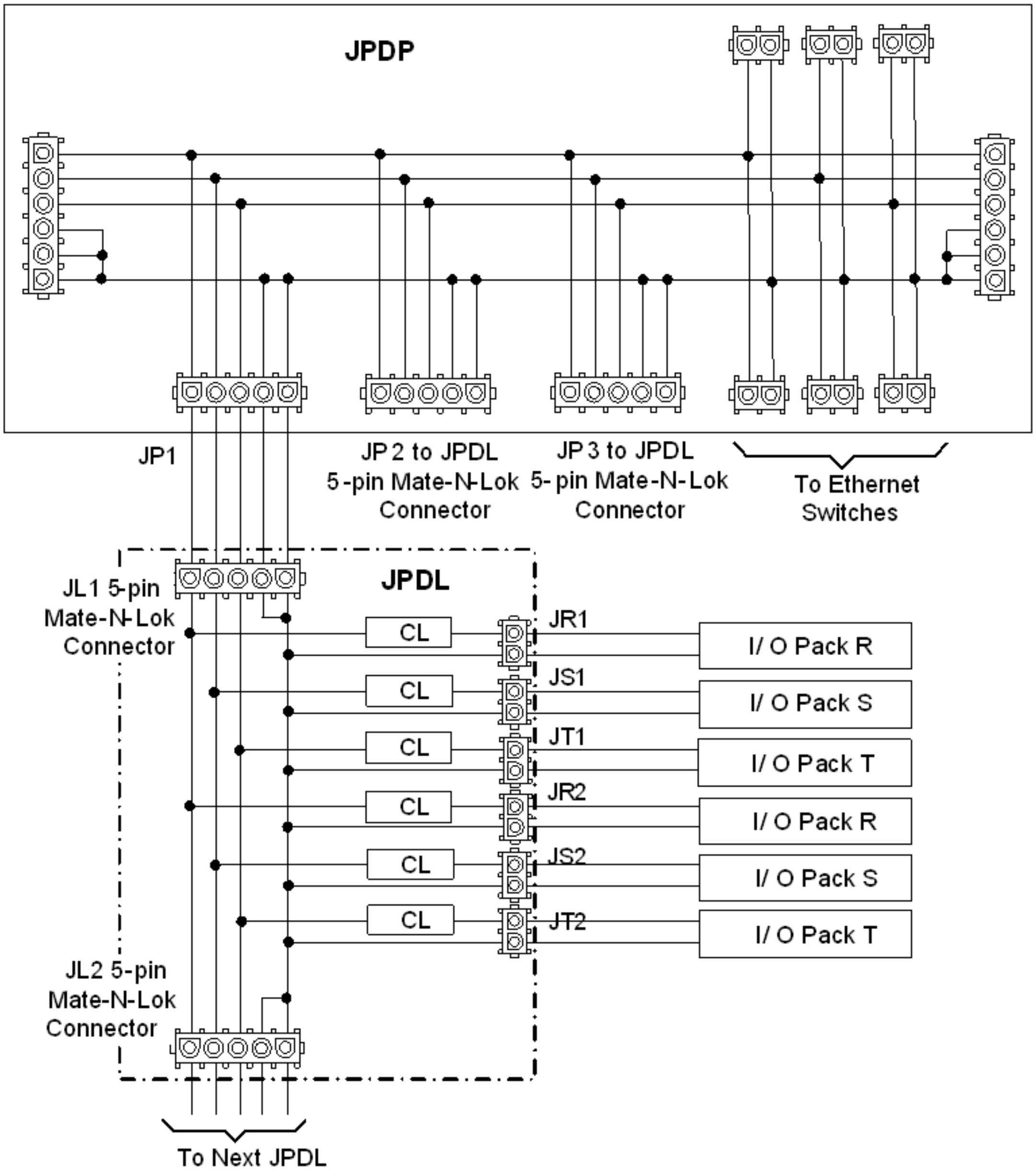
JDPL mounts vertically on a metal bracket next to the I/O packs. Power input cables come in from the back and the output cables come out of the front. All have Mate-N-Lok connectors. For cable destinations, refer to the circuit diagram.



JPDL Cabling

18.13.3 Operation

The following figure explains how the R, S, and T 28 V dc power is distributed in JPDL, and how it reaches the I/O packs. Connector JL2 is used to daisy chain power to multiple downstream JPDL boards.



JPDL Simplified Circuit Diagram with JPDP

18.13.3.1 Inputs

Input power is typically 28 V dc, received from JPDP, JPDS, JPDM, JPDG, JPDC and another JPDL as up to three redundant feeds. The 5-pin Mate-N-Lok input connector receives the three separate power feeds on three different pins for triple redundancy. The feeds are designated Red, Blue, and Black. The JP1, 2, and 3 connectors on JPDP provide this connection. Return current is common among the three TMR feeds and is passed on the remaining two pins of the 5-pin Mate-N-Lok connector.

18.13.3.2 Outputs

Six identical output circuits provide power feeds to individual I/O packs. Two are sourced from each of the R, S, and T feeds (red, blue, and black). Each of the six I/O pack feeds includes a re-setting positive temperature coefficient fuse device, labeled CL (current limit) to provide branch circuit protection that is coordinated with the wire between JPDL and the I/O pack.

18.13.4 Specifications

Item	JPDL Specification	
Inputs	One 5-pin connection with three separate 28 V dc power feeds	red, blue, black, and return
Current	Three power traces will each take 7.5 A continuous	Each trace will take 15 A max. peak
Outputs	Six 2-pin connections for I/O packs, each one with positive temperature coefficient fuse protection to 1.6 A at 20 ºC (derated to 0.8 A at 70 ºC)	2 red, 2 blue, 2 black
	One 5-pin connection with three separate 28 V dc power feeds to downstream JPDLs	red, blue, black, and return
Ambient Rating for Enclosure Design†	-40 to 70ºC (-40 to 158 ºF)	
Board Dimensions	29.21 cm high x 2.54 cm wide (11.5 in x 1.0 in)	
Mounting	Three mounting holes	

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

18.14 JPDM Core Power Distribution

18.14.1 Functional Description

The Power Distribution (JPDM) board receives 28 V dc input power from external ac/dc or dc/dc converters and distributes power to the control system. JPDM provides fuse protection for all outputs. JPDM integrates into the PDM system feedback through the PPDA I/O pack.

JPDM is designed to maintain three separate power buses for R, S, and T applications. Jumpers can be used to provide a single bus with redundant supplies. Two adjacent JPDM boards can be wired together.

The JPDM power distribution board receives 28 V dc power from the chosen supplies and distributes it to system controllers and the branch circuit I/O pack power distribution boards. It is not designed for Class I Division 2 applications because it uses fuses. It is designed to maintain three separate power buses for R, S, and T controls, or it can optionally be jumpered to provide a single bus with redundant supplies. It is also possible to wire two adjacent JPDM boards together. This board is functionally the same as the JPDS except it includes fewer JPDP output connectors and it has fuse protection for all outputs.

18.14.1.1 Compatibility

The IS200JPDM board is compatible with the feedback signal P1/P2 connectors on JPDB, JPDF, and JPDE leading to a PPDA I/O pack. The DC-62 connector on JPDM is compatible with the IS220PPDA I/O pack.

18.14.2 JPDM I/O Characteristics

- Three power supply inputs are provided on JR, JS, and JT. The connector uses pins 8 and 9 for positive 28 V. Pins 1-3 are used for 28 return, providing 24 A steady state capacity. These connectors include low level signals capable of detecting status switches on each supply and generating a feedback signal to the PPDA. Pin 4 provides positive 10 V wetting to the switch, and the return is on pin 5. Pins 6 and 7 are not connected.
- Terminal boards TB1 and TB2 at the bottom and top of the board provide access to the three power buses. If two adjacent JPDM boards are used, jumpers may be placed between TB1 and TB2 on the boards to parallel the bus on the two boards. If it is desired to have a single power bus fed by redundant supplies, jumpers may be placed between PR, PS, and PT terminals to tie the positive bus terminals together.
- Three fused two-pin Mate-N-Lok connectors (JCR, JCS, and JCT) are provided to power controllers or other loads. Pin 1 is 28 V, and pin 2 is the return. Fusing is 15 A, sized to protect the wiring.
- Three two-pin Mate-N-Lok connectors (JAR, JAS, and JAT) with filtering and fusing are provided for auxiliary loads. These outputs feature a series common mode filter inductor and they have self-resetting polysilicon fuses rated for 1.6 A at 20 °C, 0.8 A at 70 °C. Pin 1 is 28 V, and pin 2 is the return.
- Three fused Mate-N-Lok connectors J1-J3 with six pins each are provided to supply R, S, and T power to remote JPDP or JPDH boards, or directly to JPDL boards when used with the appropriate wire harness. On all six connectors pins, 1-3 are 28 V return, pin 4 is 28 R, pin 5 is 28 S, and pin 6 is 28 T. Each positive output wire is fused for 15 A to protect the wiring.
- The DC62 connector JA1 is for a PPDA power diagnostic I/O pack. It contains the status feedback signals for up to six core power distribution boards.
- P4 is provided to supply power to the PPDA I/O pack. It is a power circuit formed from R, S, and T power using a diode-or arrangement followed by a polysilicon self-resetting fuse rated for the PPDA power requirements. This ensures that the I/O pack receives power if any of the three power buses are active.
- Diagnostic daisy chain 50 pin ribbon cable connectors P1 and P2 are located on top and bottom of the board. They are used for pass-through of the diagnostic signals.

18.14.2.1 JPDM Diagnostic Features

JPDS and JPDM have feedback wiring that different from the other core PDM boards. One JPDS or JPDM will host the PPDA I/O pack on the JA1 connector. On that board, the P1 connector is not used because the output signals are sent to the PPDA. If a second JPDS or JPDM board is used, the P1 connector on the second board will be used to conduct its feedback into P2 of the board hosting the PPDA. In either case, the P2 connector provides passage of feedback signals from other core PDM boards. The following signals are created by JPDM:

- An electronic ID identifies the board type, revision, and serial number.
- PS28vStat_R, _S, _T are three analog P28 voltage readings for R, S, and T bus. Separate analog feedback signals are used. Accuracy is specified to be ±1% of full scale and calculated accuracy is ±0.2% at 3 sigma.
- One dry contact from each of three power supplies (DryCntStat_R, _S, _T) yields three Boolean values.
- Three Aux output fuse status signals (AuxFuseStat_R, _S, _T) multiplexed into a single analog value yields three Boolean values after.
- Three control output fuse status signals (FU1_Stat through FU3_Stat) plus 9 J1, J2, and J3 fuse output signals (FU4_Stat through FU12_Stat).

JPDM is a special case for feedback wiring. Due to the large signal count present on this board (15 fuses, 3 contacts, and 3 bus voltages) a single group of five analog board feedback signals are not adequate to transmit all of the information to the PPDA. When JPDM hosts the PPDA I/O pack, it uses two groups of feedback signals limiting the system to a maximum of 5 PDM boards instead of six. If a second JPDM is included in the system and wired into PPDA using the P1 connector, it consumes an additional two groups of feedback signals limiting the system to a maximum of four PDM boards instead of six.

JPDM provides the following four test point outputs for connection of external test equipment:

- HWI - 28PR
- HW2 - 28PS
- HW3 - 28PT
- HW4 - 28N

The positive side test points include series 10 kΩ current limiting resistors. These allow access to all three 28 V power buses and the common return circuit.

18.14.2.2 JPDM Grounding

Mark VIe control systems separate ground into a functional earth (FE) and a protective earth (PE). The PE is intended for power distribution functions such as JPDF, while functional earth is used for *quiet* uses such as the control electronics and their power as on JPDM.

Grounding of the JPDM takes place through metal mounting standoffs fastened to the underlying sheet metal. The ground is used as a local reference when creating the magnitude feedback signals appearing on P2 and JA1. The JPDM is expected to be part of the FE system in a control and mounting on a FE potential back-base is normal practice. This is different than JPDB, JPDE, and JPDF where a PE connection is desired.

The IS200JPDM board is grounded through the sheet metal bracket to the underlying back base. In most cases, this is the system FE.

18.14.2.3 JPDM Physical Arrangement

JPDM is designed to accept power input from cables into the JR, JS, and JT connectors so it exhibits less mounting position sensitivity than some other boards. As mentioned, it is expected that the mounting surface will be at functional earth potential. If the board hosts a PPDA I/O pack, consideration should be given to visibility of the indicator lights on the top of PPDA. If two JPDM boards are used together, arrange them next to each other to make it easier to use any needed barrier terminal strip connections. The P1 and P2 ribbon cable headers on all of the JPDx boards are designed so the JPDS or JPDM holding the PPDA I/O pack is best located at the top of the arrangement. This allows ribbon cables to flow from one board to the next, exiting the top and entering the bottom of the next board until the PPDA host is reached.

The JPDM accepts power from cables and distributes it to the JR, JS, and JT connectors. JPDM, when hosting a PPDA I/O pack, will be mounted so indicator lights on the pack are easily visible. Two JPDM boards, when used together, will be mounted so that all terminal board connections are easily accessible. The location of JPDM is not critical in a panel. Connector P1 transmits feedback signals to a board hosting a PPDA I/O pack. Connector P2 optionally receives feedback from another power distribution board and passes the signals out of P1 towards the PPDA. If a feedback cable connection from JPDM P2 to another power distribution board is used, consideration should be given to the feedback cable routing.

18.14.3 JPDM Application Notes

In TMR systems it is generally desirable to maintain separate R, S, and T power systems throughout the control. When used this way, JPDM will have three power supply inputs. The barrier terminal at the top and bottom of the board will not be used to connect the three separate supplies. In dual systems, it is common to use dual redundant power supplies for 28 V power. When this is done, the positive side of the P28 R, S, and possibly T buses need to be connected using jumpers applied to one of the barrier terminal strips. It is also possible to use three supplies tied together into a single supply bus if desired.

Because JPDM does have output circuit fusing it is acceptable to use two or more 500 W power supplies connected together into a single output bus.

The internal wiring is designed so that three independent 28 V dc power buses can be maintained, or all three can be combined into a single internal bus. Each bus is sized to handle 25 A. They share a common ground sized for 75 A. With three supplies, it is possible to operate R, S, and T controllers and their I/O from separate power supplies. Failure of a supply can cause its controller and I/O to go offline while not affecting the other two channels. There is a dedicated 28 V power output for the PPDA I/O pack ensuring power system feedback is available if a channel power failure occurs.

A second method of operation has jumpers placed between the R, S, and T 28 V bus connection screws on TB1 and TB2. The board then provides a single highly reliable source of 28 V. Up to three supplies could power this bus with parallel operation capability designed into the external supplies. When buses are paralleled, the rating becomes the sum of the paralleled circuits. Three 25 A circuits paralleled yield a 75 A capability.

A third method of operation involves using the TB1 and TB2 screw terminals to parallel the power buses between two adjacent JPDM boards. Features offered by two boards include:

- Two sets of control rack output for duplex or TMR applications using redundant supplies in the control racks, or systems where more than three supplies are to be paralleled. The supply inputs would be fed from the same sources, with outputs fed to separate JPDM boards. This allows for the system to have more than 25 A capacity on the control 28 V outputs and/or allow for a dual failure of two supplies to not impact all of the 28 V circuits. For example, if the system will have a 30 A load, separate the loads into two groups, select supplies for each group with adequate ratings, route the two group supplies using separate JPDM boards, and route from the appropriate JPDM through JPDP boards to the output device(s) for that group of devices. It is highly recommended that the separate groups of outputs be physically separate panels within the cabinet containing the separate power feeds. When selecting the supplies, ensure the following:
  - The output rating for each supply must be matched to the worst case load for that branch.
  - The input type (ac/dc or dc/dc) is the same to maintain the redundant source feeds and monitoring.
- Six JPDP outputs instead of three
- Separated R, S, and T power may have two input power supplies providing supply redundancy on each bus.

In some applications, it could be desirable to apply a battery bus as a power backup. It is possible to use a grounded battery system as input to this board using the screw terminals on the end of the board. This requires diodes not on JPDM to provide isolation between the battery and internal bus, because the JPDM is not designed to function as a battery charger.

Note During installation or repair, any configuration performed through the barrier terminal strips must match system documentation.

18.14.3.1 PPDA Configuration with JPDM

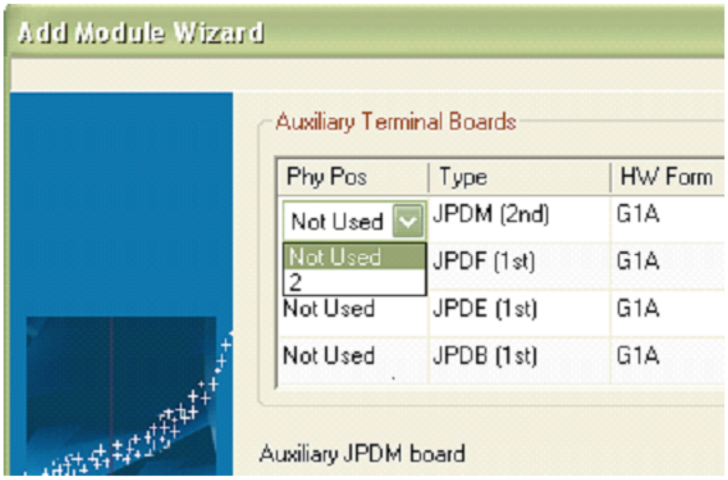
If one or two of the 28 V circuits are not powered, the undervoltage detection for that circuit can be disabled by changing the value of *PS28vEnable*. This also removes the alarm driven by the power supply dry contact monitor associated with that circuit. Because of the high feedback signal count, JPDM uses more PPDA resources. PPDA is able to support fewer connected core PDM boards when JPDM is present.

Note If the Dry Contact status feedback from the Power supply are not used, the *PS28vEnable* can be set to *NoDryCnt* to continue to allow the 28 V input to be used, but disable diagnostic alarms driven by the power supply dry contact monitor.

18.14.4 JPDM Installation

The JPDM is base-mounted vertically on a metal bracket in a cabinet used by the PDM. Refer to the wiring diagrams for power input and output. There is a 50-pin diagnostic connector, P1/P2, mounted on the top and bottom of the board.

Both the JPDC and JPDM power distribution boards consume two groups of feedback signals with the PPDA I/O pack, so when used, the next available position will be two groups higher.



Phy Pos	Type	HW Form
Not Used	JPDM (2nd)	G1A
	JPDF (1st)	G1A
Not Used	JPDE (1st)	G1A
Not Used	JPDB (1st)	G1A

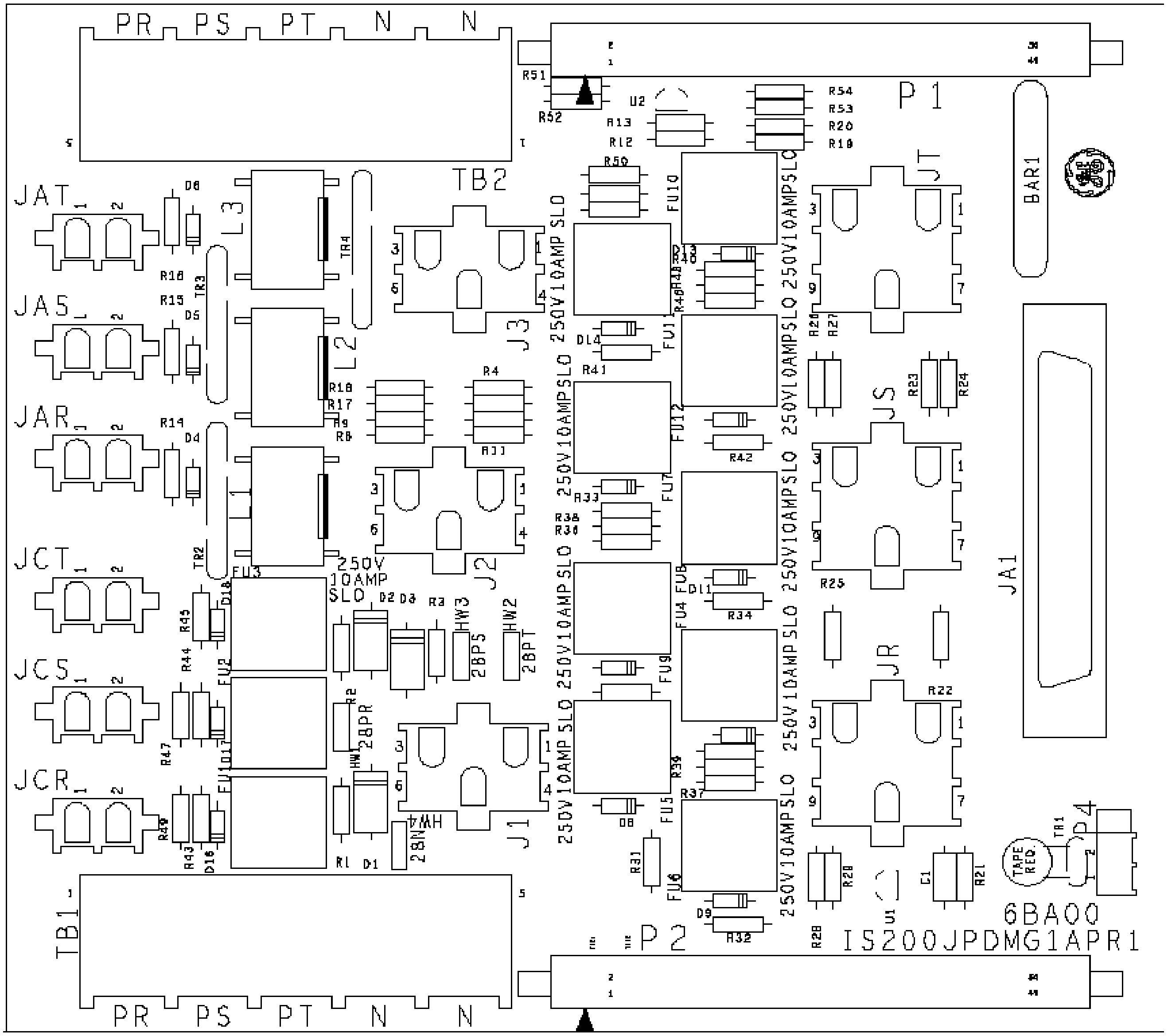
Auxiliary JPDM board

18.14.5 JPDM Operation

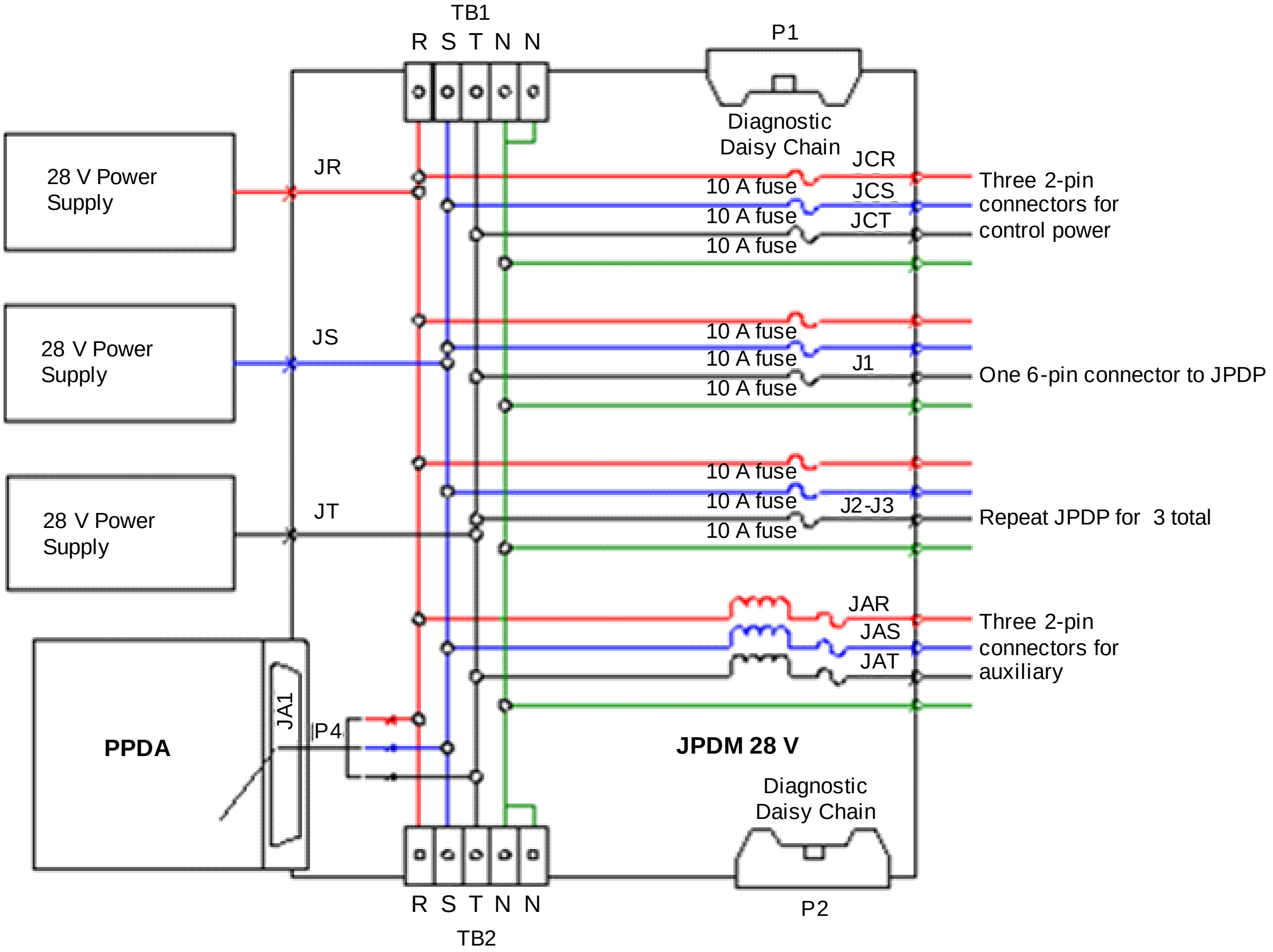
The following I/O characteristics apply to the JPDM module:

- JPDM supplies three power supply inputs on JR, JS, and JT. Each connector uses pins 8 and 9 for positive 28 V dc and pins 1-3 for 28 V dc return providing 24 A steady state capacity. These connectors include low-level signals capable of monitoring status switches on each supply and sending feedback signals to PPDA. Pin 4 provides +10 V dc wetting to the status switch and return is on pin 5.
- Terminal boards TB1 and TB2 at the bottom and top of the board provide access to the three power buses. Jumpers can be used to parallel the bus between TB1 and TB2 when more than one JPDM board is used. Jumpers can also be used between terminals PR, PS, and PT to tie the positive bus terminals together when a single power bus is fed by redundant power supplies.
- Three fused two-pin Mate-N-Lok connectors, JCR, JCS, JCT power controllers, and other loads. Pin 1 is +28 V dc and pin 2 is the return. A 10 A fuse protects the circuit.

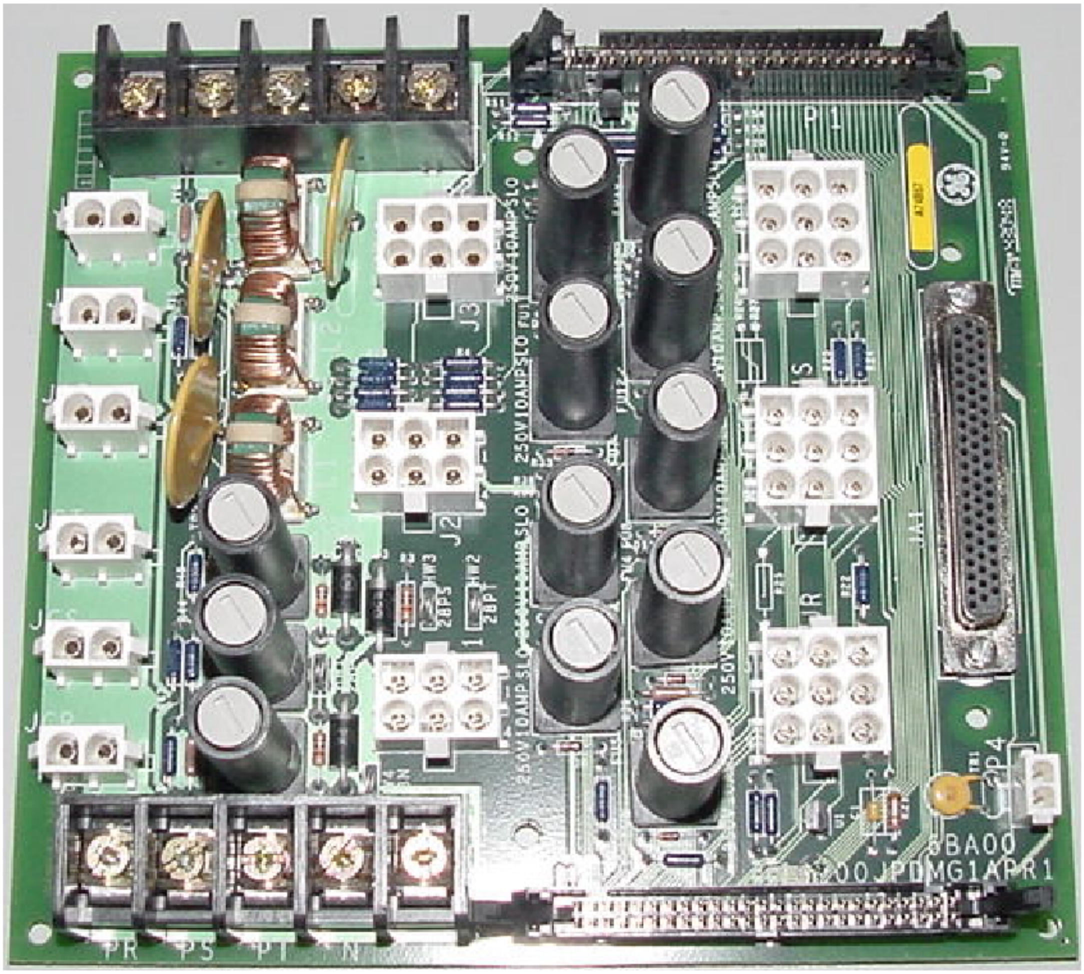
- Three fused Mate-N-Lok connectors, J1, J2, and J3 have six pins each are provided to supply R, S, and T power to remote JPDP boards. They can also supply JPDL boards when using the proper wire harness. Pins 1 – 3 are 28 V dc return, pin 4 is +28R, pin 5 is +28S, and pin 6 is +28T. Each positive output is fused for 15 A to protect the circuits.
- A DC-62 connector, JA1, is for connecting to a PPDA I/O pack. The pack contains status feedback signals for up to six core power distribution boards.
- P4 supplies power to the PPDA I/O pack. It uses R, S, and T power using a diode-OR arrangement in addition to a self-resetting fuse. This ensures the pack receives power if any of the three power buses are active.
- Two 50-pin diagnostic ribbon cable connectors, P1 and P2, are supplied on the top and bottom of the board. Connector P1 transmits feedback signals to a board hosting a PPDA I/O pack. Connector P2, when connected, receives feedback from another power distribution board and passes the signals out of P1 towards the PPDA.



JPDM Mechanical Board Layout



JPDM Simplified Circuit Diagram



JPDM Board

18.14.6 JPDM Specifications

Item	JPDM Specification	
Inputs	Three 9-pin connections for 28 V dc Power Supply inputs 5-screw terminal block for daisy chaining power distribution boards	25 A max each 35 A max per screw
Outputs	J1-J3 connections for either JPDP or JPDL boards	10 A 250 V fuse per circuit, Bussmann MDA-10 typical.
	JCR, JCS,JCT connections for controller power	10 A 250 V fuse per circuit, Bussmann MDA-10 typical.
	JAR, JAS, JAT connections, filtered and fused, for auxiliary devices	3.75 A at 20 ºC, derated to 1.88 A at 70 ºC self-resetting fuse per circuit
	P4 connection for PPDA I/O pack power	0.25 A max
	JA1 connection for PPDA power diagnostics	±5 V max
Ambient Rating for Enclosure Design	-40 to 70ºC (-40 to 158 ºF) *Refer to GEH-6721_Vol_I, the chapter Technical Regulations, Standards, and Environments.*	
Board Size	16.51 cm High x 17.8 cm Wide (6.5 in x 7.0 in)	
Mounting	DIN-rail mounting or base mounted steel bracket	

18.14.7 JPDM Diagnostics

The feedback wiring on JPDS and JPDM is different from the other PDM core boards. One JPDS or JPDM can host the PPDA I/O pack using the JA1 connector. The P1 connector is not used in this configuration because the output signals are going directly to PPDA. When a second JPDS or JPDM board is used, the P1 connector on the second board can be used for feedback into P2 of the board hosting PPDA. In both configurations, the P2 connector provides feedback signals from other core PDM boards. The following signals are created by JPDM:

- An electronic ID identifying the board type, revision, and serial number
- Three analog 28 V dc readings for the R, S, and T bus power supplies. Separate analog feedback signals are used. Accuracy is specified at ±1% of full scale.
- Each power supply connector (JR1, JS1, JT1) has provisions for a dry contact indicating power supply status. JPDS conditions these signals and places them in the feedback signal set.
- Auxiliary Supply status feedback from downstream of the fuses provides three feedback signals to PPDA.
- Three control output fuse status signals plus nine J1 – J3 fuse output signals provide 12 feedback signals to PPDA

Due to a large signal count present on JPDM (15 fuses, 3 contacts and 3 bus voltages), a single set of board feedback signals is not adequate to transmit the signals to a PPDA I/O pack. Each JPDM consumes two sets of feedback signals out of the six available sets. The JPDS contains test rings for 28 V dc power from the three internal circuits, 28PR, 28PS, and 28PT. Each test ring has a series 10 k resistor to isolate the ring, and there is a single grounded ring 28N for the return path. These can be used to measure the 28 V dc power voltage using external test equipment.

Note Fuse and dry contacts failure diagnostics will not be generated if *InputDiagEnab* on the respective dc input (R/S/T) is set to Disable or the dc input is below the low limit threshold, 5 V. Fuses 1, 4, 7, and 10 are on the R supply. Fuses 2, 5, 8, and 11 are on the S supply. Fuses 3, 6, 9, and 12 are on the T supply.

Also, dry contact diagnostics will not be generated if the user selects *NoDryCnt* on the input on which a dry contact exists.

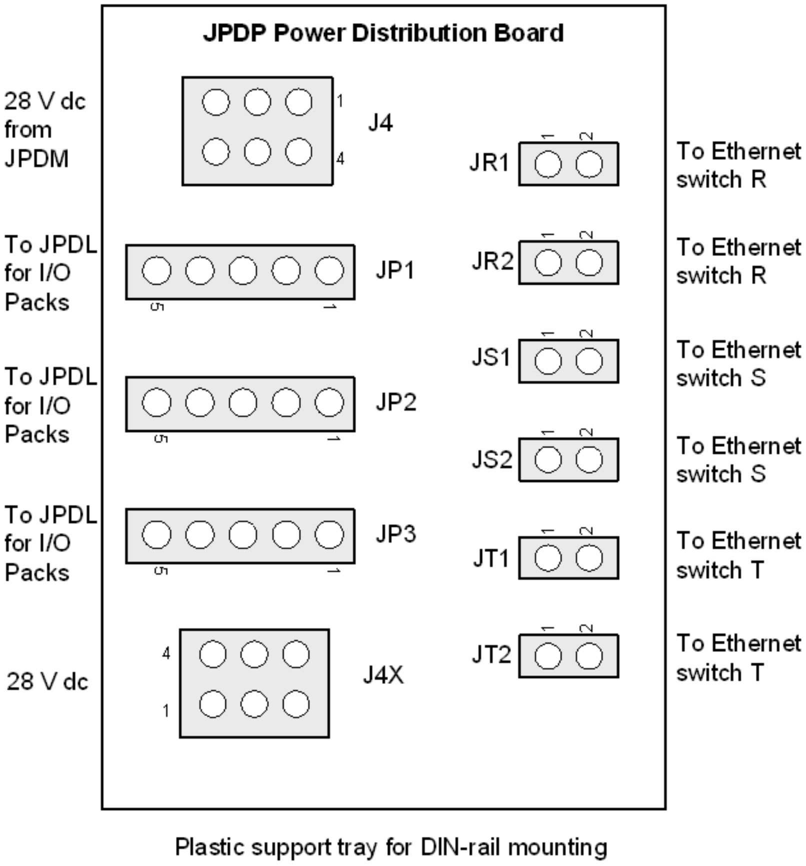
18.15 JPDP Local Power Distribution

18.15.1 Functional Description

The Local Power Distribution (JPDP) board provides intermediate 28 V dc power distribution from the JPDS, JPDM, JPDC, or JPDG board to multiple JPDL boards for further distribution to the I/O packs. JPDP also optionally provides power to Ethernet switches.

18.15.2 Installation

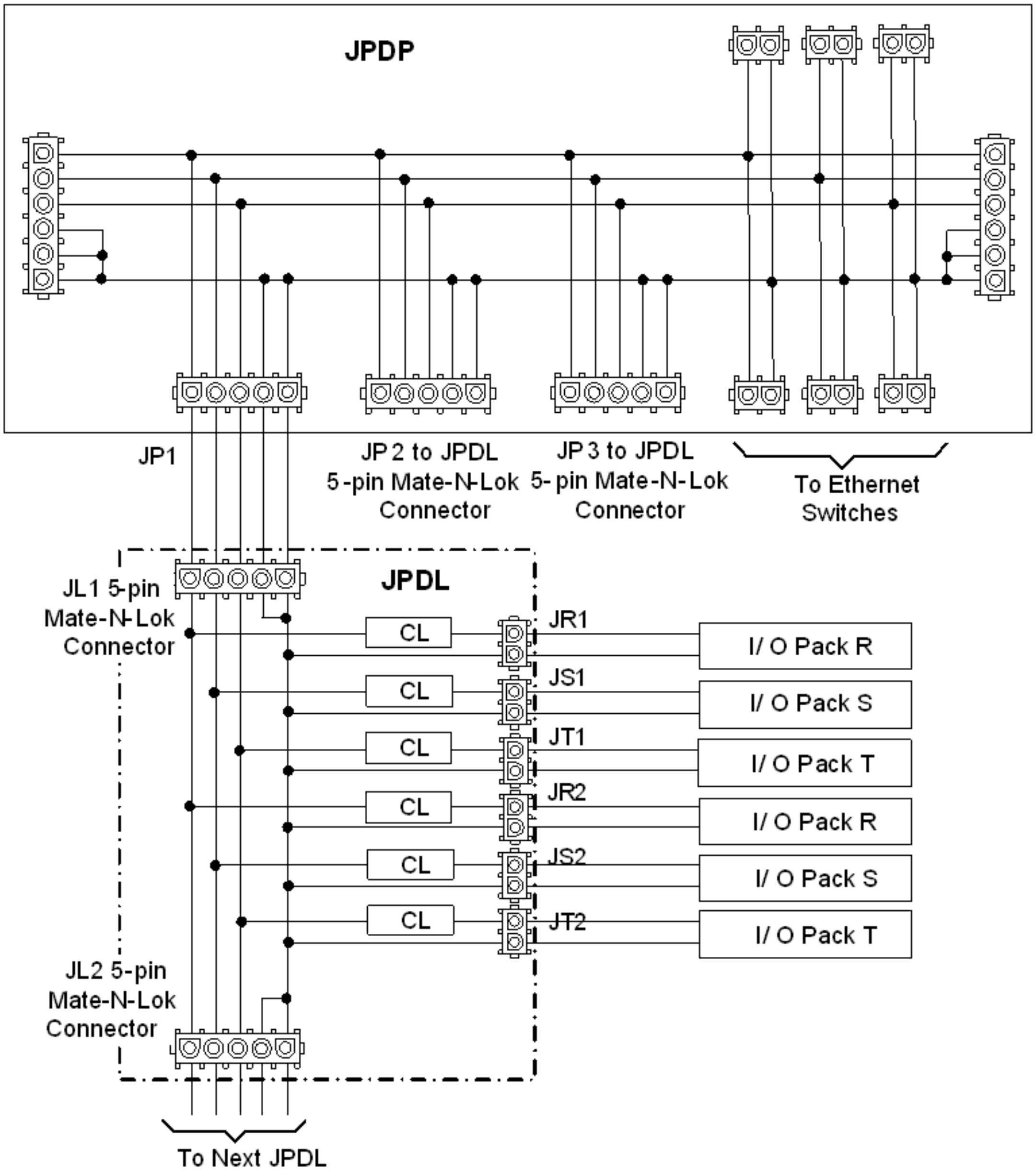
JPDP mounts in a plastic holder, which fits on a vertical DIN-rail next to other power distribution boards. Power input and output cables have Mate-N-Lok connectors. For cable destinations, refer to the circuit diagram.



JPDP Wiring and Cabling

18.15.3 Operation

The following figure explains how the 28 V dc power is distributed in JPDP, and how it reaches the I/O packs and the Ethernet switches.



JPDP Simplified Circuit Diagram with JPDL

18.15.3.1 Inputs

Input power is typically 28 V dc, received from the JPDS, JPDM, JPDC, or JPDG (referred to as Pbus). The 6-pin Mate-N-Lok input connector receives three separate Pbus feeds from JPDS for triple redundancy. The feeds are designated Red, Blue, and Black.

18.15.3.2 Outputs

Three identical output circuits provide power feeds to JPDL boards. Each JPDL output uses a 5-pin Mate-N-Lok connector. Three of the five pins are for Red, Blue, and Black. The other two pins are for Pbus return.

Six identical outputs are provided for Ethernet switches. Two connectors are dedicated to each of the three feeds (red, blue, and black).

18.15.4 Specifications

Item	JPDP Description	
Inputs	One 6-pin connection with three separate 28 V dc Pbus feeds	Red, Blue, Black, and Return
Outputs	Six 2-pin connections for Ethernet Switches	2 Red, 2 Blue, 2 Black
	Three 5-pin connections for JPDL boards, feeding I/O packs	Each one Red, Blue, Black, and Return
	One 6-pin connection with three separate 28 V dc Pbus feeds	Red, Blue, Black, and Return
Ambient Rating for Enclosure Design†	-40 to 70ºC (-40 to 158 ºF)	
Board Dimensions	15.875 cm high x 10.795 cm wide (6.25 in x 4.25 in)	
Mounting	DIN-rail, card carrier mounting Base mounted steel bracket, 4 holes	

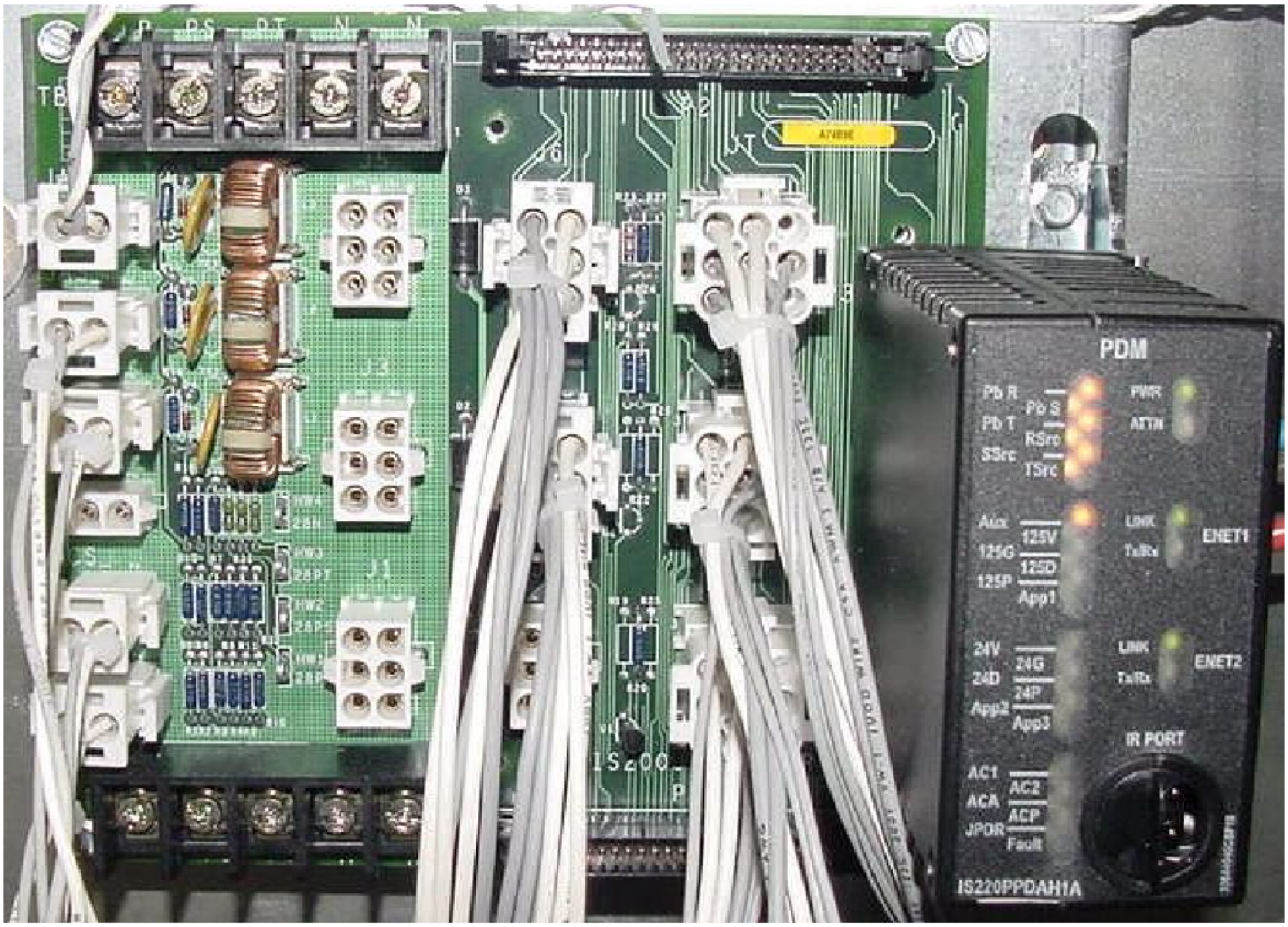
Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

18.16 JPDS Core 28 V DC Power Distribution

18.16.1 Functional Description

The JPDS power distribution board receives 28 V dc power from chosen supplies and distributes it to system controllers and branch circuit I/O pack power distribution boards. It has no fuses or switches and can maintain three separate power buses for R, S, and T controls, or optionally it can be jumpered to provide a single bus with redundant supplies. It is also possible to wire two adjacent JPDS boards together. JPDS integrates into the PDM system feedback offered through the PPDA I/O pack.

The JPDS power distribution board receives 28 V dc power from chosen supplies and distributes it to system controllers and branch circuit I/O pack power distribution boards. It is designed for Class I Division 2 applications, so it has no fuses or switches. It can maintain three separate power buses for R, S, and T controls, or optionally it can be jumpered to provide a single bus with redundant supplies. It is also possible to wire two adjacent JPDS boards together.



JPDS with PPDA I/O Pack In Use

18.16.1.1 Compatibility

The IS200JPDS board is compatible with the feedback signal P1/P2 connectors on JPDB, JPDF, and JPDE leading to a PPDA I/O pack. The DC-62 connector on JPDS is compatible with the IS220PPDA I/O pack.

18.16.2 JPDS I/O Characteristics

- Three power supply inputs are provided on JR, JS, and JT. The connector uses pins 8 and 9 for positive 28 V power. Pins 1-3 are used for 28 return, providing 24 A steady state capacity. These connectors include low level signals capable of detecting status switches on each supply and generating a feedback signal to the PPDA. Pin 4 provides positive 10 V wetting to the switch, and the return is on pin 5. Pins 6 and 7 are not connected.
- Terminal boards TB1 and TB2 at the bottom and top of the board provide access to the three power buses. If two adjacent JPDS boards are used, jumpers may be placed between TB1 and TB2 on the boards to parallel the bus on the two boards. For a single power bus fed by redundant supplies, jumpers may be placed between PR, PS, and PT terminals to tie the positive bus terminals together.

Do not exceed the maximum available fault current out of the JPDS board when tying the positive bus terminals together. For applications requiring greater available fault current, the JPDM is a better choice.

Attention

- Three two-pin Mate-N-Lok connectors (JCR, JCS, and JCT) are provided to power the controllers or other loads. Pin 1 is 28 V, and pin 2 is the return.
- Three two-pin Mate-N-Lok connectors (JAR, JAS, and JAT) with filtering and fusing are provided for auxiliary loads. These outputs feature a series common mode filter inductor, and they have self-resetting polysilicon fuses rated for 1.6 A at 20 °C, derated to 0.8 A at 70 °C. Pin 1 is 28 V, and pin 2 is the return.
- Six Mate-N-Lok connectors with six pins each are provided to supply R, S, and T power to remote JPDP or JPDH boards, or directly to JPDL boards when used with the appropriate wire harness. On all six connectors, pins 1-3 are 28 V return, pin 4 is 28 R, pin 5 is 28 S, and pin 6 is 28 T.
- The DC62 connector JA1 is used for a PPDA power diagnostic I/O pack. It contains the status feedback signals for up to six core power distribution boards.
- P4 supplies power to the PPDA I/O pack. It is a power circuit formed from R, S, and T power using a diode-or arrangement followed by a polysilicon self-resetting fuse rated for the PPDA power requirements. This ensures that the I/O pack receives power if any of the three power buses are active.
- Diagnostic daisy chain 50 pin ribbon cable connectors P1 and P2 are located on top and bottom of the board. They are used for pass-through of the diagnostic signals.

18.16.2.1 Diagnostic Features

JPDS and JPDM have feedback wiring that is different from the other core PDM boards. One JPDS or JPDM will host the PPDA I/O pack on the JA1 connector. On that board, the P1 connector is not used because the output signals are sent to the PPDA. If a second JPDS or JPDM board is used, the P1 connector on the second board will be used to conduct its feedback into P2 of the board hosting PPDA. In either case, the P2 connector provides passage of feedback signals from other core PDM boards. The following signals are created by JPDS:

- An electronic ID identifies the board type, revision, and serial number.
- PS28vStat_R, _S, _T are three analog P28 voltage readings for R, S, and T bus. Separate analog feedback signals are used. Accuracy is specified to be ±1% of full scale and calculated accuracy is ±0.2% at 3 sigma.
- One dry contact from each of the three power supplies (DryCntStat_R, _S, _T) yields three Boolean values.
- Three Aux output fuse status signals (AuxFuseStat_R, _S, _T) multiplexed into a single analog value yields three Boolean values after PPDA decodes the signal.

JPDS provides the following four test point outputs for connection of external test equipment:

- HWI - 28PR
- HW2 - 28PS
- HW3 - 28PT
- HW4 - 28N

The positive side test points include series 10 kΩ current limiting resistors. These allow access to all three 28 V power buses and the common return circuit.

18.16.2.2 Grounding

Mark VIe control systems separate ground into a functional earth (FE) and a protective earth (PE). The PE is intended for power distribution functions such as JPDF, while functional earth is used for *quiet* uses such as the control electronics and their power as on JPDS.

The IS200JPDS board is grounded through the sheet metal bracket to the underlying back base. In most cases, this can be the system FE.

Grounding of the JPDS takes place through metal mounting standoffs fastened to the underlying sheet metal. The ground is used as a local reference when creating the magnitude feedback signals appearing on P2 and JA1. This is done because the JPDS is expected to be part of the FE system in a control and mounting on a FE potential back-base is normal practice.

Note This is different than JPDB, JPDE, and JPDF where a PE connection is desired.

18.16.2.3 Physical Arrangement

JPDS accepts power from cables and distributes it to the JR, JS, and JT connectors. JPDS, when hosting a PPDA I/O pack, is mounted so indicator lights on the pack are easily visible. Two JPDS boards, when used together, are mounted so that any terminal board connections are easily accessible. The location of JPDS is not critical in a panel. Connector P1 transmits feedback signals to a board hosting a PPDA I/O pack. Connector P2 receives feedback from other power distribution boards and passes the signals out of P1 to the PPDA. If a feedback cable connection from JPDS P2 to another power distribution board is planned, consideration should be given to the feedback cable routing.

JPDS is designed to accept power input from cables into the JR, JS, and JT connectors so it exhibits less mounting position sensitivity than some other boards. The mounting surface is expected to at functional earth potential. If the board hosts a PPDA I/O pack, consideration should be given to maintain the visibility of the indicator lights located on the top of the PPDA. If two boards are used together, arranging them next to each other will make any needed barrier terminal strip connections easier to use. The P1 and P2 ribbon cable headers on all of the JPDx boards are designed so the JPDS or JPDM holding the PPDA I/O pack is best located at the top of the arrangement. This allows ribbon cables to flow from one to the next, exiting the top and entering the bottom of the next until the PPDA host is reached.

18.16.3 JPDS Application Notes

The internal wiring permits either three independent 28 V dc power buses to be maintained, or all three combined into a single internal bus. Each bus is sized to handle 25 A. They share a common ground that is sized for 75 A. With three supplies, it is possible to operate R, S, and T controllers and their I/O from separate power supplies. Failure of a supply can take one controller and I/O but not affect the other two channels. There is a dedicated 28 V diode-OR power output for the PPDA I/O pack to avoid losing power system feedback if a channel power failure occurs.

A second method of operation has jumpers between the R, S, and T 28 V bus connection screws on TB1 and TB2. The board provides a single highly reliable source of 28 V. Up to three supplies could power this bus with parallel operation capability designed into the external supplies.

The screw terminals could also be used to parallel the power buses from two adjacent JPDS boards. Two boards offer the following features:

- Two sets of control rack output for Duplex or TMR applications using redundant supplies in the control racks, or systems where more than three supplies are to be paralleled
- Twelve JPDP outputs instead of six
- Separated R, S, and T power could now have two input power supplies providing supply redundancy on each bus.

In some applications, a battery bus can be applied as a power backup. A grounded battery system can also be used as input to this board using the screw terminals on the end of the board. This requires diodes not on JPDS to provide isolation between the battery and internal bus. During installation or repair, any configuration performed through the barrier terminal strips must match system documentation.

In TMR systems, it is generally desirable to maintain separate R, S, and T power systems throughout the control. When used this way, JPDS will have three power supply inputs. The barrier terminal at the top and bottom of the board will not be used to connect the three separate supplies. In dual systems, it is common to use dual redundant power supplies for 28 V power, and to connect the positive side of the P28 R, S, and possibly T buses using jumpers applied to one of the barrier terminal strips. It is also possible to use three supplies tied together into a single supply bus if desired.

Because JPDS does not have any output circuit fusing, it depends on the current limit of the power supplies to limit fault current on outputs. If two power supplies of 500 W or greater are used in a diode or configuration, there will be too much available fault current so the JPDM board with fusing must be used.

18.16.3.1 PPDA Configuration with JPDS

If one or two of the 28 V circuits are not powered, the undervoltage detection for that circuit can be disabled by changing the value of *PS28vEnable* from **Enable** to **Disable**. This also removes the alarm driven by the power supply dry contact monitor associated with that circuit.

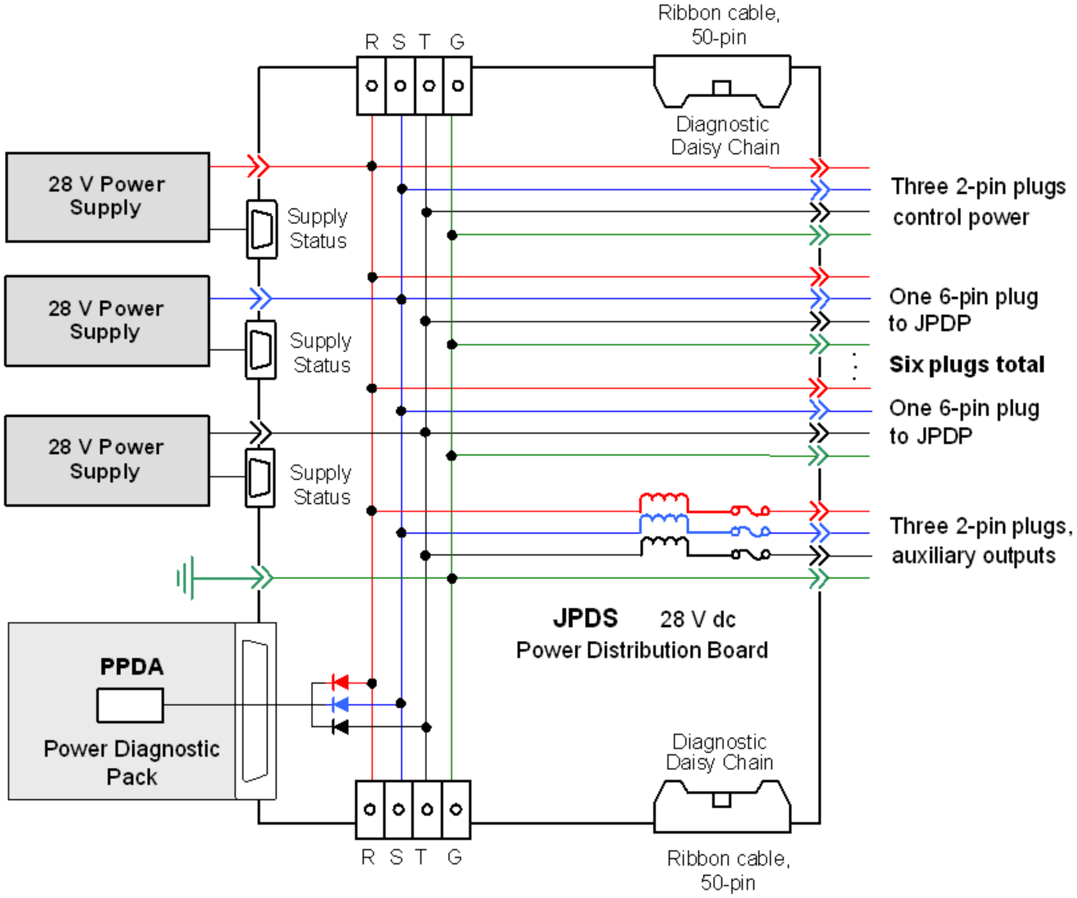
Note If the Dry Contact status feedback from the Power supply are not used, the *PS28vEnable* can be set to **NoDryCnt** to continue to allow the 28 V input to be used, but disable diagnostic alarms driven by the power supply dry contact monitor.

18.16.4 JPDS Installation

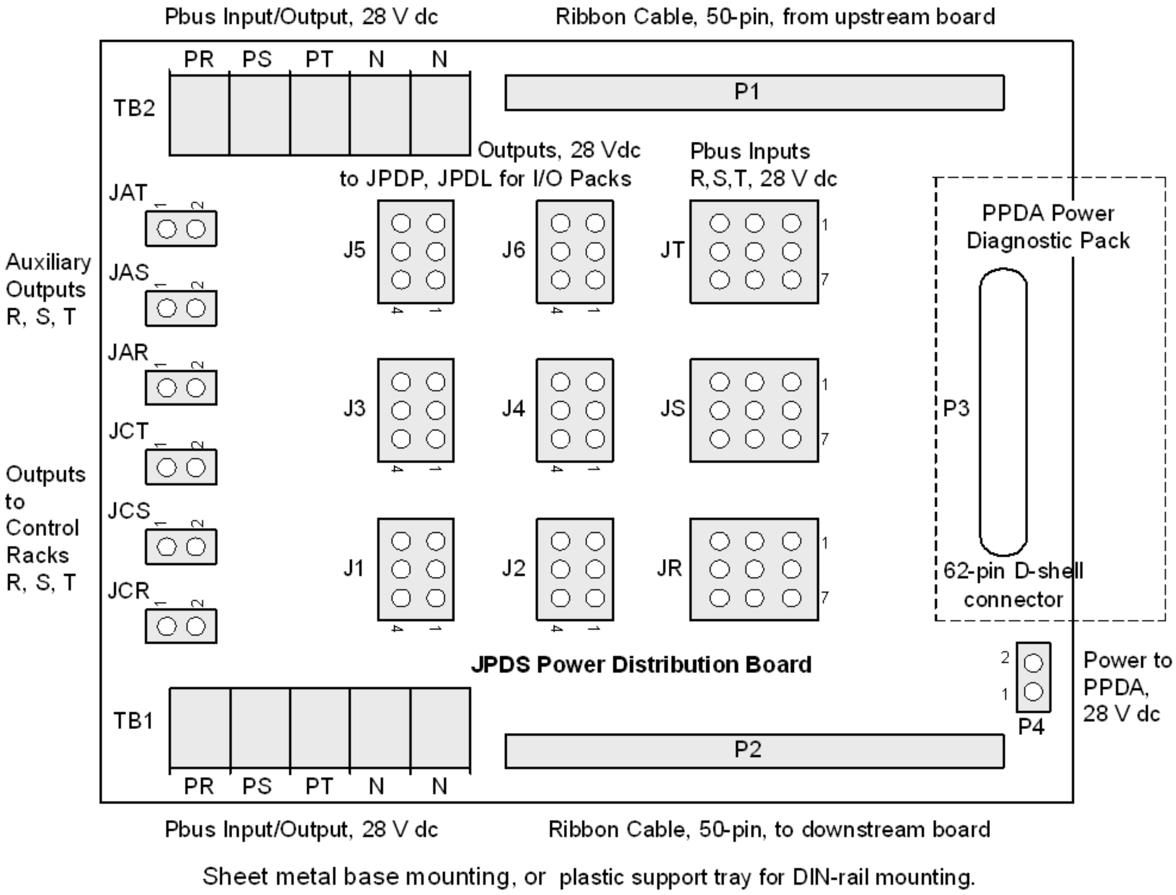
JPDS mounts in a metal holder, which fits on a vertical DIN-rail next to other power distribution boards. Optionally, JPDS is also available with a metal holder designed for direct mounting. Refer to the wiring diagrams for power input and output routing. There is a 50-pin diagnostic connector mounted on the top and bottom of the board.

18.16.5 JPDS Operation

The JPDS is the power distribution board that receives 28 V dc power from the selected supplies and distributes it to the JPDP boards (for power to the I/O packs) and to the control racks. The normal 28 V power input to JPDS is through JR, JS, JT connectors.



JPDS Simplified Circuit Diagram


Pbus Input/Output, 28 V dc
Ribbon Cable, 50-pin, from upstream board
PR
PS
PT
N
N
TB2
P1
Outputs, 28 Vdc to JPDP, JPDL for I/O Packs
Pbus Inputs R,S,T, 28 V dc
PPDA Power Diagnostic Pack
JAT
JAS
JAR
JCT
JCS
JCR
Auxiliary Outputs R, S, T
Outputs to Control Racks R, S, T
J5
J6
JT
J3
J4
JS
J1
J2
JR
1
7
4
P3
62-pin D-shell connector
JPDS Power Distribution Board
Power to PPDA, 28 V dc
P4
TB1
P2
Pbus Input/Output, 28 V dc
Ribbon Cable, 50-pin, to downstream board
Sheet metal base mounting, or plastic support tray for DIN-rail mounting.

JPDS Mechanical Board Layout

The JPDS I/O characteristics are as follows:

- Three 28 V power input connectors, JR, JS, JT. The connectors on the power supplies have two connections for positive and three connections for negative power. In addition, there are three power supply health inputs each with two dry contact inputs per power source, which become diagnostic signals.
- Three dc outputs, JCR, JCS, and JCT, to control rack CPCI power supplies
- Six outputs to JPDP cards through six-pin connectors J1, J2, J3, J4, J5, J6 (3x2 Mate-N-Lok). This is the same connector with the same pin assignments used on JPDP. It is possible to directly connect up to six JPDL boards to JPDS to supply the I/O packs.
- Three outputs JAR, JAS, JAT, to auxiliary power connectors, each with a positive temperature coefficient fuse for current limiting and containing a common-mode choke for noise suppression
- Access to the internal 28 V bus at the board top and bottom using individual screw terminals on TB1 and TB2. Screw terminals for R, S, and T are sized to handle a maximum of 35 A continuous current. These terminals can be used to jumper boards together The screw terminal for ground is sized for 75 A.
- DC-62 connector for PPDA power diagnostic I/O pack. The PPDA monitors JPDS and up to five additional power distribution boards connected to JPDS with a 50-pin diagnostic ribbon cable.
- P28 power output, P4, diode ORed for the PPDA power diagnostic pack

18.16.6 Specifications

Item	JPDS Specification	
Inputs	Three 9-pin connections for 28 V dc Power Supply inputs	25 A max each
	One 50-pin ribbon cable with diagnostic data from upstream boards	±5 V max
	One 5-screw terminal block for daisy chaining power distribution boards	35 A max per screw
Outputs	Six 6-pin connections for either JPDP or JPDL boards	13 A max per pin
	Three 2-pin connections for CPCI control rack power	12.5 A max per pin
	Three 2-pin connections, filtered and fused, for auxiliary devices	1.6 A at 20 °C (derated to 0.8 A at 70 °C) positive temperature coefficient fuse
	One 50-pin ribbon cable with diagnostic data to downstream boards	±5 V max
	One 5-screw terminal block for daisy chaining power distribution boards	35 A max per screw
	One 2-pin connection for 28 V dc power to the PPDA pack	0.25 A max
	One 62-pin D-shell connection for PPDA power diagnostic pack	±5 V max
Ambient Rating for Enclosure Design†	-40 to 70ºC (-40 to 158 ºF)	
Board Dimensions	16.51 cm high x 17.8 cm wide (6.5 in x 7.0 in)	
Mounting	DIN-rail mounting Base mounted steel bracket	

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

18.16.7 Diagnostics

Diagnostic signals are obtained and routed into the PPDA I/O pack as follows:

- An electronic ID identifying the board type, revision, and serial number
- Three analog P28 voltage readings for R, S, and T bus
- Each power supply connector (JR1, JS1, JT1) has provisions for a dry contact indicating power supply status. JPDS conditions these signals and places them in the feedback signal set.
- Auxiliary Supply status feedback from downstream of the fuses provides three feedback signals to PPDA.

JPDS contains test rings for 28 V dc power from the three internal circuits, 28PR, 28PS, and 28PT. Each test ring has a series 10k resistor isolating the ring and a single grounded ring, 28N, for the return path. These can be used to measure the 28 V dc power voltage using external test equipment.

Note Fuse and dry contacts failure diagnostics will not be generated if *InputDiagEnab* on the respective dc input (R/S/T) is set to Disable or the dc input is below the low limit threshold, 5 V.

Also, dry contact diagnostics will not be generated if the user selects *NoDryCnt* on the input on which a dry contact exists.

18.17 JGND Shield Ground

18.17.1 Functional Description

The Shield Ground (JGND) terminal board mounts along side the terminal board and provides convenient ground connections for the customer’s shield drain wires.

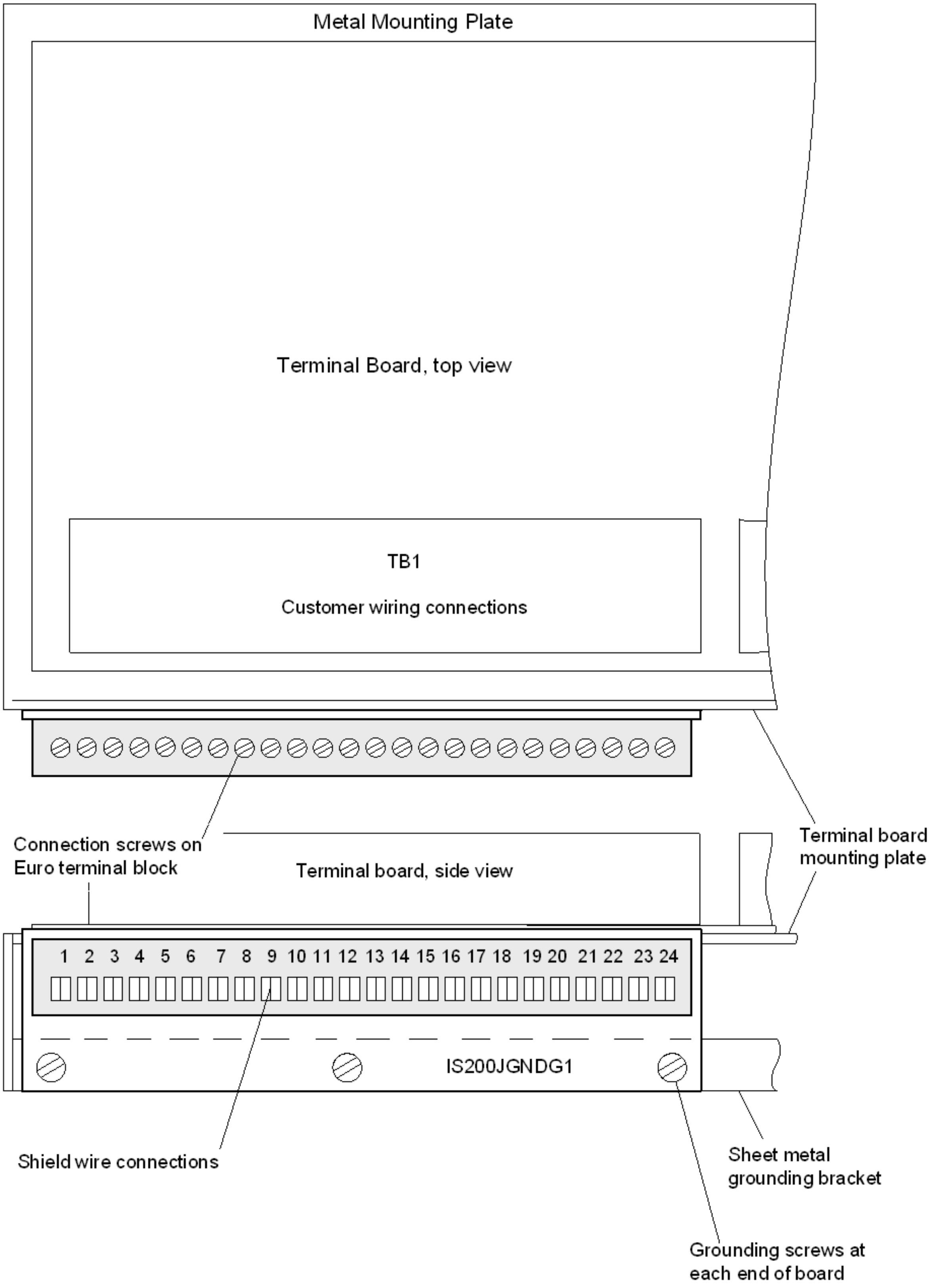
18.17.2 Installation

JGND mounts on a sheet metal bracket attached to the plate, which holds the terminal board. JGND is grounded to the bracket with the two screws at each end of the terminal board. The customer's shield wires connect to terminals in the Euro-type terminal block.

One or two JGND can be located on the side of the terminal board mounting bracket, for a maximum of 48 ground connections.

JGND provides a path to sheet metal ground at the board mounting screw locations. The default mechanical assembly of this board to its mount includes a nylon washer between the board and the sheet metal. This isolates JGND from the sheet metal and allows wiring of the board ground current into any desired grounding location. Removal of the washer permits conduction of the ground currents into local sheet metal and does not require any additional grounding leads.

At the time a JGND board is installed, a choice must be made to conduct ground currents through a wire to designated ground (washer present) or to conduct directly to sheet metal (washer absent). A direct connection to sheet metal is preferred. If a wire connection is used, it should be as short as possible, not exceeding 5 cm (2 in).


Metal Mounting Plate
Terminal Board, top view
TB1
Customer wiring connections
Connection screws on Euro terminal block
Terminal board, side view
Terminal board mounting plate
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
IS200JGNDG1
Shield wire connections
Sheet metal grounding bracket
Grounding screws at each end of board

JGND Mounting

18.17.3 Operation

All 24 connectors on the Euro block are connected to ground through the two grounding screws at the ends of JGND. These make contact with the metal mounting bracket, which is connected to ground. If nylon washers are used to isolate the board, ground currents must be wired into an alternate system location.

18.17.4 Specifications

Item	JGND Description
Terminals	24 terminals on Euro type terminal block
Ambient Rating for Enclosure Design†	-40 to 70ºC (-40 to 158 ºF)
Board Dimensions	3.175 cm high x 12.7 cm wide (1.25 in x 5.0 in)
Mounting	Held with three screws to sheet metal bracket on side of terminal board

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

18.18 Vendor Manufactured Control Power Supplies

A group of power supplies (VMCPS) are in place to support the Mark VIe control. All of these supplies share these features:

- Convection cooling only. No fans are used.
- The supplies are designed to operate in -30 to 65º C ambient temperatures except where noted.
- All 28 V output supplies are designed for ±2% voltage regulation for compatibility with terminal boards that require ±5%.
- Designs are compatible with all vibration and contamination environments identified for the Mark VIe control.
- All bulk supplies include a normally open dry contact for status feedback. When the supply is working correctly, the contact is closed. When a problem is detected, the contact is open.
- A current limit function is included in the output that limits current to a defined level. The current limit is rectangular rather than being a fold-back limit. The current limits at the defined value and output voltage is decreased.
- Supplies include filtering on the input that should prevent sensitivity to input interference, and the supplies should not inject unacceptable noise into the source.
- Supplies are CE marked.

The Mark VIe and Mark VIeS control systems have several options for vendor manufactured control power supplies (VMCPS).

VMCPS

Power Supply	Control Power	Available Ratings	Manufacturer
AC or DC input / DC output	Input: 115/230 V ac (auto switch), 90-350 V dc or 120-350 V dc (model dependent) Output: 24, 28, or 48 V dc	120 to 960 W	Phoenix Contact
AC input / DC output	Input: 115/230 V ac (selectable) Output: 24, 28, or 48 V dc	150 to 600 W	TRACO® Power
DC input / DC output	Input: 24 or 125 V dc Output: 28 V dc	150 to 500 W	ACROPower™

The following features are common to all of the vendor manufactured control power supplies:

- Convection cooling – no cooling fans used
- Ambient rating for enclosure design: -30 to 65°C (-13 to 149° F) free convection (no fans), Refer to GEH-6721_Vol_I, the chapter *Technical Regulations, Standards, and Environments*.
- ±2% voltage regulation
- Compatible with Mark VIe and Mark VIeS environmental and agency standards
- Normally open dry contact and LEDs for status feedback
- Power supply outputs can be paralleled (ACROPower and TRACO support direct connection and current sharing. Phoenix does not current share but supports redundant operation using an external diode OR module.)
- Current limit and over-voltage protection of outputs
- Input filtering for EMC compliance for incoming and out-going conducted EMI
- CE Mark for Low Voltage Directive and EMC
- UL 508 listing

18.18.1 Phoenix Power Supplies

The following table provides the features that are specific to the Phoenix power supplies.

Phoenix Power Control Power Supplies, GE Cat# 342A3647x

Item #	‡GE Part #	Output Rated W (≤60°C, 140 °F)	Out-put V dc	Boost Output (<40°C, 104 °F) A dc	Rated Output (<60°C, 140 °F) A dc	Output (65°C, 149 °F) A dc	Out-put Clamp V	Out-put Clamp A	†HazLoc Cert: UL 1604 CL 1 Div 2	Input Inrush Cur-rent A	Input Surge (I^2T at 25°C, 77 °F) A^2s	Hold Up Time mS 120/23-0 V
1	342A3647 P120W24	120	24	7.5	5	4.4	35	7.5	Yes	20	2.5	20/120
2	342A3647 P120W28	120	28	6.3	4.2	3.7	35	7.5	Yes	20	2.5	20/120
3	342A3647 P240W24	240	24	15	10	8.8	35	15	Yes	15	1.5	50/>50
4	342A3647 P240W28	240	28	12.8	8.5	7.4	35	15	Yes	15	1.5	50/>50
5	342A3647 P240W48	240	48	7.5	5	4.4	63	7.5	No	15	1	50/>50
6	342A3647 P480W24	480	24	26	20	17.5	35	26	Yes	15	3.2	30/50
7	342A3647 P480W28	480	28	22.1	17	14.9	35	26	Yes	15	3.2	30/50
8	342A3647 P480W48	480	48	13	10	8.8	60	13	No	15	3.2	30/>30
9	342A3647 P960W24	960	24	45	40	35	32	45	Yes	15	3.2	20/>20
10	342A3647 P960W28	960	28	38.3	34	30	32	45	Yes	15	3.2	20/>20
11	342A3647 P960W48	960	48	22.5	20	17.5	60	27.5	No	15	3.2	20/>20
12	342A3647 PD48A40	N/A	48	–	–	40	60	***	No	N/A	N/A	N/A

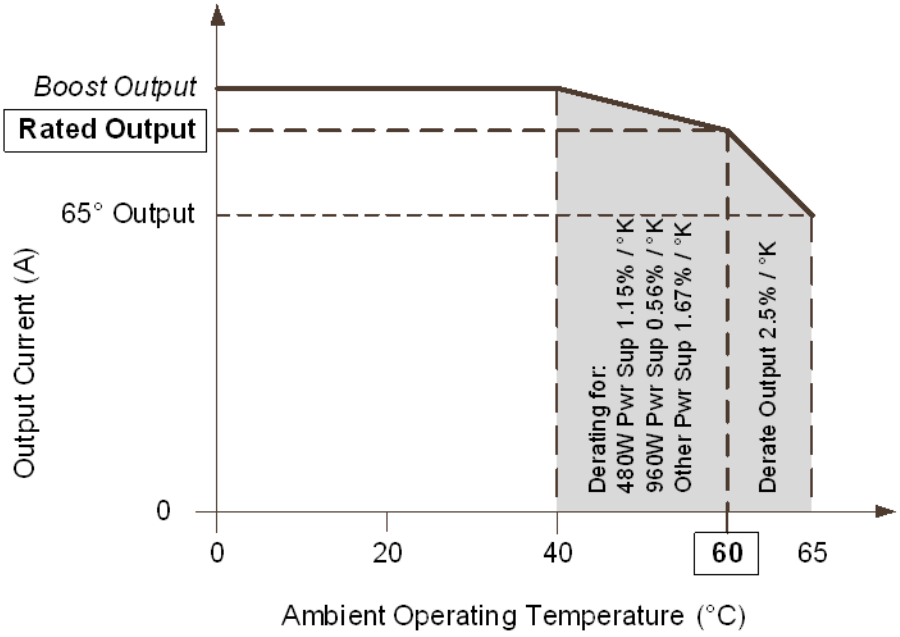
† Class 1 Div 2 HazLoc: UL 1604 is superseded by ISA 12.12.01-2000 as of 7/31/2012. Items 1,2,3,4,6,7,9,10 maintain the older UL 1604 certification. ATEX HazLoc: Items 1-12 are not ATEX certified.

‡ This part is a Diode-OR module for redundant connection of two power supplies. Each of the two inputs are rated for 48 V dc and 20 A dc continuous. The output continuous rating is 40 A dc.

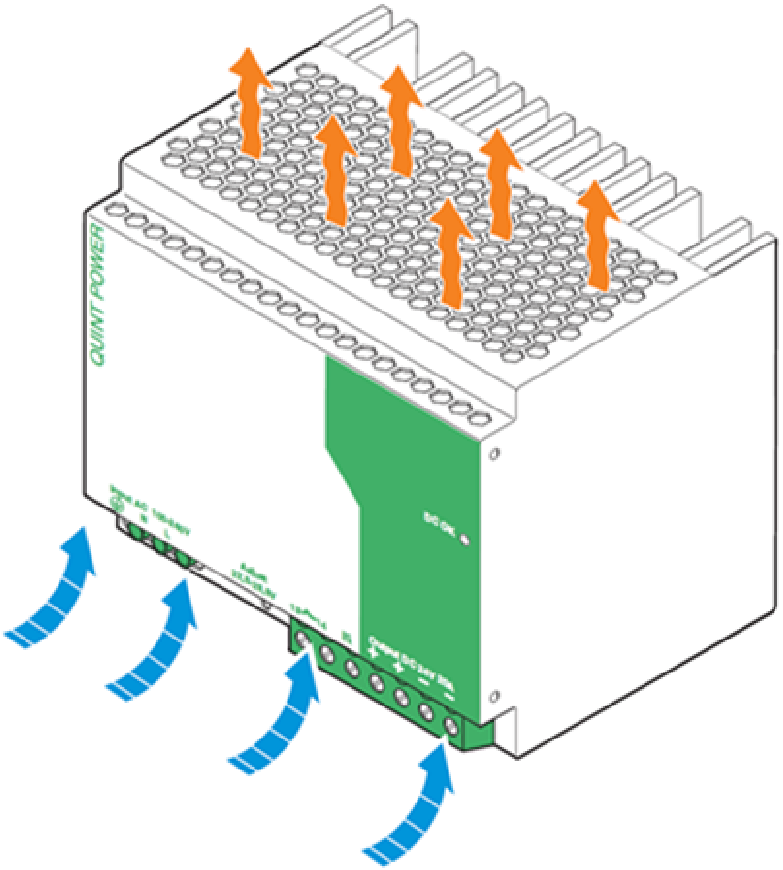
At an ambient operating temperature of up to 40°C (104 °F), the unit continuously supplies *Boost* output current. The unit can supply rated output current up to an ambient operating temperature of 60°C (140 °F). The output power must be decreased by 2.5% per Kelvin temperature increase for ambient operating temperatures from 60°C (140 °F) to 65°C (149 °F). At ambient operating temperatures above 70°C (158 °F) or in the event of a thermal overload, the unit does not switch off. The output power is decreased to such an extent that unit protection is provided. Once the unit has cooled down, the output power is increased again.

Attention

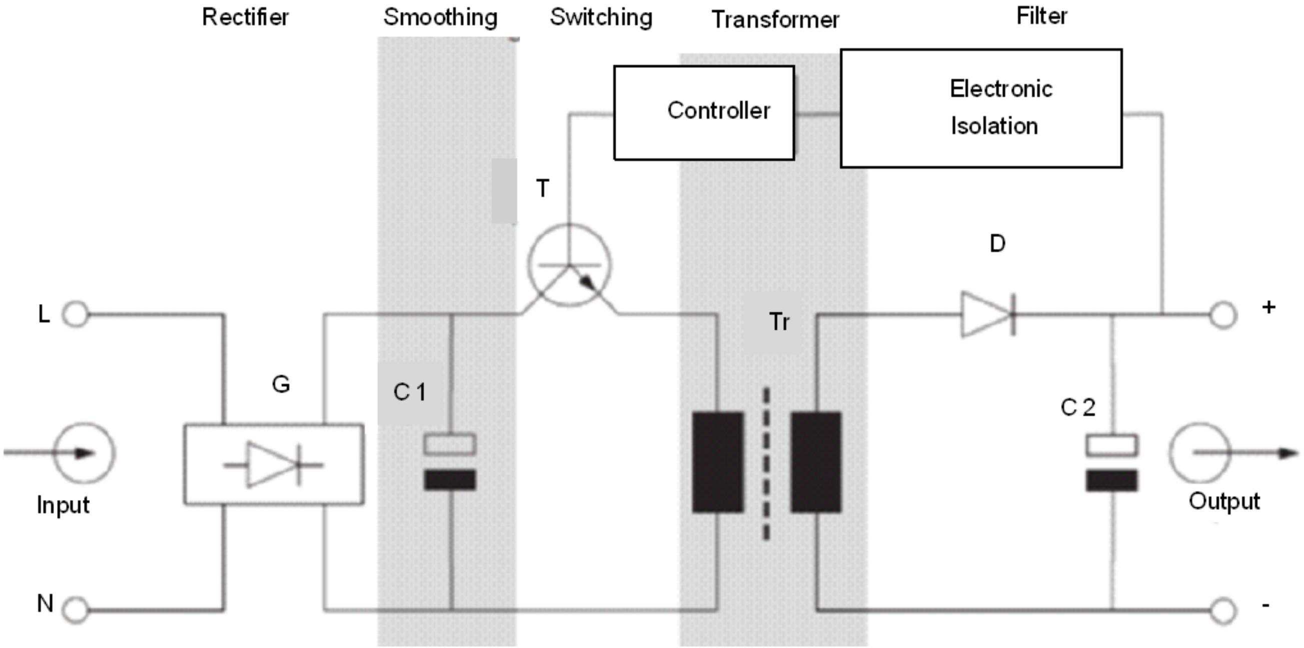
The 960 W power supplies are not suited for use in 125 V dc battery systems. The minimum input voltage for the 960 W power supplies is 120 V dc.



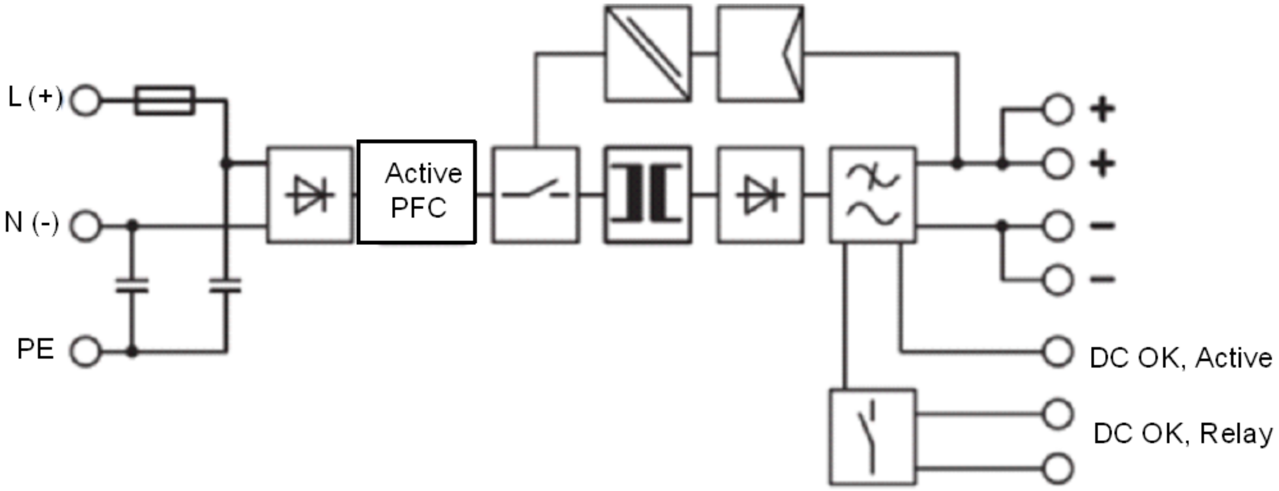
Boost and Output Derating



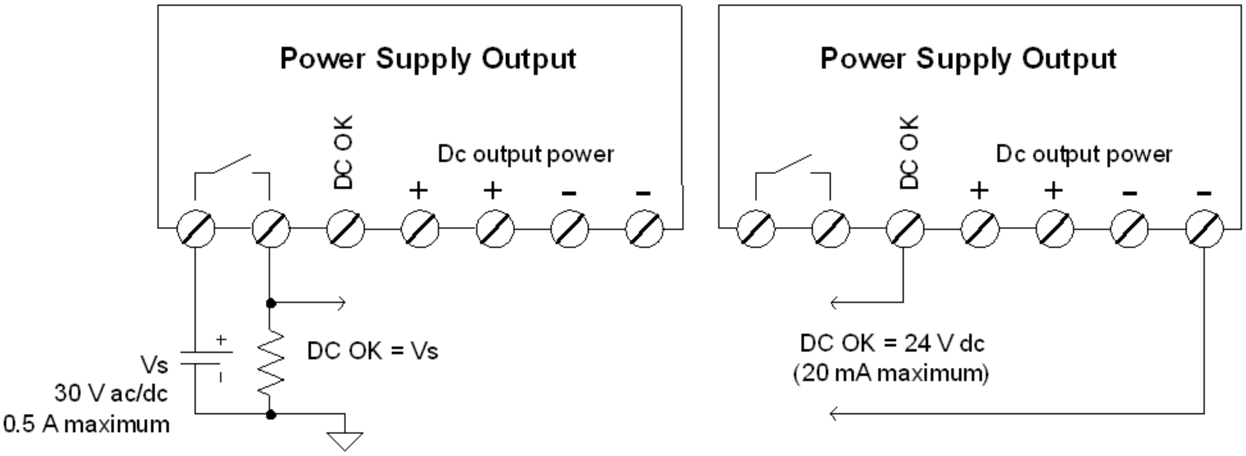
Convection Cooling and Mounting Orientation



Power Supply Topology



Power Supply Block Diagram



DC OK Threshold	*24 V supplies Vout > 22 V* *28 V supplies Vout > 22 V* *48 V supplies Vout > 44 V*

Diagnostic Output

18.18.1.1 Specifications

Inputs

Input Data	Phoenix Specification
Input Voltage Range	960 W power supplies: 85-264 V ac (auto switch) or 120-350 V dc All other power supplies: 85-264 V ac (auto switch) or 90-350 V dc
Input Frequency for AC Operation	45-65 Hz
Over-current Input Protection	Internal slow-blow fuse; activates during non-recoverable power supply failure Fuse is not user-replaceable
Over-voltage Protection	Varistor

Attention

The 960 W power supplies are not suited for use in 125 V dc battery systems. The minimum input voltage for the 960 W power supplies is 120 V dc.

Outputs

Output Data	Phoenix Specification
Derating	Refer to the curve in the figure, *Boost and Output Derating*.
Voltage Adjustment	Externally accessible potentiometer
Switching Frequency	Variable with load – resonant switching
Ripple and Noise (20 MHz Bandwidth)	< 100 mV peak-to-peak (pp)
Turn on Delay After Applying Input Power	1 s maximum
Min Load	None
Parallel Operation, Current Sharing	No capability
Parallel Operation, Redundancy	Redundant with external Diode-OR module

Reliability

Item	Specification
Mean-time-between-failure (MTBF)	> 500,000 h according to IEC 61709 (SN 29500)

Mounting

Item	Phoenix Specification
Mounting Position	On horizontal NS 35 DIN-rail mounted according to EN 60715
Mounting Location	***Attention*** **It is very important that each supply is mounted in a location with adequate space for free convective airflow and away from other heat sources.**
Recommended Clearance Around Power Supply for Full Power Output	25 mm (1 in) on either side, 127 mm (5 in) above and 76 mm (3 in) below
Vertical Stacking of Power Supplies Operating at Full Power	Not recommended. The convection cooling path is through the bottom and out the top. The difference between inlet and exhaust air can be as high as 28°C (82 °F) at full power.

Environment

Item	Phoenix Specification
Storage Temperature (non-operating)	-40 to 85°C (-40 to 185 °F)
Humidity (non-condensing)	5 to 95%
Environmental Compatibility	Pollution Degree 2 according to EN 50178 Climatic Class 3K3 according to EN 60721
Housing	AluNox (AlMg1), closed
Degree of Protection	IEC 60529 IP20

Vibration and Shock

Item	Specification
Seismic Universal Building Code (UBC)	Not applicable at the power supply (component) level
Vibration	< 15 Hz, amplitude ±2.5 mm, 15 Hz - 150 Hz, 2.3g, 90 minutes per IEC 60068-2-27
Shock	30g in all space directions, per IEC 60068-2-27

Standards and Electrical Safety

Item	Specification
CE - Low Voltage Directive	EN 61010-1
Electrical Safety of Industrial Equipment	UL/C-UL Listed UL 508 EN 50 178 (VDE 0160)
Electrical Safety of IT Equipment	EN 60950/VDE 0805, UL/C-UL Recognized UL 60950
Input Output Insulation Voltage	Input to Output: 4 kV ac (type test)/2 kV ac (routine test) Input to PE: 3.5 kV ac (type test)/1.5 kV ac (routine test) Output to PE: 500 V dc (routine test)

Standards and Electromagnetic Compatibility (EMC)

Item	Specification
Emissions Standards	
EN 55011	Radiated E-field emissions, 30 - 1000 MHz
EN 55011	Conducted emissions, 150 kHz - 30 MHz, applicable to ac power mains
Immunity Standards	
EN 61000-6-2	Generic immunity standard for industrial locations
IEC 61000-4-2	Electrostatic discharge (ESD) immunity
IEC 61000-4-3	Electromagnetic HF field immunity
IEC 61000-4-4	Electrical fast transient/burst immunity
IEC 61000-4-5	Surge immunity
IEC 61000-4-6	Conducted RF immunity
IEC 61000-4-11	Voltage dips and interruptions immunity

Diagnostics

Dc Output OK	Function
Green LED[1]	LED on when output OK Flashes or off when output not OK[3]
DC OK Output, Active Signal, Single-ended	High when output OK Signal level 24 V dc, 20 mA Refer to the figure, *Diagnostic Output*.
DC OK Output, Isolated Relay Contact[2]	Closed when output OK Isolated contact Contact rating 30 V ac/dc 0.5 A maximum With heavy inductive loads, a free-wheeling diode is required.
DC OK Threshold	24 V supplies: V_{out} >22 V 28 V supplies: V_{out} >22 V 48 V supplies: V_{out} >44 V
[1] No LED for input voltage [2] Relay is not Form C single NO contact only [3] No LED for overcurrent and overtemperature	

18.18.1.2 Safety Procedures

Warning

The device contains dangerous live elements and high levels of stored energy. Never carry out work when power is applied.

Warning

Risk of burns. The housing temperature can reach high values depending on the ambient temperature and the load of the device.

Attention

Make sure that all output cables are the correct size for the maximum output current or have separate fuse protection. The cable cross sections in the secondary circuit must be large enough to keep the voltage drops on the cables as low as possible. Further recommendations are given with the individual power supply descriptions provided in this document.

Before startup, please verify that the following conditions have been met:

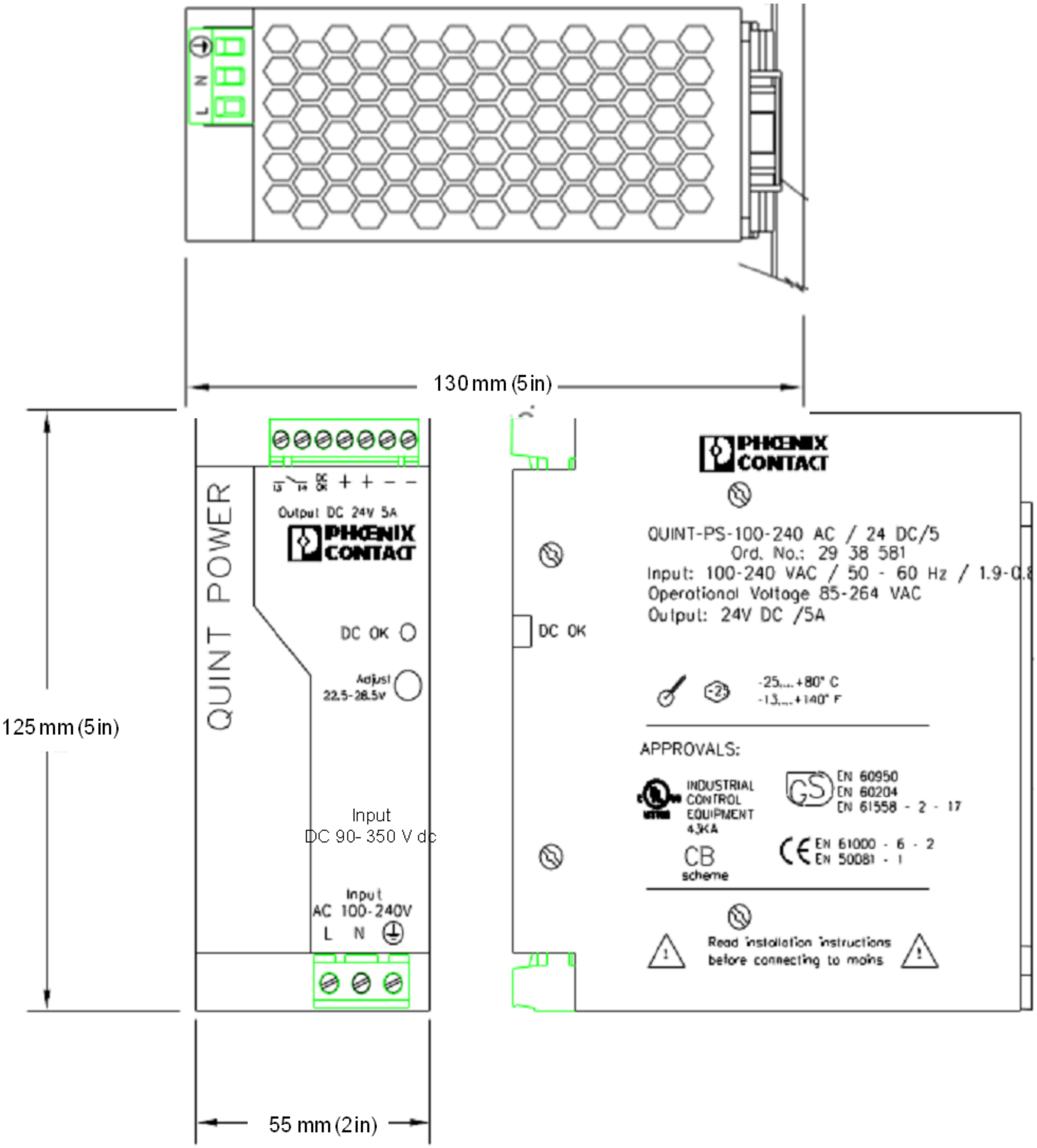
- The Mains has been connected correctly and protection is provided against electric shock.
- The device can be switched off outside the power supply according to EN 60950 regulations (such as by the line protection on the primary side).
- The protective conductor is connected.
- All supply lines have sufficient fuse protection and are the correct size.
- All output cables are the correct size for the maximum device output current or have separate fuse protection.
- Sufficient convection is ensured.

Attention

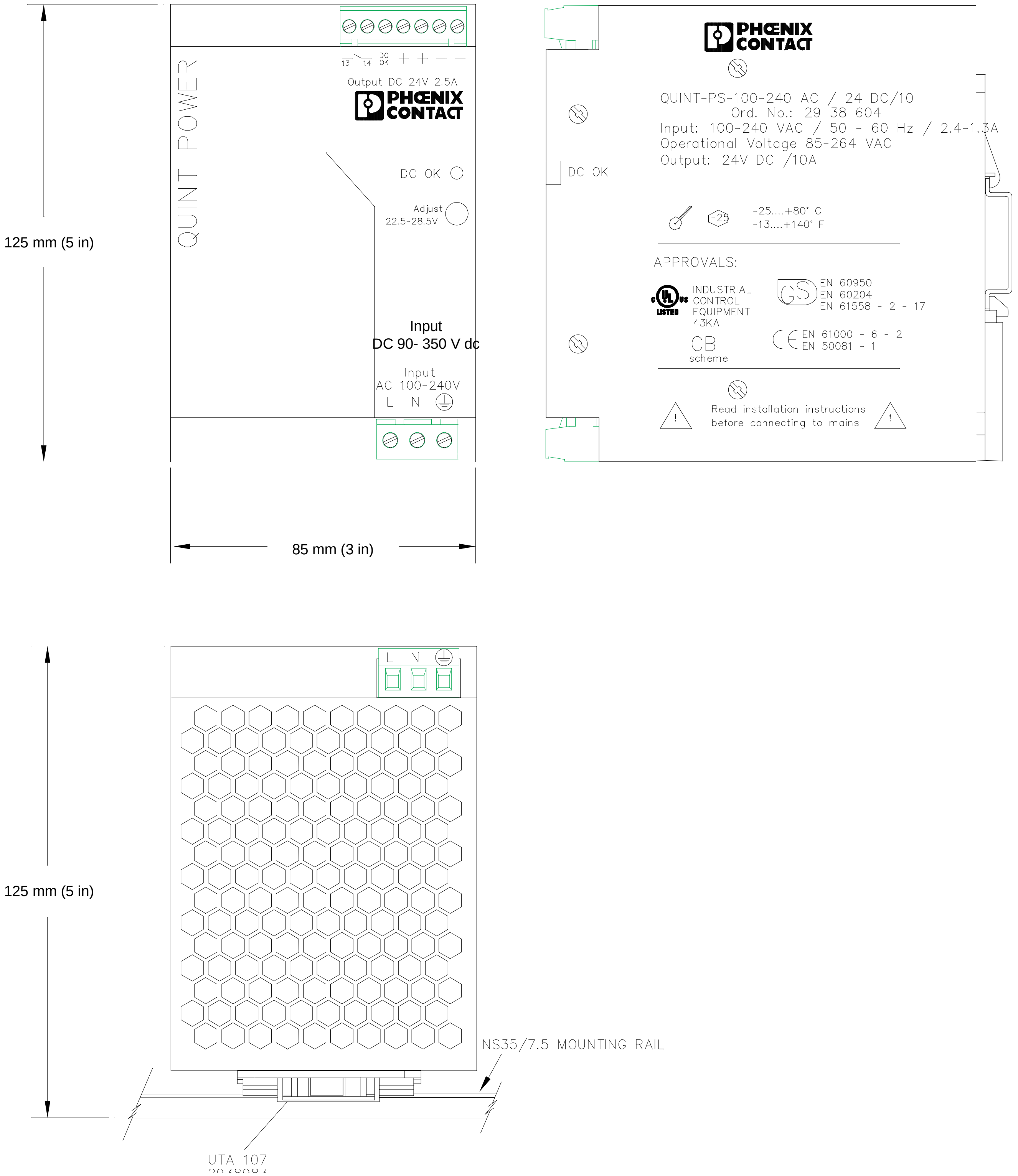
An internal fuse is provided for device protection. Branch circuit protection external to the supply is recommended to guard wiring and connections. For dc input applications, the external fuse or circuit breaker must be rated for dc operation. Further recommendations are given with individual supply descriptions provided in the following sections of this document.

If the internal fuse is blown, this is most probably due to component failures in the power supply. In this case, the power supply should be checked in the factory.

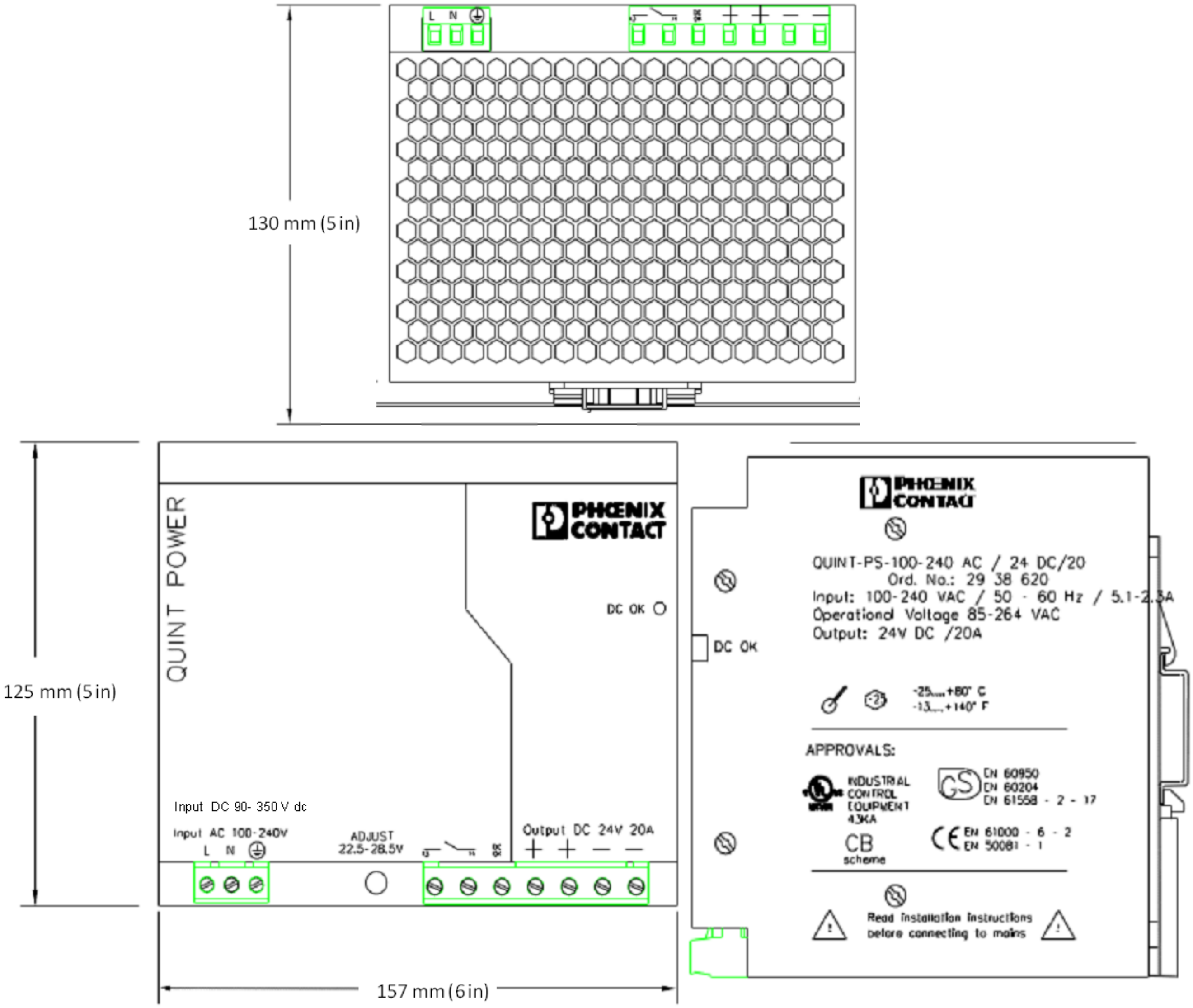
18.18.1.3 Phoenix Power Supply Dimensions



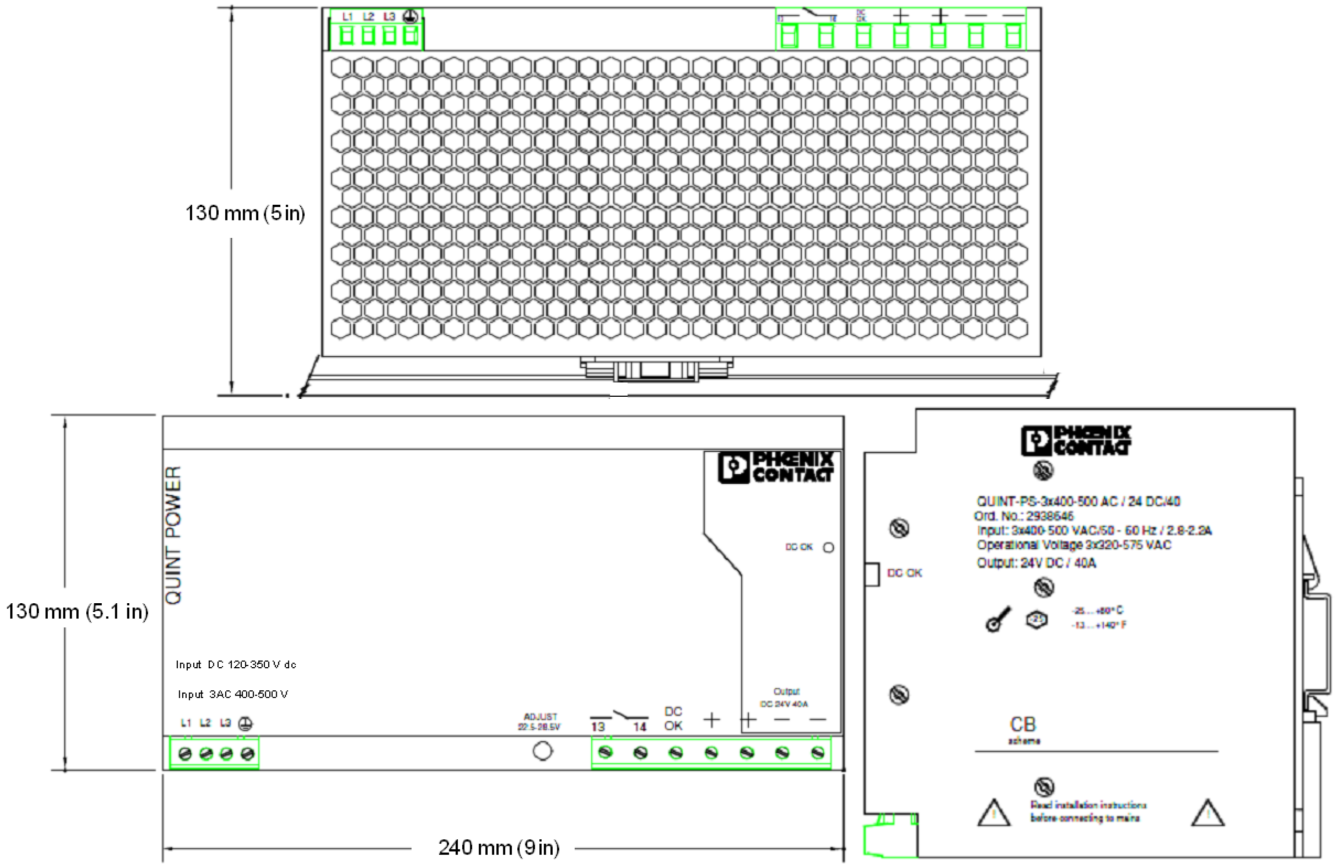
120 W Power Supply I/O and Dimensions



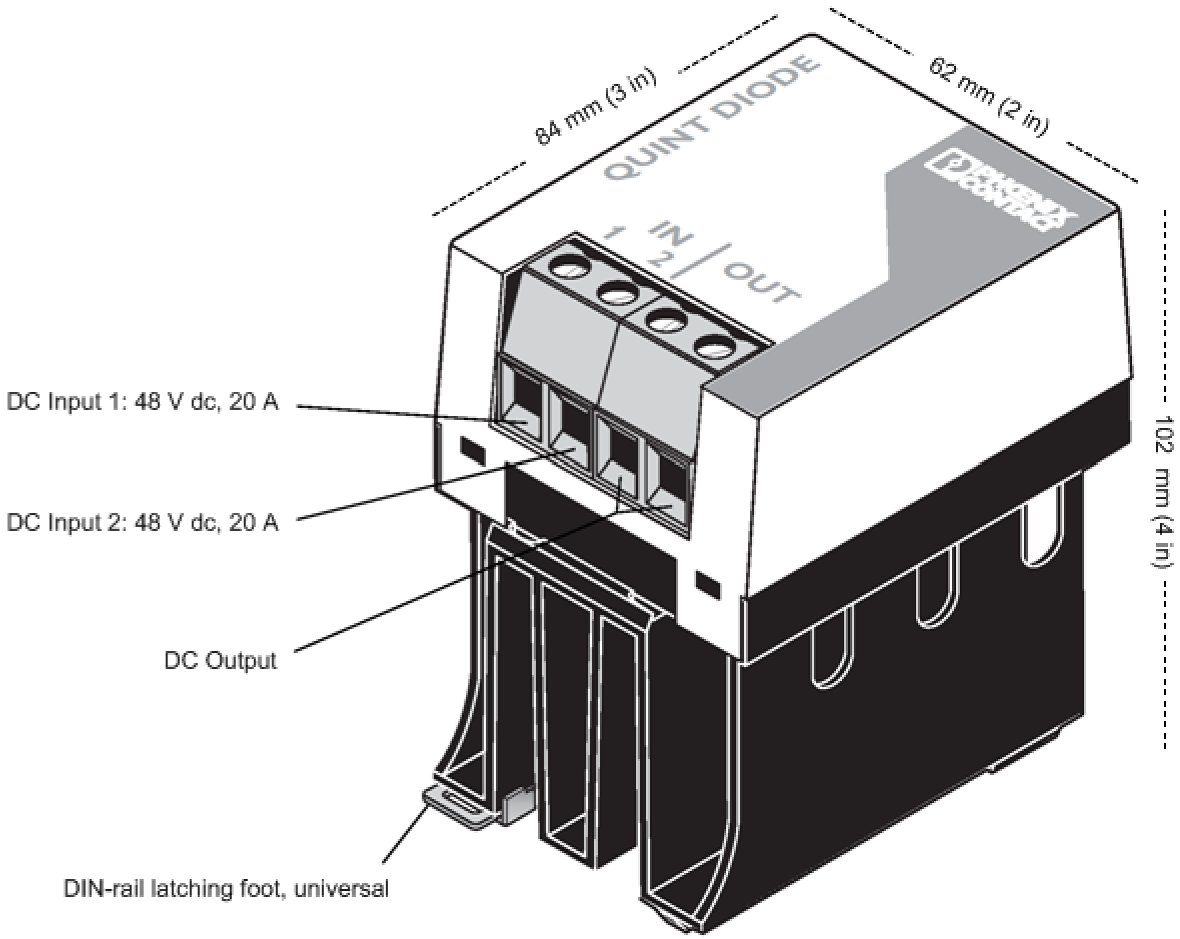
240 W Power Supply I/O and Dimensions



480 W Power Supply I/O and Dimensions



960 W Power Supply I/O and Dimensions


84 mm (3 in)
62 mm (2 in)
102 mm (4 in)
QUINT DIODE
PHOENIX CONTACT
IN
1
2
OUT
DC Input 1: 48 V dc, 20 A
DC Input 2: 48 V dc, 20 A
DC Output
DIN-rail latching foot, universal

342A3647PD40A48, Diode-OR Redundancy Module Power Supply I/O and Dimensions

18.18.1.4 Connecting Cable Wire Sizes

Caution

Input power must be removed before changing I/O connections.

Use a screwdriver with the correct blade width for wiring. Refer to the following table for cable cross sections. For reliable and safe-to-touch connections, strip the cable ends in accordance with the table.

Power Supplies Cable Wire Sizes Summary

Power Supply	I/O Group	Wire AWG (maximum)	Wire Stripping Length	Screw Torque
120 and 240 W	Input	14	7 mm (0.3 in)	0.5 - 0.6 Nm (4.4 - 5.3 in-lb)
	Output	14	7 mm (0.3 in)	0.5 - 0.6 Nm (4.4 - 5.3 in-lb)
	Signal	14	7 mm (0.3 in)	0.5 - 0.6 Nm (4.4 - 5.3 in-lb)
480 W	Input	10	7 mm (0.3 in)	0.5 - 0.6 Nm (4.4 - 5.3 in-lb)
	Output	6	10 mm (0.4 in)	1.2 - 1.5 Nm (10.6 - 13.3 in-lb)
	Signal	6	10 mm (0.4 in)	1.2 - 1.5 Nm (10.6 - 13.3 in-lb)
960 W	Input	10	8 mm (0.31 in)	0.5 - 0.6 Nm (4.4 - 5.3 in-lb)
	Output	6	10 mm (0.4 in)	1.2 - 1.5 Nm (10.6 - 13.3 in-lb)
	Signal	10	8 mm (0.31 in)	0.5 - 0.6 Nm (4.4 - 5.3 in-lb)

342A3647PD40A48, Diode-OR Module Cable Cross Sections

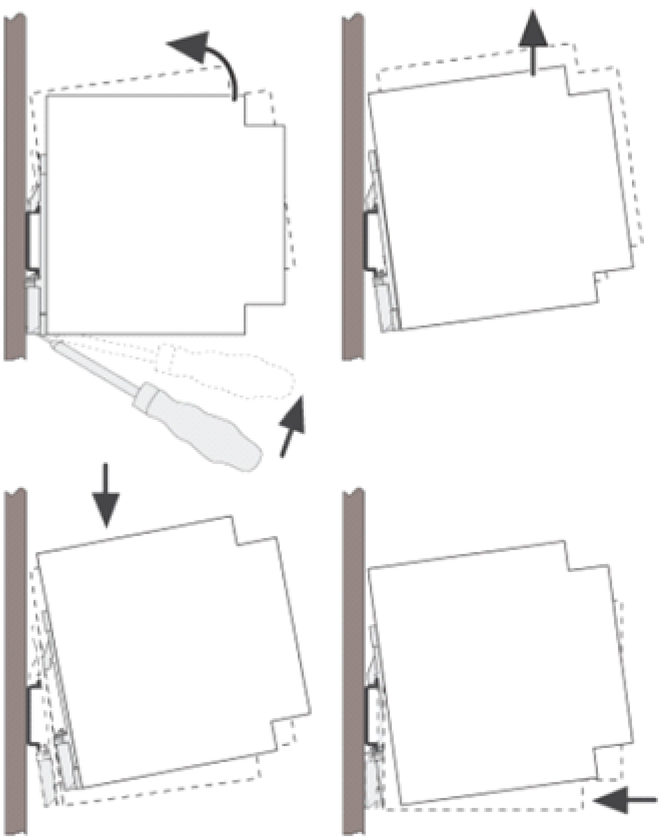
Cable	Solid	Flexible	AWG	Torque	Stripping Length
Input	0.2 - 16 mm (0.01 - 0.6 in)^2	0.5 - 10 mm (0.02 - 0.4 in)^2	14 - 6	1.2 - 1.5 Nm (10.6 - 13.3 in-lb)	10 mm (0.4 in)
Output	0.2 - 16 mm (0.01 - 0.6 in)^2	0.5 - 10 mm (0.02 - 0.4 in)^2	14 - 6	1.2 - 1.5 Nm (10.6 - 13.3 in-lb)	10 mm (0.4 in)

18.18.1.5 Mounting

Most units are supplied ready for installation in a narrow mounting position. The following figure displays the default mounting position for the Phoenix power supplies.

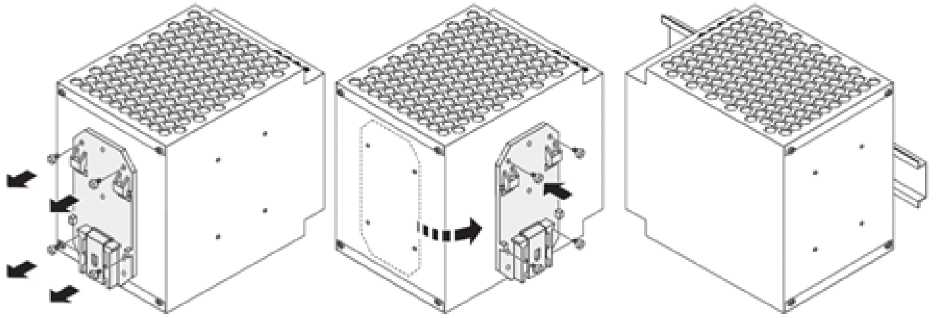
- **To mount the power supply unit:** position the module with the DIN-rail mounted guideway on the top edge of the DIN-rail and then snap it downwards.

- **To remove the unit:** release the snap-on catch using a screwdriver and detach the module from the bottom edge of the DIN-rail.



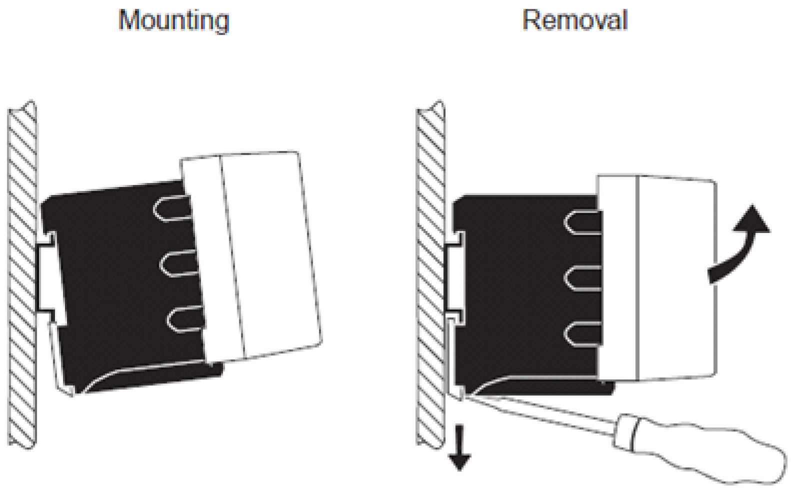
Typical Mounting Position

A side mounting position can be achieved by mounting the module onto the DIN-rail at a 90° angle. Mount the DIN-rail adapter (UTA 107) as displayed in the following figure. No additional assembly material is required.



Side Mounting Position

The Diode-OR Redundancy module can be snapped onto all DIN-rails according to EN 50 022-35. The module can be DIN-rail mounted horizontally (input terminal blocks facing upwards or downwards) or vertically. The following figure displays the default mounting and removal position for the redundancy module.



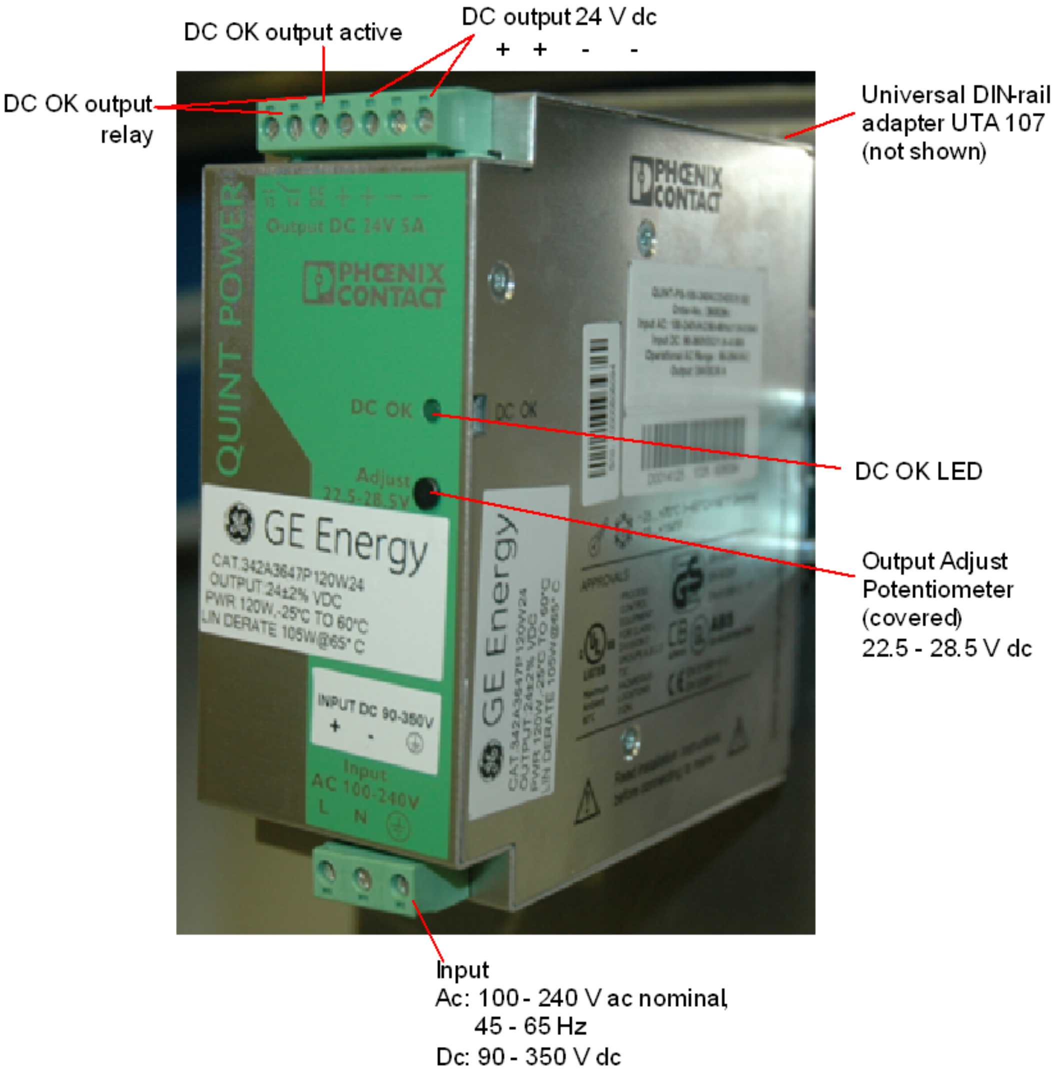
Diode-OR Module Mounting and Removal Position

Diode-OR Module Mounting Specifications

Mounting Position	Minimum Spacing Between Modules
Vertical	5 cm (2.0 in)
Horizontal	2 cm (0.8 in)

18.18.1.6 342A3647P120W24, 120 W, 24 V dc, 5 A Power Supplies

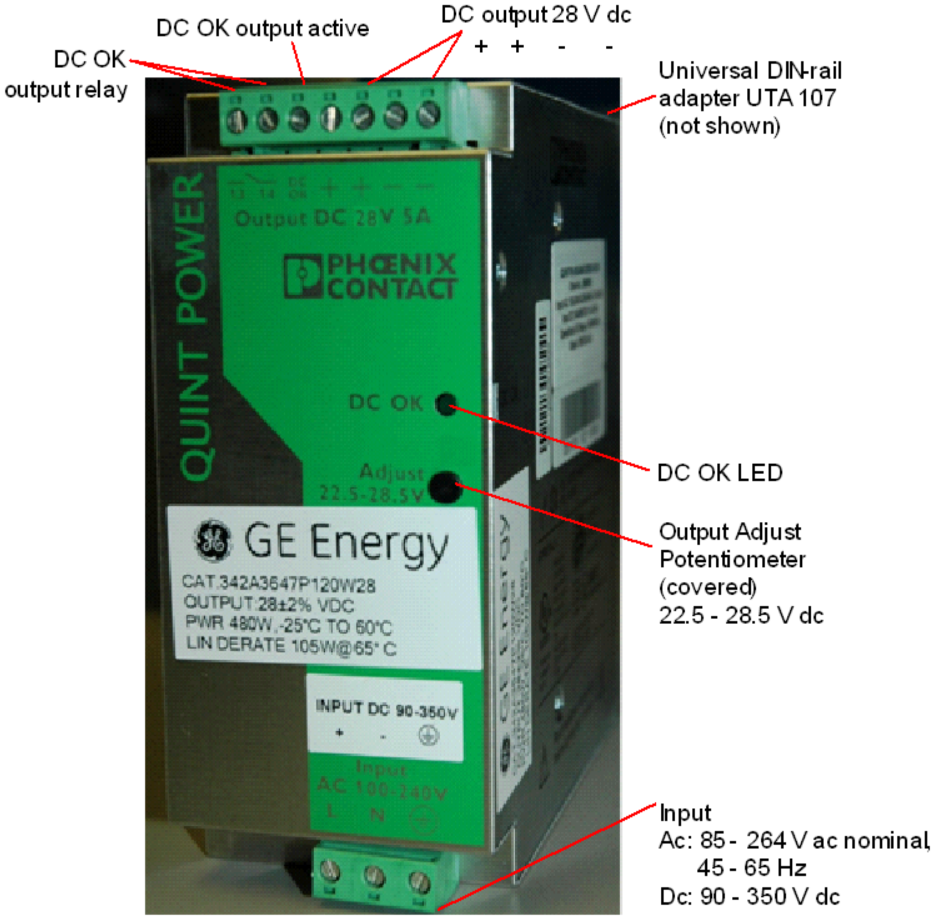
The 342A3647P120W24, 120 W, 24 V dc, 5 A Phoenix control power supply is a DIN-rail mounted, single-phase, switching power supply. The following photograph displays the features of the power supply.


DC OK output active
DC output 24 V dc
+ + - -
DC OK output relay
Universal DIN-rail adapter UTA 107 (not shown)
DC OK LED
Output Adjust Potentiometer (covered) 22.5 - 28.5 V dc
Input
Ac: 100 - 240 V ac nominal, 45 - 65 Hz
Dc: 90 - 350 V dc

342A3647P120W24, 120 W, 24 V dc, 5 A Power Supplies Features

18.18.1.7 342A3647P120W28, 120 W, 28 V dc, 4.2 A Power Supplies

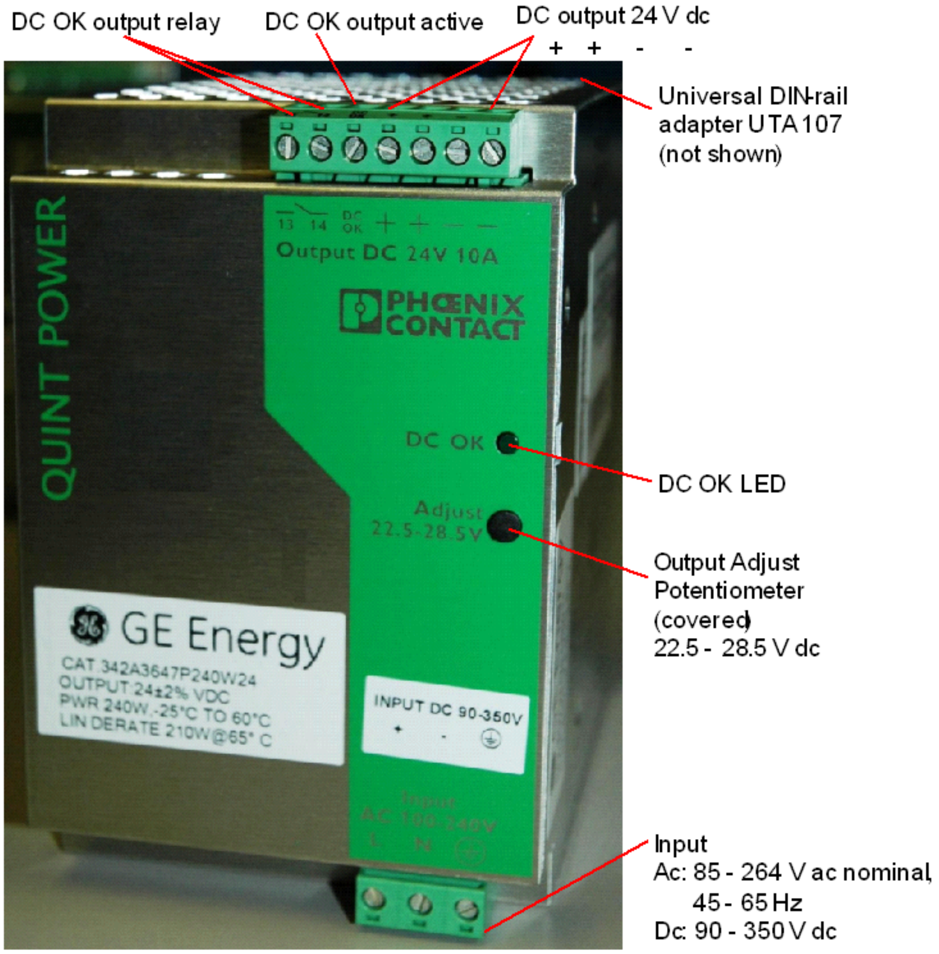
The 342A3647P120W28, 120 W, 28 V dc, 4.2 A Phoenix control power supply is a DIN-rail mounted, switching power supply. The following photograph displays the features of the power supply.



342A3647P120W28, 120 W, 28 V dc, 4.2 A Power Supplies Features

18.18.1.8 342A3647P240W24, 240 W, 24 V dc, 10 A Power Supplies

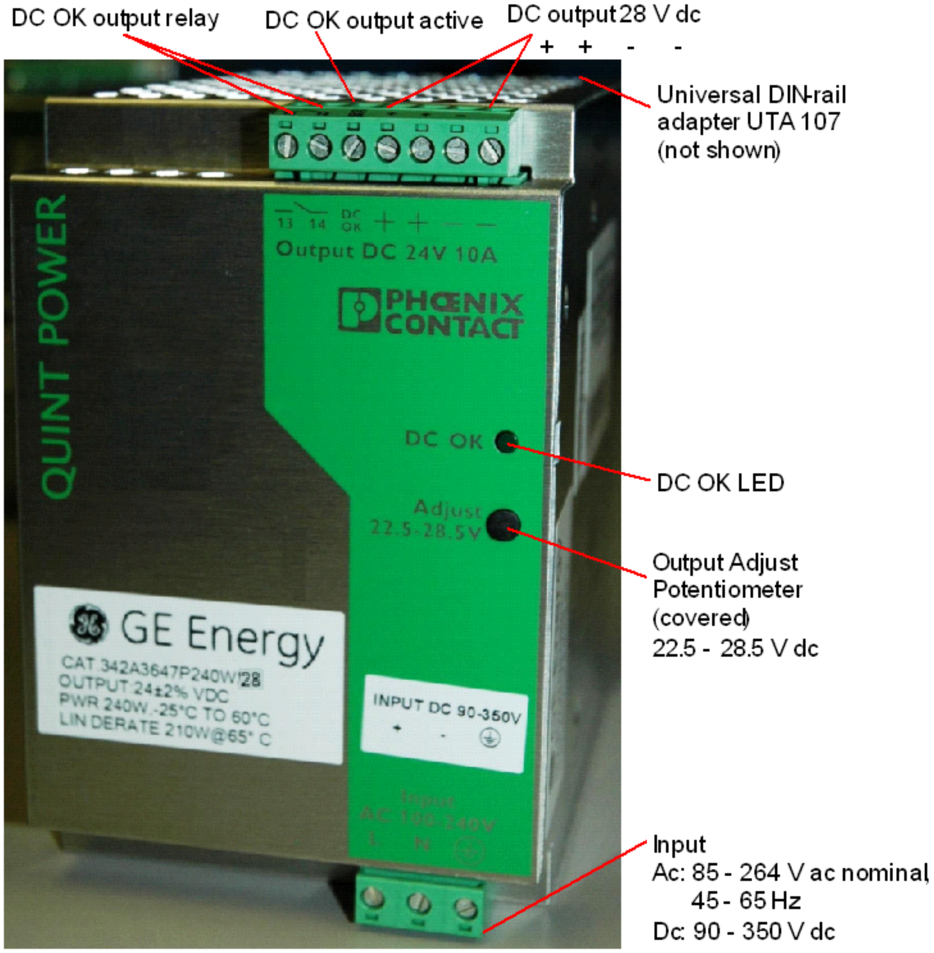
The 342A3647P240W24, 240 W, 24 V dc, 10 A Phoenix control power supply is a DIN-rail mounted, single-phase switching power supply. The following photograph displays the features of the power supply.



342A3647P240W24, 240 W, 24 V dc, 10 A Power Supplies Features

18.18.1.9 342A3647P240W28, 240 W, 28 V dc, 8.5 A Power Supplies

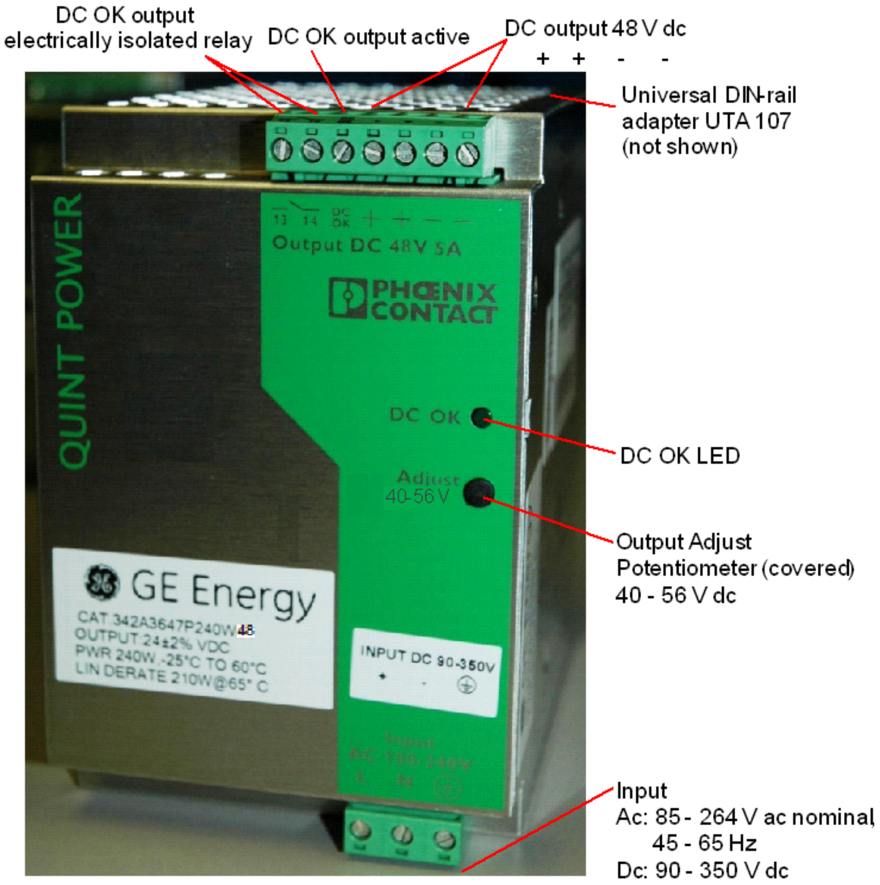
The 342A3647P240W28, 240 W, 28 V dc, 8.5 A Phoenix control power supply is a DIN-rail mounted, single-phase switching power supply. The following photograph displays the features of the power supply.



342A3647P240W28, 240 W, 28 V dc, 8.5 A Power Supplies Features

18.18.1.10 342A3647P240W48, 240 W, 48 V dc, 5 A Power Supplies

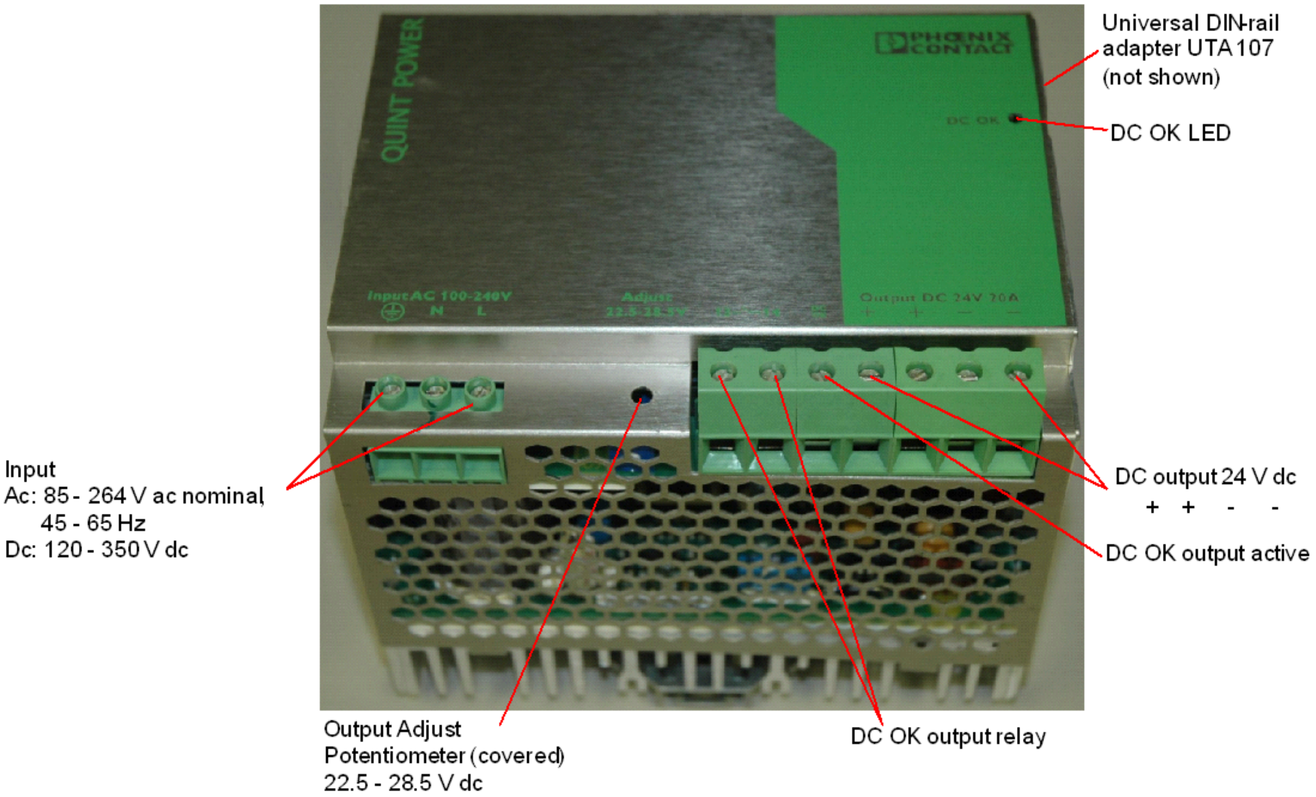
The 342A3647P240W28, 240 W, 48 V dc, 5 A Phoenix control power supply is a DIN-rail mounted, primary switching power supply for universal use. The following photograph displays the features of the power supply.



342A3647P240W28, 240 W, 48 V dc, 5 A Power Supplies Features

18.18.1.11 342A3647P480W24, 480 W, 24 V dc, 20 A Power Supplies

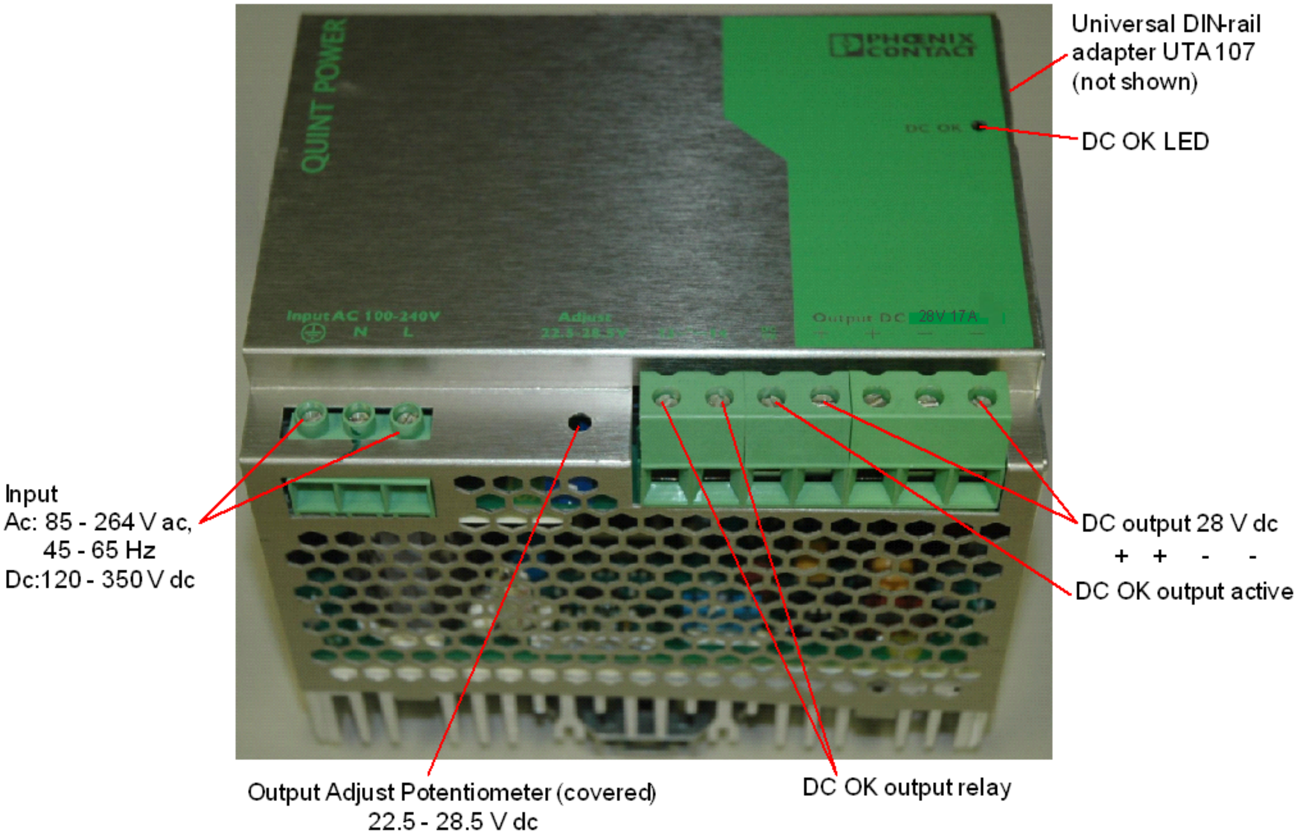
The 342A3647P480W24, 480 W, 24 V dc, 20 A Phoenix control power supply is a DIN-rail mounted, single-phase switching power supply. The following photograph displays the features of the power supply.



342A3647P480W24, 480 W, 24 V dc, 20 A Power Supplies Features

18.18.1.12 342A3647P480W28, 480 W, 28 V dc, 17 A Power Supplies

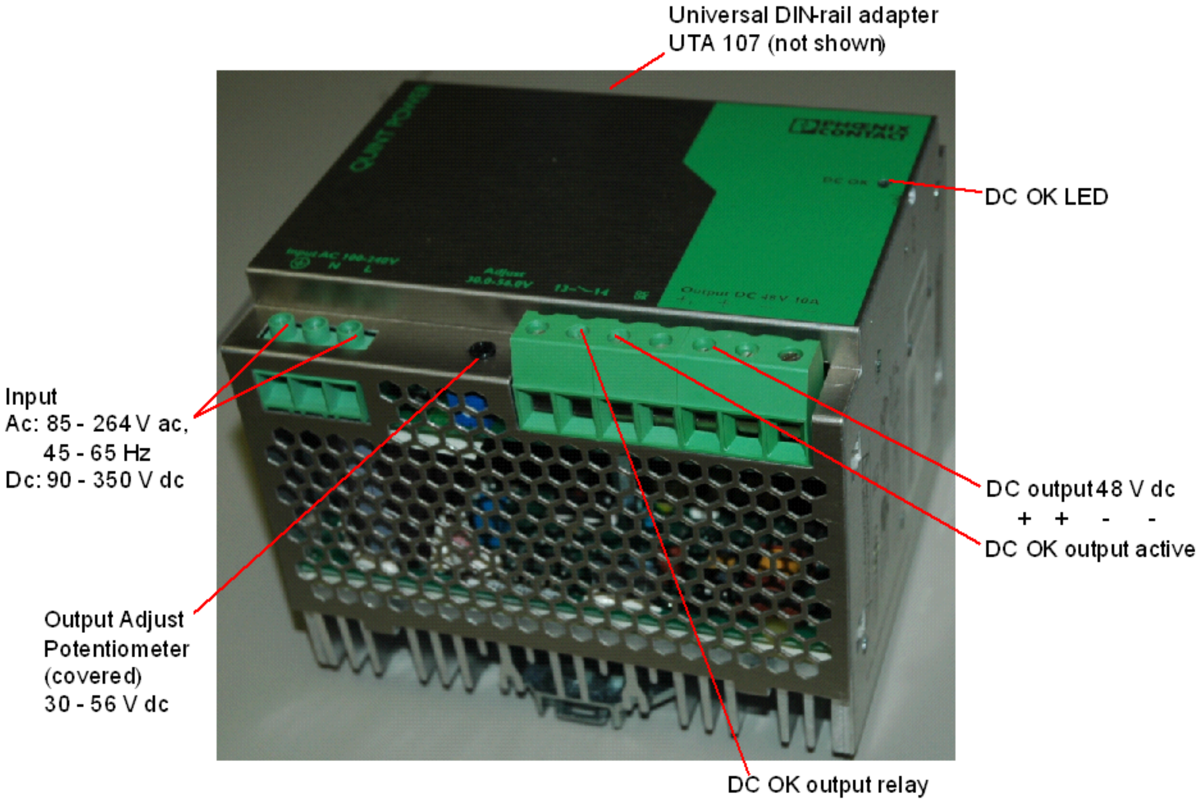
The 342A3647P480W28, 480 W, 28 V dc, 17 A Phoenix control power supply is a DIN-rail mounted, single-phase switching power supply. The following photograph displays the features of the power supply.



342A3647P480W28, 480 W, 28 V dc, 17 A Power Supplies Features

18.18.1.13 342A3647P480W48, 480 W, 48 V dc, 10 A Power Supplies

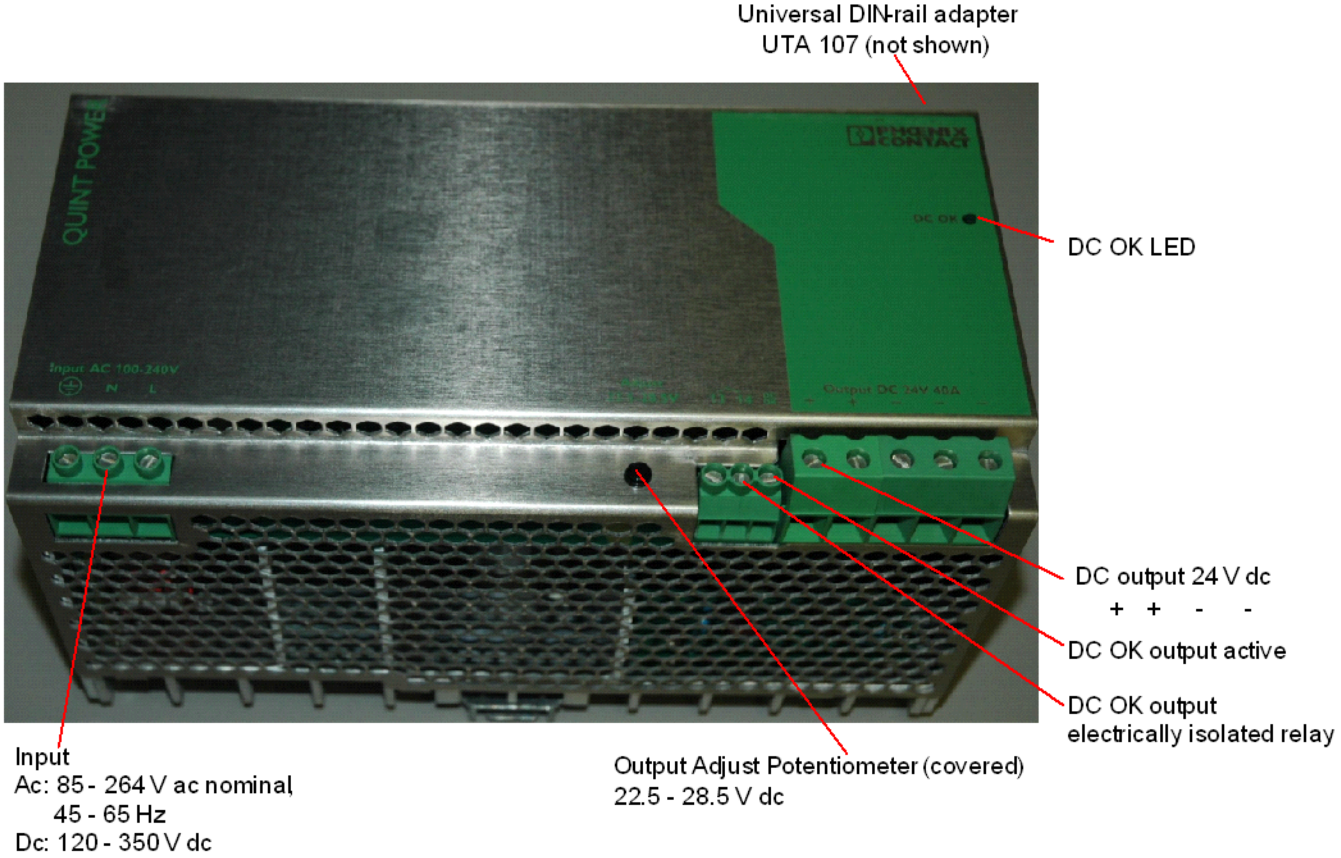
The 342A3647P480W48, 480 W, 48 V dc, 10 A Phoenix control power supply is a DIN-rail mounted, primary, single-phase switching power supply. The following photograph displays the features of the power supply.



342A3647P480W48, 480 W, 48 V dc, 10 A Power Supplies Features

18.18.1.14 342A3647P960W24, 960 W, 24 V dc, 40 A Power Supplies

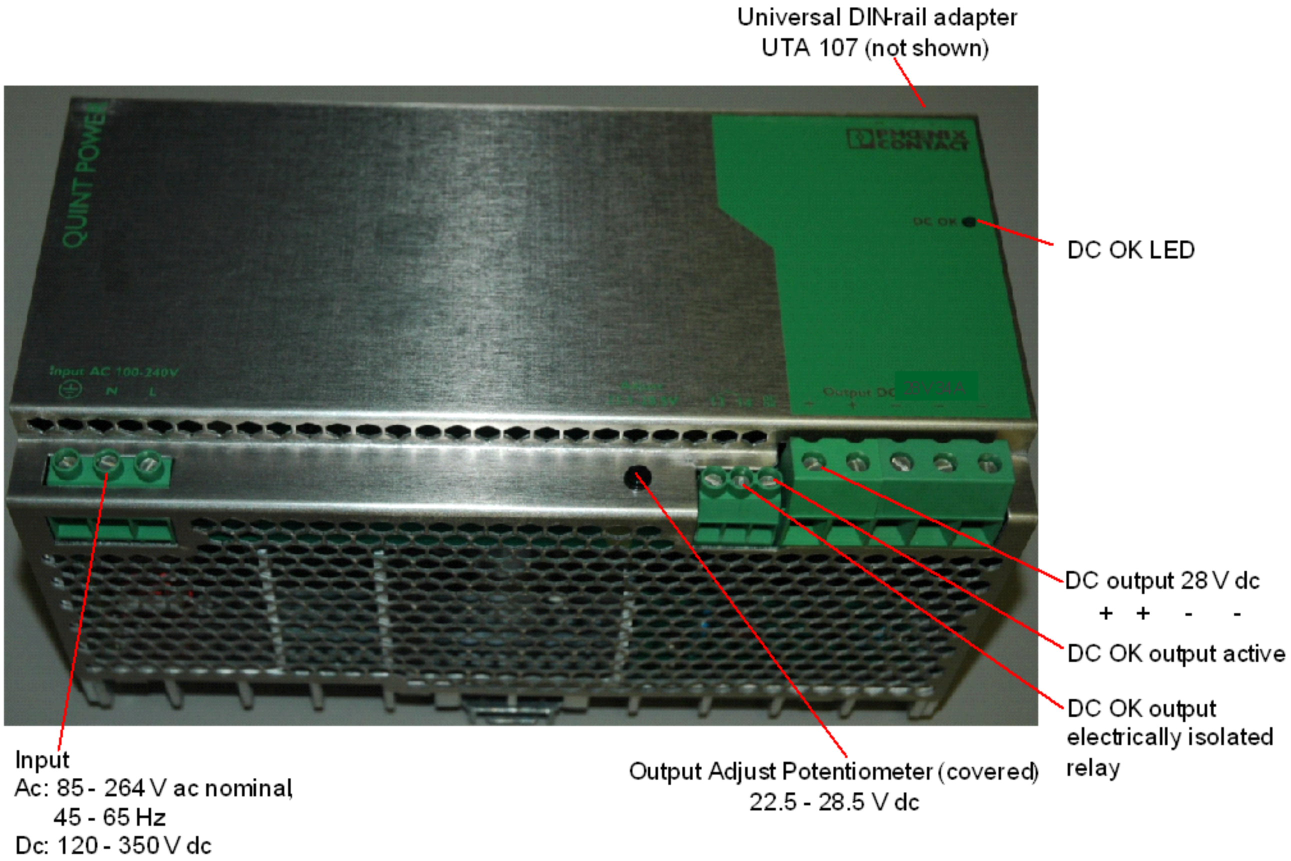
The 342A3647P960W24, 960 W, 24 V dc, 40 A Phoenix control power supply is a DIN-rail mounted, single-phase, primary switching power supply used for universal use. The following photograph displays the features of the power supply.


Universal DIN-rail adapter UTA 107 (not shown)
DC OK LED
DC output 24 V dc
+ + - -
DC OK output active
DC OK output electrically isolated relay
Output Adjust Potentiometer (covered) 22.5 - 28.5 V dc
Input
Ac: 85 - 264 V ac nominal, 45 - 65 Hz
Dc: 120 - 350 V dc
QUINT POWER
PHOENIX CONTACT
DC OK
Input AC 100-240V
N L
Output DC 24V 40A

342A3647P960W24, 960 W, 24 V dc, 40 A Power Supplies Features

18.18.1.15 342A3647P960W28, 960 W, 28 V dc, 34 A Power Supplies

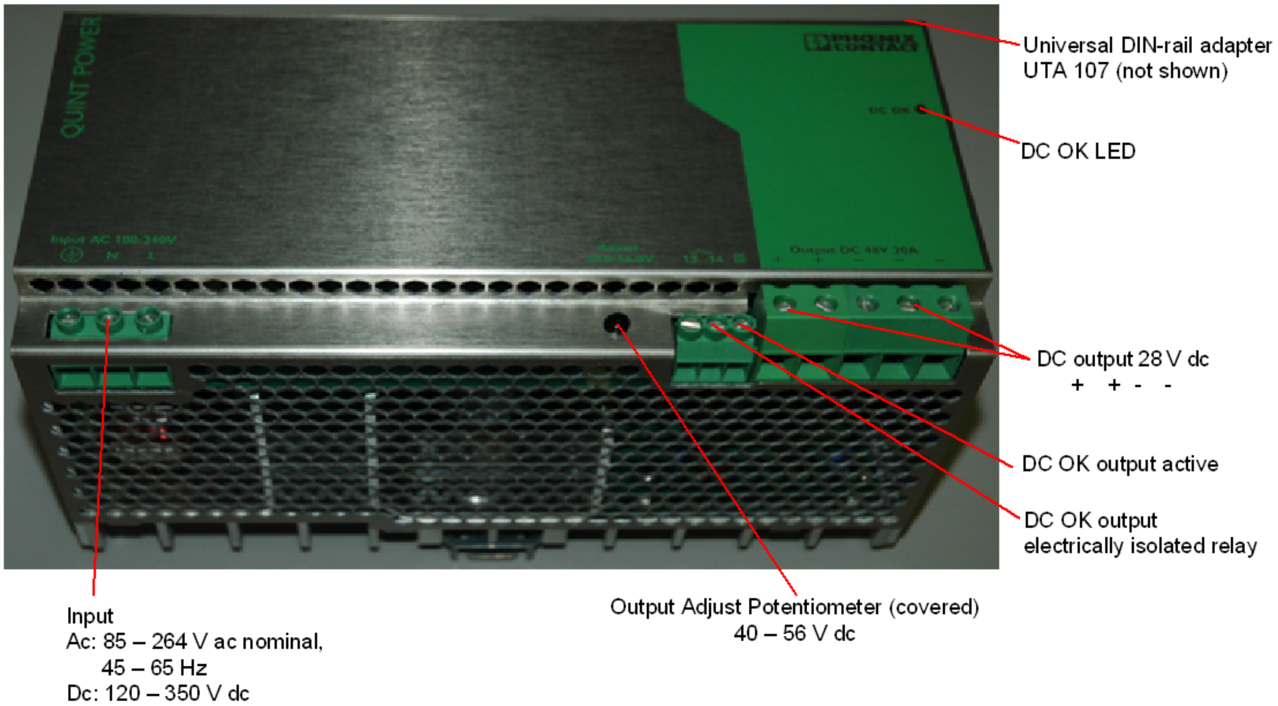
The 342A3647P960W28, 960 W, 28 V dc, 34 A Phoenix control power supply is a DIN-rail mounted, single-phase, primary switching power supply used for universal use. The following photograph displays the features of the power supply.



342A3647P960W28, 960 W, 28 V dc, 34 A Power Supplies Features

18.18.1.16 342A3647P960W48, 960 W, 48 V dc, 20 A Power Supplies

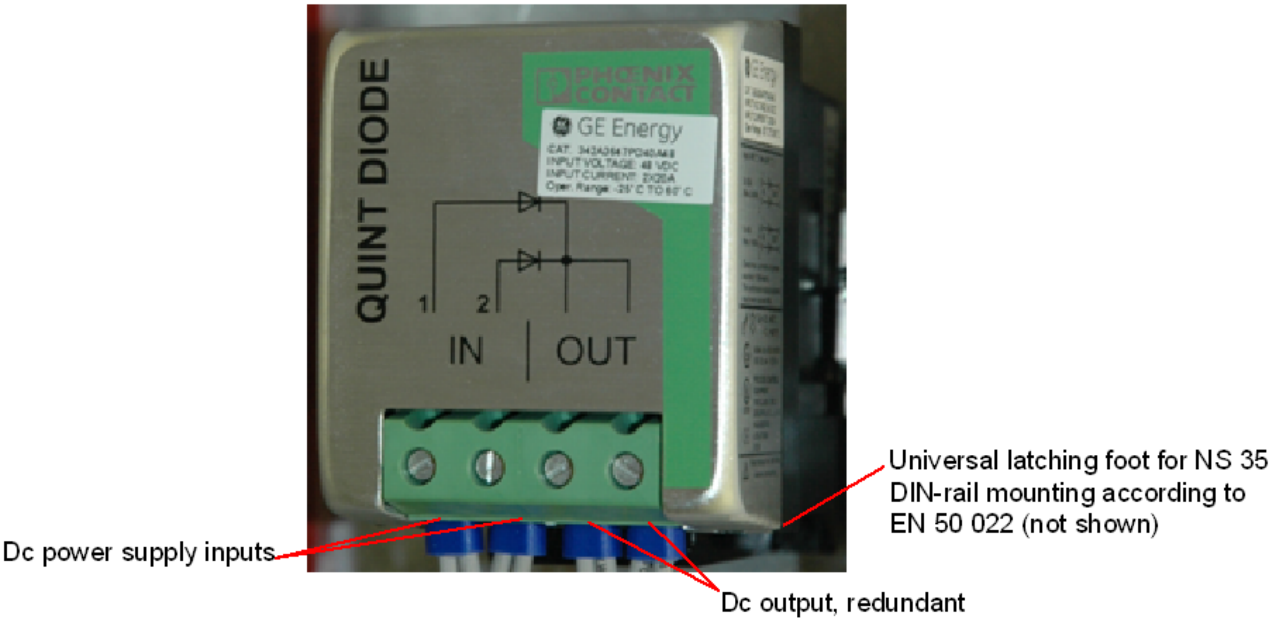
The 342A3647P960W28, 960 W, 28 V dc, 34 A Phoenix control power supply is a DIN-rail mounted, single-phase, primary switching power supply used for universal use. The following photograph displays the features of the power supply.



342A3647P960W28, 960 W, 48 V dc, 20 A Power Supplies Features

18.18.1.17 342A3647PD40A48, Diode-OR Redundancy Module, 48 V dc, 40 A Power Supplies

The 342A3647PD40A48, Diode-OR module, 48 V dc, 40 A Phoenix control power supply is a redundancy module that can be used to diode-OR and decouple two power supplies of the same type to increase power or provide redundancy. The Diode-OR module provides 100% decoupling of power supplies connected in parallel. The module is supplied ready for DIN-rail mounting. The following photograph displays the features of the Diode-OR module.

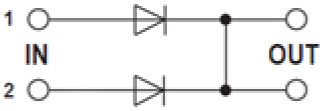


Universal latching foot for NS 35 DIN-rail mounting according to EN 50 022 (not shown)

Dc power supply inputs

Dc output, redundant

342A3647PD40A48, Diode-OR Module, 48 V dc, 40 A Redundancy Module Features



Diode-OR Module Schematic

Note This module provides redundant power supply configurations. At any given time, only one of the two supplies provides 100% of the load current. This module will not force load sharing between the supplies.

Diode-OR Module Specifications

Parameter	Condition	Specification
Voltage	Input, rated	60 V dc
	Reverse Bias Transient Protection	120 V dc
	Input to output voltage drop at rated current	0.65 V dc
Input Current	Input 1 or 2, rated	20 A dc
	Input 1 or 2, peak	30 A dc
	Input 1 and 2 in parallel, rated	40 A dc
	Input 1 and 2 in parallel, peak	60 A dc
	Input 1 and 2 in parallel, transient, 10 ms sine single pulse	1020 A pk
Power Dissipation	Input 1 and 2 at rated current	26 W
Reliability	Refer to the section, *Specifications*.	
Electrical Safety		
Environment		
Shock and Vibration		
EMC		

18.18.2 TRACO Power Supplies

The following table provides the features that are specific to the TRACO power supplies.

Item #	GE Part Number	Output Rated W	Output V dc	Input Voltage	Full Load Input Current	Hold Up Time ms 120/230 V ac
1	342A4917P150W28	150	28	93-132 or 187-264 V ac**	3 A at 115 V ac, 1.7 A at 230 V ac	25/30
2	342A4917P150W48	150	48	93-132 or 187-264 V ac**	3 A at 115 V ac, 1.7 A at 230 V ac	25/30
3	342A4917P300W24	300	24	93-132 or 187-264 V ac**	5.4 A at 115 V ac, 3.3 A at 230 V ac	25/30
4	336A4940FEP01	300	28	93-132 or 187-264 V ac**	5.4 A at 115 V ac, 3.3 A at 230 V ac	25/30
5	342A4917P600W24	600	24	93-132 or 187-264 V ac**	10.5 A at 115 V ac, 6.4 A at 230 V ac	15/25
6	342A4917P600W28	600	28	93-132 or 187-264 V ac**	10.5 A at 115 V ac, 6.4 A at 230 V ac	15/25
7	342A4917P600W48	600	48	93-132 or 187-264 V ac**	10.5 A at 115 V ac, 6.4 A at 230 V ac	15/25

Caution

**** The input voltage is based on the Input Select 115 V /230 V switch. Select the correct input voltage before applying power to prevent damage to the power supply.**

18.18.2.1 Specifications

Feature	Specification
Output Voltage Regulation	24, 28, and 48 V dc output has 2%
Mark VIe and Mark VIeS Compatibility Requirements	Vibration and contamination
Load Share	Multiple supplies can load share when wired together
Parallel Operation	Support without extra components. Diode-equivalent is included on the output of each power supply (with 342A4917 and 342A4922).
Input Filtering	Prevents sensitivity to input interference

18.18.2.2 342A4917P150W28 and 342A4917P150W48 Power Supplies

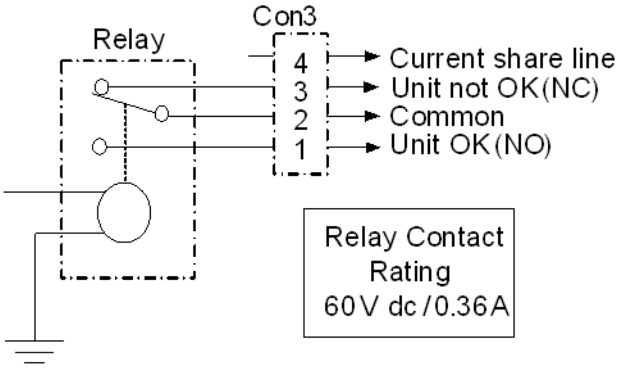
The dc power supplies 342A4917P150W28 and 342A4917P150W48 provide bulk dc power to electronic loads in the Mark VIe and Mark VIeS control systems. Power is supplied through a 3-position terminal, Con1, mounted on the bottom of the supply. The inputs are, from left to right, ground, neutral, and line. A switch selects the input voltage range of 93 to 132 V ac or 187 to 264 V ac. The nominal selected voltage is displayed on the switch. The full load input current is rated 3 A at 115 V ac and 1.7 A at 230 V ac. The user must protect the wiring with a slow blow fuse or Type C circuit breaker. The power supply is internally protected by a 4 A, 250 V time delay fuse. If ac line loss occurs, the power supply holdup feature will maintain the output for 25 ms for 115 V ac and 30 ms for 230 V ac.

Caution

Select the correct input voltage before applying power to prevent damage to the power supply.

Power output is through a seven-position terminal, Con3, located on the top of the supply. The terminal is clearly labeled on the side of the power supply displaying all its connection points. Con2 is not used.

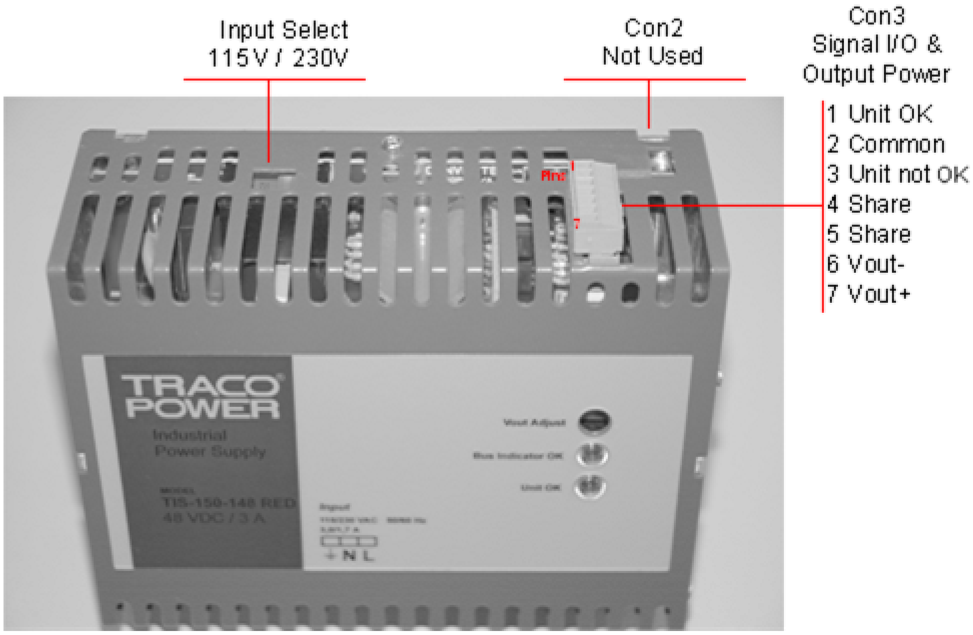
Power supply status is a dry form C relay contact rated at 0.36 A at 60 V dc. The relay indicates the output is within regulation, with no over-current and no over-temperature. The relay contacts, wired to Con3, have normally open (NO) on pin 1, common on pin 2, and normally closed (NC) on pin 3. When the power supply status is OK, pin 1 to pin 2 is closed and pin 3 to pin 2 is open. Pins 1 and 2 are typically wired to a JPDS or JPDM power distribution board for feedback to the PPDA power diagnostic pack.



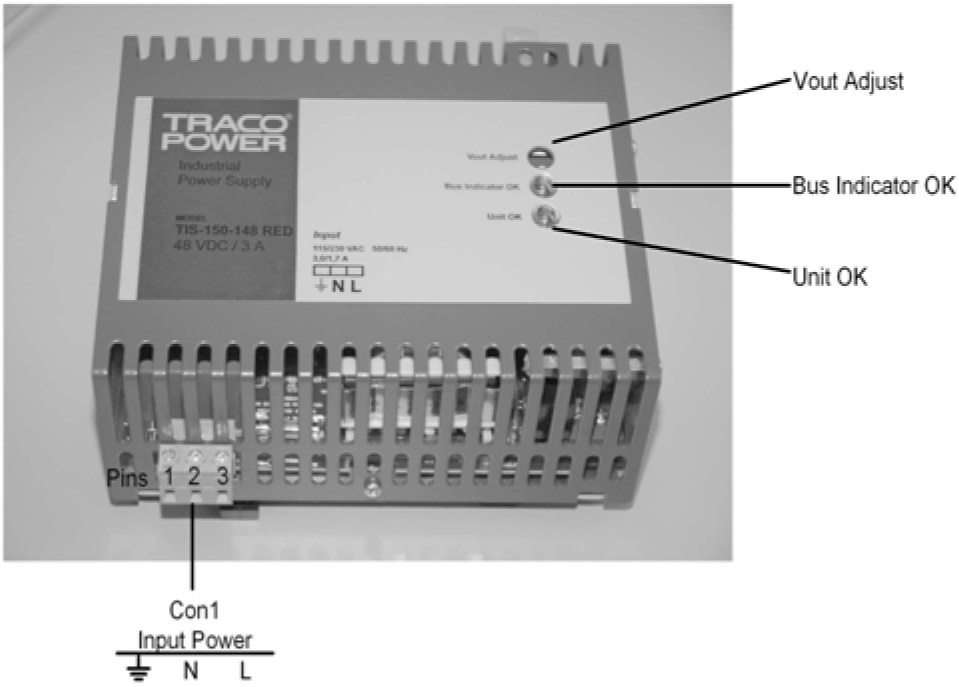
Power Supply Relay Contacts on Con3

Two or more power supplies of the same design can be paralleled, sharing the current equally to provide more output power. Pin 4 on Con3 provides an active load sharing signal and must be wired between power supplies to enable sharing. For accurate load sharing (within 10%), the negative outputs from all supplies must be tied together within a few feet of the supplies.

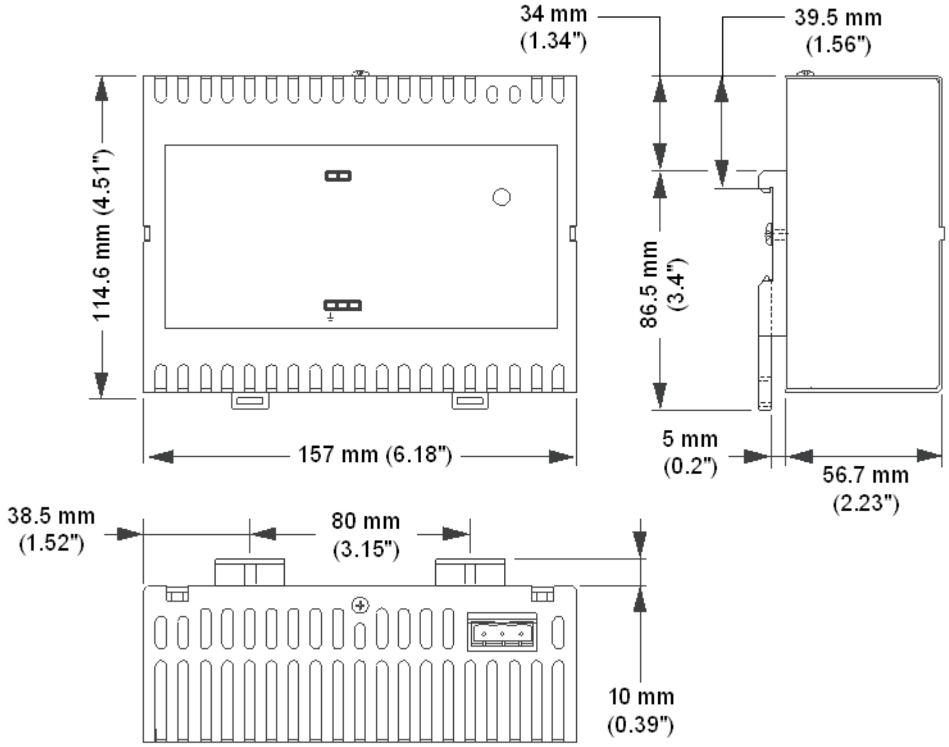
The Vout Adjust potentiometer provides adjustment of the output voltage from 24 to 32 V on the 28 V model and from 48 to 52 V dc on the 48 V model. The power supply has two indicator lamps, Bus Indicator OK and Unit OK. Bus Indicator OK lights when input power is applied. Unit OK lights when the supply is within regulation and has no over-current or over-temperature.



Ac Input 150 W Power Supply Front View



Ac Input 150 W Power Supply Bottom View



Ac Input 150 W Power Supply Dimensions

18.18.2.3 342A4917P300W24 and 336A4940FEP01 Power Supplies

The dc power supplies 342A4917P300W24 and 336A4940FEP01 provide bulk dc power to electronic loads in the Mark VIe and Mark VIeS control systems. Power is supplied through the 3-position removable plug, Con1, mounted on the bottom of the supply. The inputs are, from left to right, ground, neutral, and line. A switch, mounted on the top of the supply, selects the input voltage range of 93 to 132 V ac or 187 to 264 V ac. The nominal selected voltage is displayed on the switch.

Caution

Select the correct input voltage before applying power to prevent damage to the power supply.

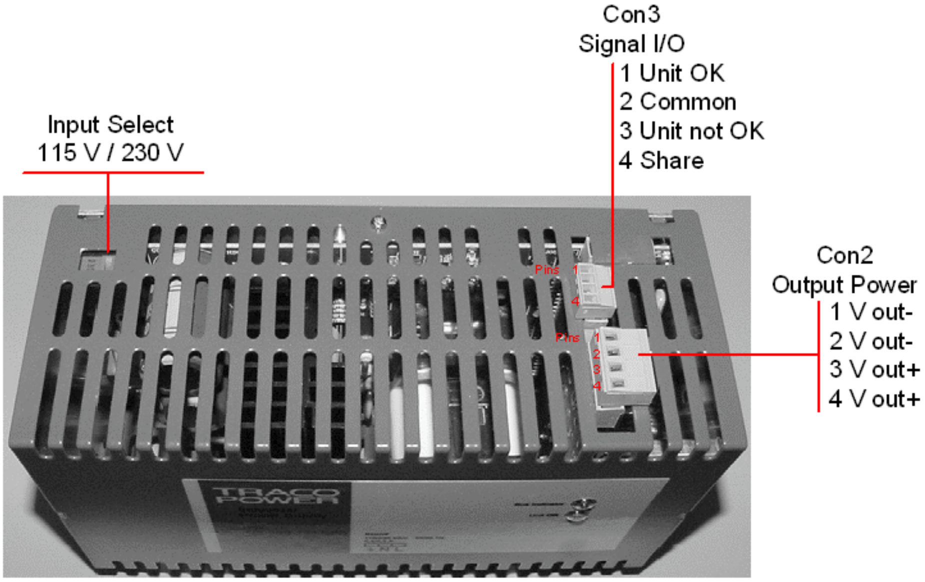
The full load input current is rated 5.4 A at 115 V ac and 3.3 A at 230 V ac. The user must protect the input wiring using a slow blow fuse or a Type C circuit breaker. The power supply is internally protected with a 6.3 A 250 V time delay fuse. If ac line loss occurs, the power supply hold up feature will maintain the output for 25 ms at 115 V ac and 30 ms at 230 V ac.

Power output is from Con2 and signal I/O is through the Con3 connector. Each connector is a removable plug. The connectors are displayed in the following figure.

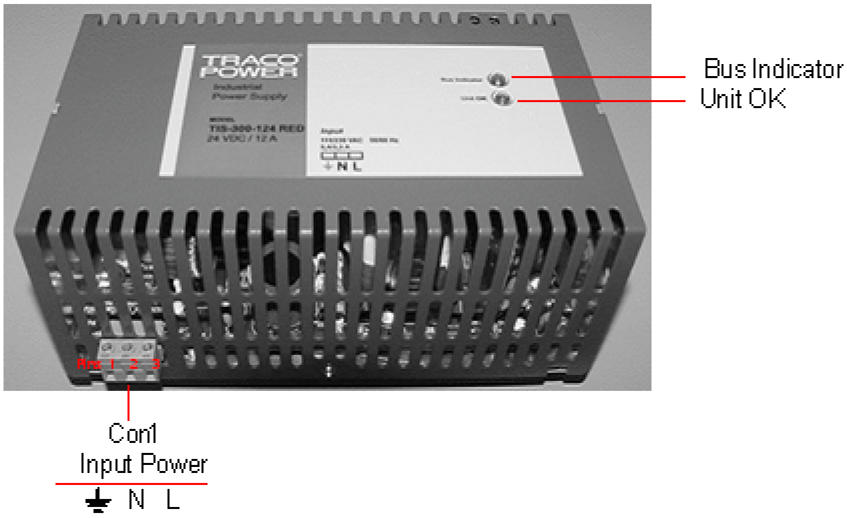
Power supply status is a dry form C relay contact rated at 3.6 A at 60 V dc. The relay indicates the output is within regulation, with no over-current and no over temperature. The relay contacts, wired to Con3 have normally open (NO) on pin 1, common on pin 2, and normally closed (NC) on pin 3. When the power supply status is OK, pin 1 to pin 2 is closed and pin 3 to pin 2 is open. Con3 is a removable plug, smaller than Con1 and Con2. Con3 accepts 18G wire. Pins 1 and 2 are typically wired to a JPDS or JPDM power distribution boards for feedback to the PPDA power diagnostic pack.

Two or more power supplies of the same design can be paralleled, sharing the current equally to provide more output power. Pin 4 on Con3 provides a signal for active load sharing. Pin 4 must be wired between power supplies for load sharing. For accurate load sharing (within 10%), the negative outputs from all supplies must be tied together within a few feet of the supplies.

The Vout Adjust potentiometer provides adjustment of the output voltage from 24- 32 V dc. The power supply has two indicator lamps, Bus Indicator and Unit OK. Bus Indicator lights when input power is applied. Unit OK lights when the supply is within regulation and has no over-current or over-temperature.



Ac Input 300 W Power Supply Top View



Ac Input 300 W Power Supply Bottom View

18.18.2.4 342A4917P600W24, 342A4917P600W28, and 342A4917P600W48 Power Supplies

The dc power supplies 342A4917P600W24, 342A4917P600W28, and 342A4917P600W48 supply bulk dc power to control system electronic loads. Power input is through a 3-position terminal, Con1, mounted on the top left side. The inputs are, from left to right, ground, neutral, and line. A switch selects the input voltage range of 93 to 132 V ac or 187 to 264 V ac. The nominal selected voltage is displayed on the switch. The full load input current is rated 10.5 A at 115 V ac and 6.4 A at 230 V ac. The user must protect the input wiring using a slow blow fuse or Type C circuit breaker. The power supply is internally protected by a 12 A, 250 V time delay fuse. If ac line loss occurs, the power supply holdup feature will maintain the output for 15 ms for 115 V ac, and 25 ms for 230 V ac.

Caution

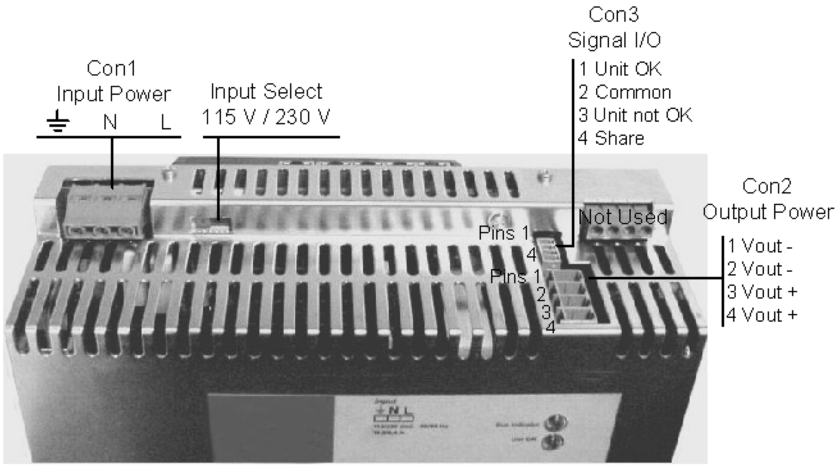
Select the correct input voltage before applying power to prevent damage to the power supply.

Power output is through the Con2 connector. Positive dc output is on pins 3 and 4 and dc common is on pins 1 and 2.

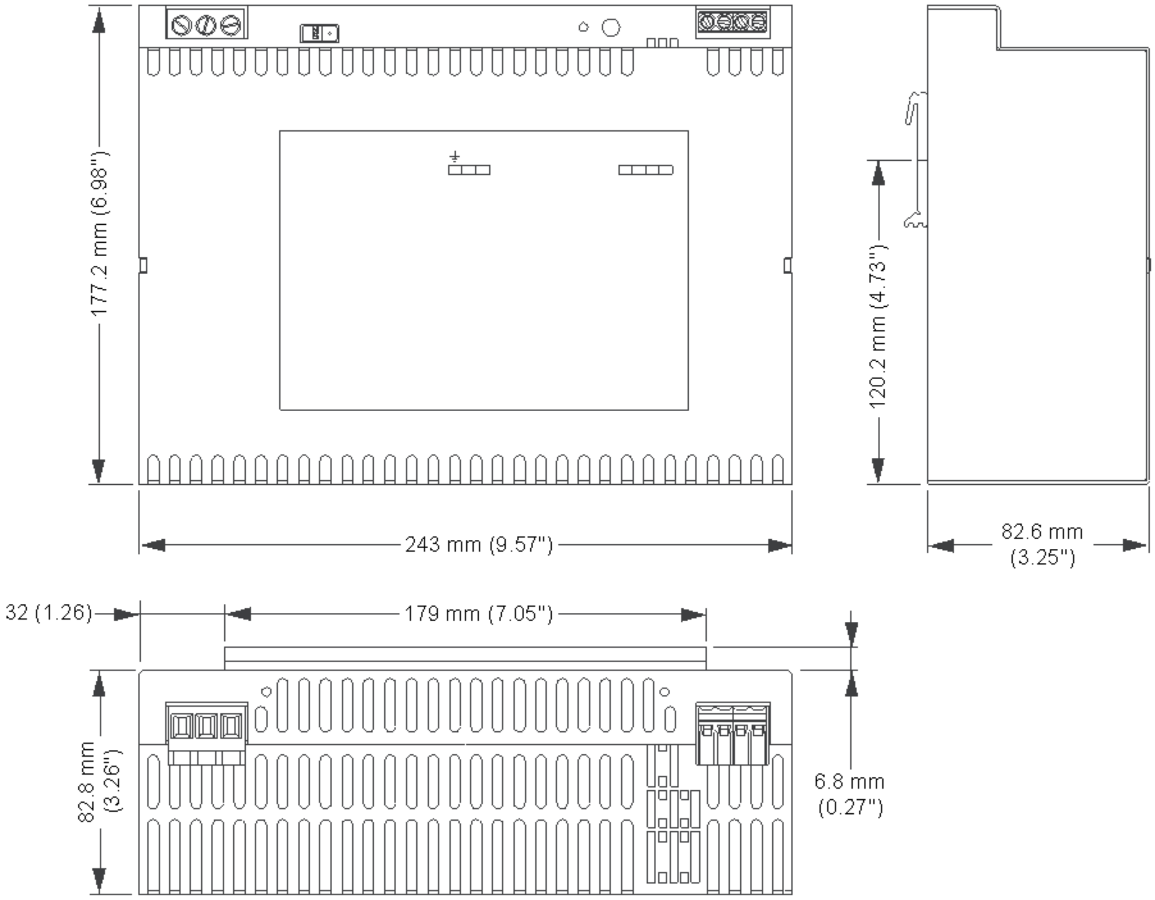
Power supply status is a dry form C relay contact rated at 3.6 A at 60 V dc. The relay indicates the output is within regulation, with no over-current, and no over-temperature. The relay contacts, wired to Con3, have normally open (NO) on pin 1, common on pin 2, and NC on pin 3. Con3 is a terminal that is smaller than Con1 and Con2. It accepts 18G wire. Pins 1 and 2 are typically wired to a JPDS or JPDM power distribution board for feedback to the PPDA power diagnostic pack.

Two or more power supplies can be paralleled, sharing the current equally to provide more output power. Pin 4 on Con3 provides a signal for active load sharing. Pin 4 must be wired between power supplies for load sharing. For accurate load sharing (within 10%), the negative outputs from all supplies must be tied together within a few feet of the supplies.

The power supply has two indicator lamps, Bus Indicator and Unit OK. Bus Indicator lights when input power is applied. Unit OK lights when the supply is within regulation and has no over-current or over-temperature.



Ac Input 600 W Power Supply Top View



Ac Input 600 W Power Supply Dimensions

18.18.3 ACROPower Power Supplies

The following table provides the features that are specific to the ACROPower power supplies.

ACROPower Power Supplies

Item #	GE Part Number	Output Rated W	Output V dc	Input Voltage	Full Load Input Current
1	342A4922P28V150DL	150	28	18-36 V dc	10 A at 18 V dc, 5 A at 36 V dc
2	342A4922P28V150DH	150	28	70-145 V dc	3 A at 70 V dc, 1.2 A at 145 V dc
3	342A4922P28V500DL	500	28	18-36 V dc	33 A at 18 V dc, 17 A at 36 V dc
4	342A4922P28V500DH	500	28	70-145 V dc	8 A at 115 V ac, 4 A at 230 V ac

18.18.3.1 Specifications

Feature	ACROPower Specification
DC/DC Operation, Input Voltage	24 and 125 V dc
Output Voltage	28 V dc, 2% regulation
Available Ratings	150 and 500 W
Parallel Operation	Built-in diode-OR and current sharing for N+1 redundant connection
Mark VIe Compatibility Requirements	Electrical Safety Standards, EMC Standards, Environmental Standards

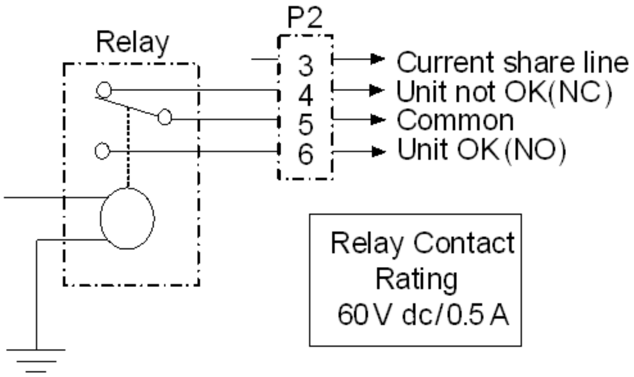
18.18.3.2 342A4922P28V150DL and 342A4922P28V150DH Power Supplies

The dc power supplies 342A4922P28V150DL and 342A4922P28V150DH, are used for the Mark VIe and Mark VIeS control system bulk 28 V dc power to electronic loads.

Power input is through the P1 connector, a pluggable box terminal. Positive dc input is connected to pin 1, negative dc input to pin 2, and ground to pin 3. The input voltage range is 18 to 36 V dc on the 24 V dc In supply and 70 to 145 V dc on the 125 V dc In supply. The input current for the 24 V dc In power supply is 10 A at 18 V dc and 5 A at 36 V dc. This supply is internally protected with a 15 A, 125 V time delay fuse. The input current for the 125 V dc In power supply is 3 A at 70 V dc and 1.2 A at 145 V dc. This supply is internally protected with a 4 A, 250 V time delay fuse. The user must protect the input wiring using a time delay fuse or circuit breaker.

Power output is through the P2 connector, a pluggable box terminal. Positive dc output is connected to pin 1 and dc common to pin 2. The supply meets the 150 W current rating over the convection cooled temperature range of -30 to 65ºC (-22 to 149 ºF).

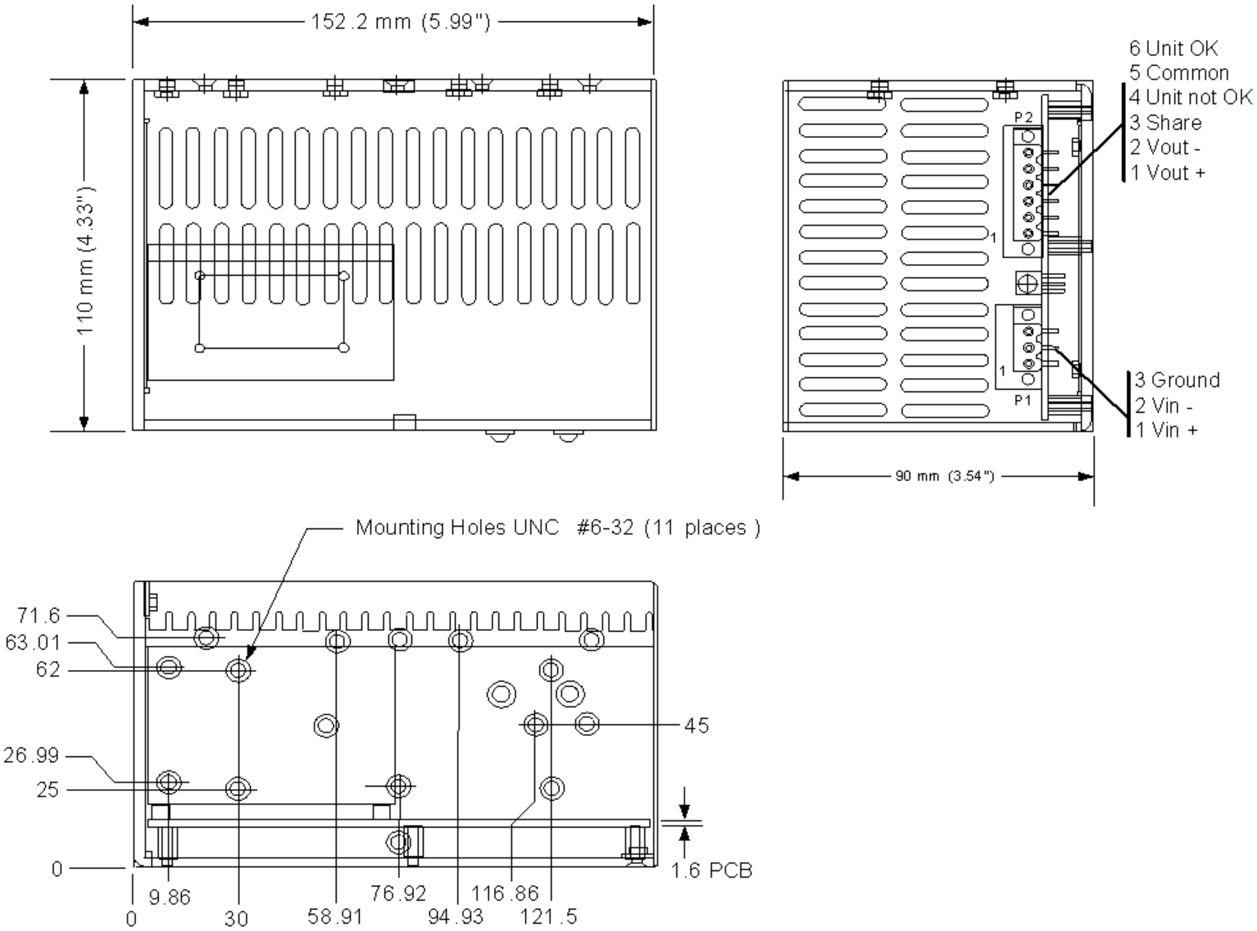
Power supply status is a dry form C relay contact rated at 0.5 A at 60 V dc. The relay indicates the output is within regulation, with no over-current and no over-temperature. The relay contacts, wired to P2, have normally open (NO) on pin 6, common on pin 5, and normally closed (NC) on pin 4. Pin 5 and pin 6 are typically wired to a JPDS or JPDM power distribution board for feedback to the PPDA power diagnostic pack.



Power Supply Relay Contacts on P2

Multiple power supplies can be paralleled, sharing current equally to provide more output power. Pin 3 on P2 provides active load sharing. For accurate load sharing (within 10%), the negative outputs from all supplies must be tied together within a few feet of the supplies.

The power supply has two indicator lamps, INP PWR and OUTP OK. INP PWR lights when input power is applied. OUTP OK lights when the unit is within regulation and has no over-current or over-temperature. The status output relay displays the same status.



Dc Input 150 W 28 V dc Power Supply Dimensions

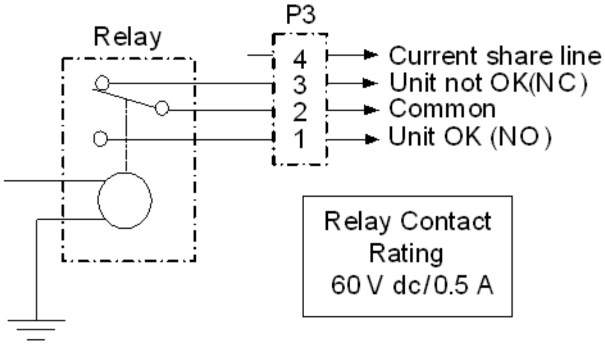
18.18.3.3 342A4922P28V500DL and 342A4922P28V500DH Power Supplies

The dc power supplies 342A4922P28V500DL and 342A4922P28V500DH supply bulk 28 V dc power to Mark VIe and Mark VIeS electronic loads.

Power is supplied through the P1 connector, a pluggable box terminal. Positive dc input is connected to pins 3 and 4, negative dc input to pins 1 and 2, and ground to pin 5. A ferrite filter is included in the input wiring to meet CE requirements. The input voltage range is 18 to 36 V dc on the 24 V dc In supply and 70 to 145 V dc on the 125 V dc In supply. The input current for the 24 V dc In power supply is 33 A at 18 V dc and 17 A at 36 V dc. This supply is internally protected with a 50 A, 300 V time delay fuse. The input current for the 125 V dc In power supply is 8 A at 70 V dc and 4 A at 145 V dc. This supply is internally protected with a 15 A, 250 V time delay fuse. The user must protect the input wiring using a time delay fuse or circuit breaker.

Power output is through the P2 connector, a pluggable box terminal. Positive dc input is connected to pins 3 and 4 and dc common to pins 1 and 2. A ferrite filter is included in the input wiring to meet CE requirements. The supply meets the 500 W current rating over the convection cooled temperature range of -30 to 65ºC (-22 to 149 ºF).

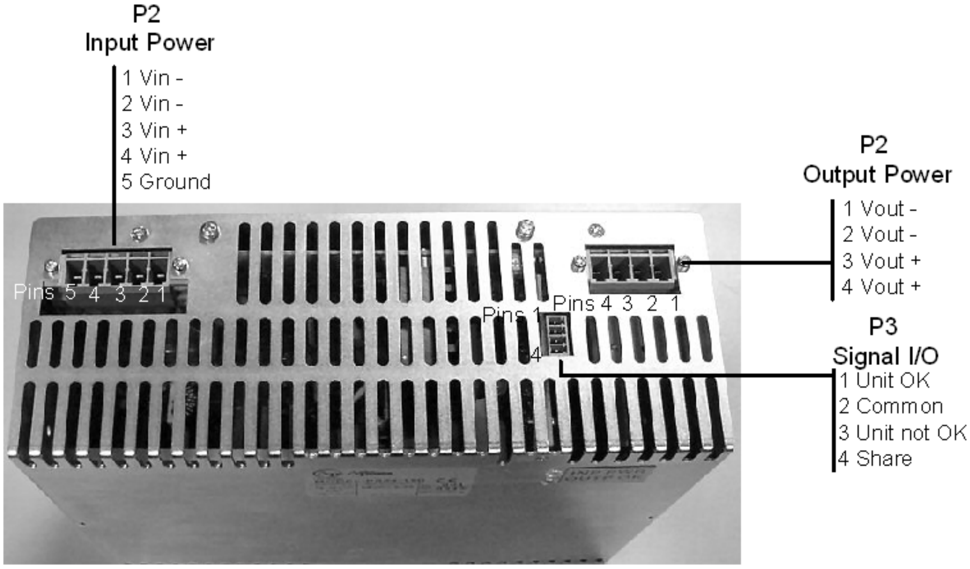
Power supply status is a dry form C relay contact rated at 0.5 A at 60 V dc. The relay indicates the output is within regulation, with no over-current and no over-temperature. The relay contacts, wired to P3, have normally open (NO) on pin 1 and common on pin 2. P3, a removable plug smaller than P1 and P2, accepts 18G wire. Pins 1 and 2 are typically wired to a JPDS or JPDM power distribution board for feedback to the PPDA power diagnostic pack.



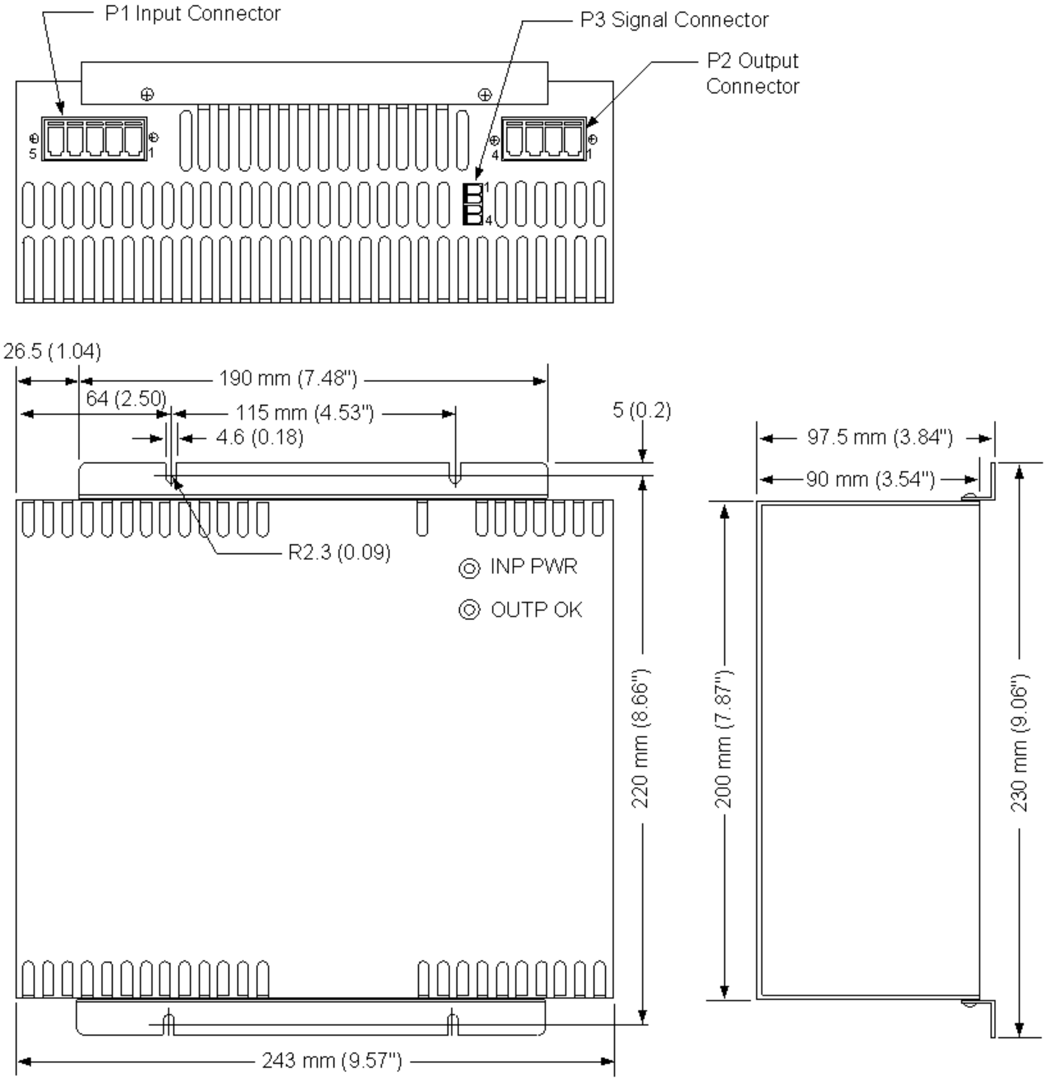
Power Supply Relay Contacts on P3

Multiple power supplies can be paralleled, sharing the current equally to provide more output power. Pin 4 on P3 provides a signal for active load sharing. Pin 4 must be wired between power supplies for load sharing. For accurate load sharing (within 10%), the negative outputs from all supplies must be tied together within a few feet of the supplies.

The power supply has two indicator lamps, INP PWR and OUTP OK. INP PWR lights when input power is applied. OUTP OK lights when the unit is within regulation and has no over-current or over-temperature. The status output relay displays the same status.



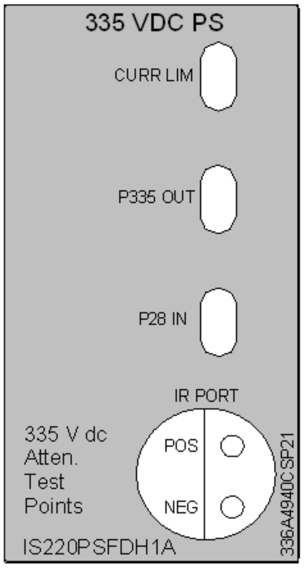
Dc Input 500 W Power Supply Top View



Dc Input 500 W 28 V Power Supply Dimensions

18.19 PSFD Flame Detector Power Supply

18.19.1 Functional Description



Infrared Port Not Used

The Flame Detector Power Supply (PSFD) typically mounts above the primary gas turbine trip protection (TRPG) terminal board. The source power is 28 V dc, from a power distribution board (JPDL). The output is rated for 335 V dc, 5 mA. Three power supplies are connected to J3, J4, and J5 of the TRPG in a diode-ORed, TMR configuration to power up to eight flame detectors. Each supply can power all eight flame detectors should the other two power supplies fail.

The main features of the PSFD include:

- Convection cooling – no cooling fans used
- Ambient temperature range is -30 to 65ºC (-22 to 149 ºF)
- 28 V dc input ±5% (26.6 to 29.4 V dc)
- Unregulated output varies with input ±5% (318 to 352 V dc)
- 1700 V dc isolation
- Output over voltage protection
- Test point pair to monitor Attenuated 335 V dc Output
- Three diagnostic LEDs
- Outputs can be diode-ORed with external diode.
- Output current limit at 7 mA dc
- Soft start hot swap input limits inrush current to 550 mA peak.
- Input filtering limits emissions and reduces sensitivity to input interference

18.19.2 Installation

Warning

To prevent electric shock, turn off power to the pack, then test to verify that no power exists on the module before touching it or any connected circuits.

Attention

To prevent equipment damage, do not remove, insert, or adjust any connections while power is applied to the equipment.

➢ **To install the PSFD**

1. Securely mount the TRPG and install the mounting plate for the PSFD. Typically, this mounting is on the upper level above the TRPG. To avoid risk of electrical shock, the mounting plant must be connected to chassis ground, typically FE (Field Earth).

2. Mechanically secure the PSFD using the threaded studs on the housing. The studs slide into a mounting brackets on the mounting plate.

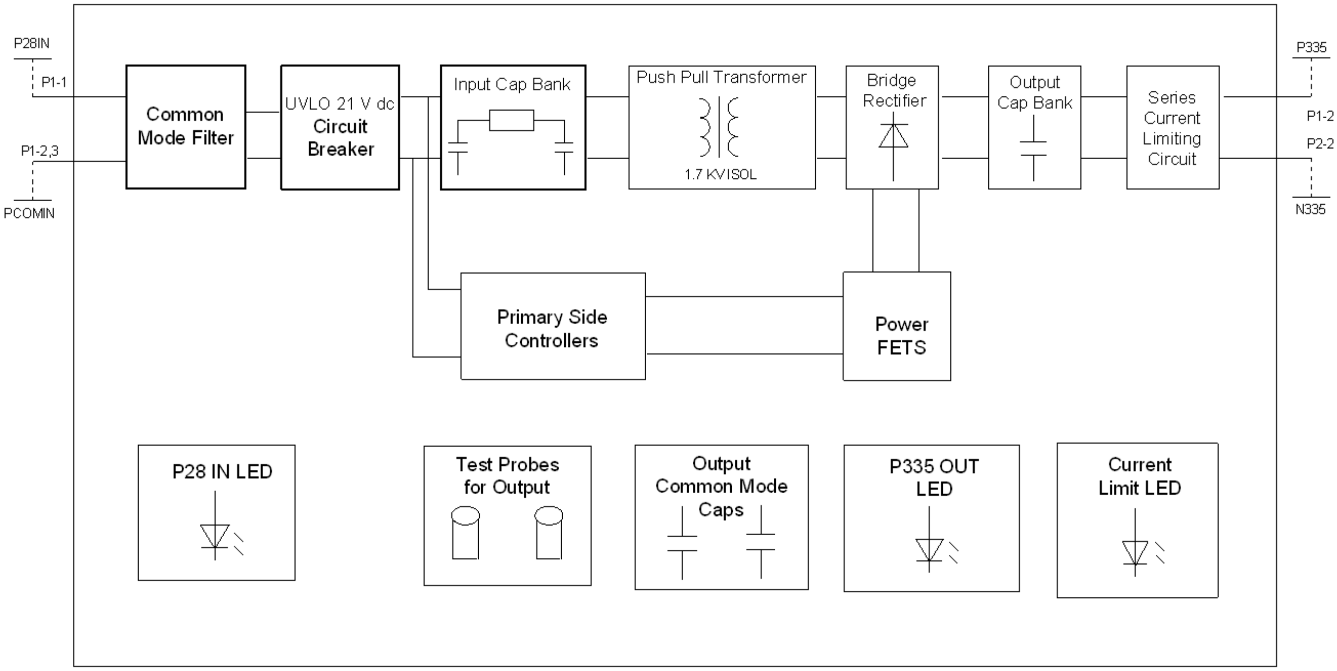
3. Connect the 335 V dc cable between PSFD 2x2 connector P2 and J3, J4, or J5 on the TRPG.

4. Apply 28 V dc power to the PSFD by plugging in the 1x3 connector P1 on the side of it. It is not necessary to insert this connector with the power removed from the cable as it has inherent soft-start capability that controls current inrush on power application.

18.19.3 Operation

The PSFD produces 335 V dc from 28 V dc. The 28 V dc input is current limited and hot swap compatible. The input is transformer isolated from the floating output. The switching topology is an non-regulated fixed ratio push pull converter. The input and output are current limited and the input is also hot swappable.

The output voltage can be monitored locally using a differential pair of test points, attenuated 100:1.



Power Supply Block Diagram

This 25 kHz switching power supply topology is push-pull with no feedback, that is it is open loop. The output increases and decreases proportionately to the input voltage. The push pull transformer has a 1:12 turns ratio to raise the 28 V dc input to 336 V dc. Diode drops reduce the output voltage another 1.5 V dc, resulting in 334 to 335 V dc. The load regulation is good, even in this open loop design, because the current capacity of the power stage is much greater than the required load current.

The input circuit breaker provides inrush current protection as well as over current protection. During current limiting, the breaker modulates a series pass FET on and off to limit power dissipation. The PSFD is hot pluggable and will not disturb other sensitive loads if it is connected to an operating P28 V dc bus. If a circuit failure and short circuit occur downstream of the circuit breaker, the fast acting circuit breaker prevents this short from propagating onto the 28 V dc bus. An EMI filter reduces noise propagation onto the 28 V dc bus. A 33 V transorb, immediately after the input connector, protects the PSFD from voltage transients and momentary reverse bias connections.

The output limiter restricts the output current to 7 mA, even during a direct short. The output can stay shorted indefinitely even in a 65°C (149 °F) ambient. A 385 V MOV provides transient protection at the output.

18.19.4 Specifications

Item	PSFD Specification
Maximum Input Voltage	29.4 V dc
Under Voltage Lockout (UVLO) Range	22.1 – 26.4 V dc
Inrush Current Limit	550 mA for 40 uS, 300 mA steady state
Startup Time at Full Load, 28 V dc	34 mS
Input Current at Full Load, 28 V dc	137 mA
Input Current Ripple at Full Load, 28 V dc	66 mA at 50 kHz
Power Consumption at Full Load, 28 V dc	4.1 W
Maximum Power Consumption at Full Load, 29.4 V dc input	4.5 W
Full Load Output	5 mA
Output Short Circuit Current Limit with Self Recovery	7 mA
Minimum Output Voltage, Full Load, 26.6 V dc Input	317 V dc
Output Voltage at Full Load, 28 V dc Input	333 V dc
Maximum Output Voltage, No Load, 29.4 V dc Input	355 V dc
Output Over Voltage Protection	385 V MOV
Efficiency at Full Load	0.4
Load Regulation	-0.005
Typical Output Ripple at Full Load	520 m Vp-p at 50 kHz
Line Regulation	0.11
Nominal Switching Frequency	25 ±6 kHz
Test Point Attenuation of 335 V dc	100:1 Referenced to case
Voltage Isolation, Output to Input	1700 V dc
Dimensions	8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in x 1.65 in x 4.78 in)
Ambient Rating for Enclosure Design†	-30 to 65ºC (-22 to 149 ºF)
Assembly Technology	Surface mount

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

18.19.5 Diagnostics

18.19.5.1 Test Points

The output voltage can be monitored locally using a differential pair of test points. The positive and negative test points connect to the positive and negative outputs through 100:1 attenuators which are referenced to the chassis for safety. Each test point can be touched without risk or electrical shock. Furthermore, each test point can be shorted to the chassis indefinitely. The test points are designated TP_POS (inboard) and TP_NEG (outboard). The test points are accessed by rotating the round plastic cover on the top.

18.19.5.2 Status LEDs

The PSFD displays three status LEDs:

- Current Limit, Red, DS3 – activates at 6-7 mA.
- P335 Out, Green, DS2 – high voltage may be present at the output. A precise voltage level cannot be discerned from this LED.
- P28 In, Green, DS1 – voltage is present at the input. A precise voltage level cannot be discerned from this LED.

The input and output LEDs do not indicate any particular voltage level and simply annunciate the presence of input or output voltage. Similarly, the current limit LED is for indication only and does not provide a measurement of the over current magnitude. The current limit LED is in series with the signal path for the activation signal. In the event that the current limit LEDs fails open, a circuit bypasses the LED and the limiter continues to function.

18.19.5.3 Output Voltage

The output voltage from each PSFD is attenuated and sensed on the TRPG terminal board. The sensed voltage is monitored by the PTUR I/O pack. In a TMR configuration, if any of the three PSFD fails to provide 335 V dc, an alarm is annunciated in the ToolboxST application or Alarm Viewer.

19 Common I/O Module Functionality

19.1 BPPx Processor

The BPPx processor board is used with most Ethernet-based I/O modules. It contains the following:

- High-speed processor with RAM and flash memory
- Two fully independent 10/100 Ethernet ports with connectors
- Hardware watchdog timer and reset circuit
- Internal temperature sensor
- Status-indication LEDs
- Electronic ID and the ability to read IDs on other boards
- Input power connector with soft start and current limiter
- Local power supplies

The processor board connects to an acquisition board specific to the I/O module function. When input power is applied, the soft-start circuit ramps up the voltage available on the processor board. The local power supplies are sequenced on, and the processor reset is removed. The processor completes self-test routines, and then loads application code specific to the I/O module type from flash memory.

The processor reads board ID information to ensure the correct matching of firmware, acquisition board, and terminal board. With a good match, the processor attempts to establish Ethernet communications, starting with request of a network address. The address request uses the industry standard dynamic host configuration protocol (DHCP) and the unique identification read from the acquisition and terminal boards. After Ethernet initialization, the processor programs the on-board logic, runs the application, and enables the acquisition board to begin operation. This network redundancy function is more tolerant of faults than a classic HotBackup where the second port is only used after a primary port failure.

The processor application code contains all the logic necessary to allow the I/O module to operate from one or two Ethernet inputs. When operated from two Ethernet inputs, both network paths are active all the time. A failure of either network will not result in any disturbance to the I/O module operation, and the failure is indicated through the working network connection. The Ethernet ports on the processor auto-negotiate between 10 and 100 Mbps speed, and between half-duplex and full-duplex operation.

Note The PFFA, PAMC, and PPNG have different internal processor boards.

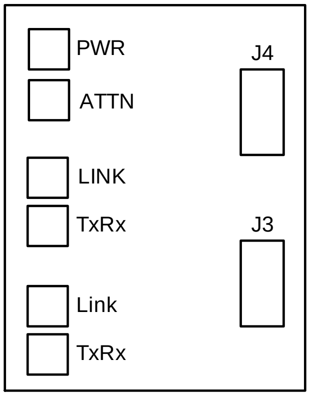
19.1.1 Power Management

The processor includes power management of its 28 V input circuit. The management function provides soft start to control current inrush during power application. After applying power, the circuit provides a fast current limit function to prevent a failure from propagating back onto the 28 V power system. When power is present and working properly, the green PWR LED is lit. If the current limit function operates, the PWR LED will be out until the problem is cleared.

19.1.2 ID Line

The processor board and acquisition board(s) within the I/O pack contain electronic ID parts that are read during power initialization. A similar part located with each terminal board pin connector allows the processor to confirm correct matching of I/O pack to terminal board and report board revision status to the Mark VIe or Mark VIeS controller.

19.1.3 BPPx Processor LEDs



Processor LEDs

Color	Label	Description
Green	PWR	Displays the presence of control power
Green	LINK	Provided for each Ethernet port to indicate if a valid Ethernet connection is present
Yellow	TxRx	Provided for each Ethernet port to indicate when the I/O module is transmitting or receiving data over the port
Red and Green	ATTN	Displays I/O module status

Flash Codes for All Mark VIe I/O Packs and BPPC-based Mark VIeS I/O Packs

LED	Flashing Pattern	Description
Red ATTN	Solid	Booting - prior to reading board ID
	4 Hz 50%	Diagnostic alarm active
	2 Hz 50%	Awaiting an IP address
	1 Hz 50%	No firmware to load (Program mode)
	0.5 Hz 50%	Application code not loaded to the I/O module
	LED out	Initializing, no problems detected
	Two 4 Hz pulses every 4 sec	Application online
Green ATTN	Solid	BIOS (at power on), but if it remains in this state, the I/O module is not functioning properly and should be replaced
	2 Hz 50%	Awaiting Auto-Reconfiguration release
	1 Hz 50%	I/O module in WAIT or STANDBY
	Two 4 Hz pulses every 4 sec	Application online

Flash Codes for BPPB-based Mark VIeS I/O Packs

LED	Flashing Pattern	Description
Red ATTN	LED out	There are no detectable problems with the I/O pack.
	LED solid on	A critical fault is present that prevents the I/O pack from operating. There could be hardware failures on the processor or acquisition boards, or there is not any application code loaded.
	4 Hz 50%	An alarm condition is present in the I/O pack. These alarms include: wrong I/O pack/terminal board combination, terminal board is missing, or errors in loading the application code.
	1.5 Hz 50%	The I/O pack is not online.
	0.5 Hz 50%	This is used during factory testing.
	Two 4 Hz pulses every 4 sec	Application online

19.2 Mark VIe TBSW Terminal Board Disconnect Switch

Many of the terminal boards in the Mark VIe control use a 24-position pluggable barrier terminal block (179C9123BB). These terminal blocks have the following features:

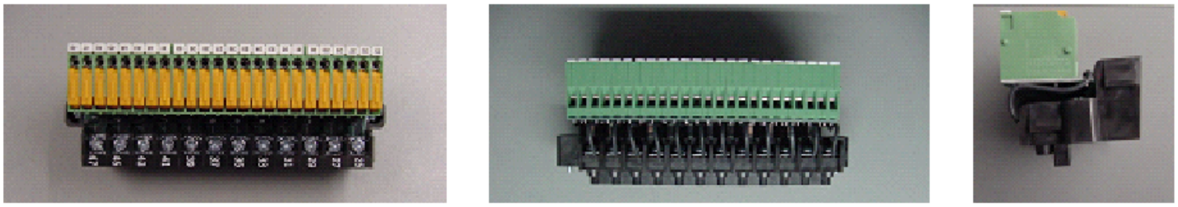
- Made from a polyester resin material with 130°C (266 °F) rating
- Terminal rating is 300 V, 10 A, UL class C general industry, 0.375 inch creepage, 0.250 inch strike or clearance
- UL and CSA code approved
- Screws finished in zinc clear chromate and contacts in tin
- Each block screw is number labeled 1 through 24 or 25 through 48 in white
- Recommended screw tightening torque is 8 in-lbs

The Mark VIe control Terminal Board Disconnect Switch (TBSW) provides individual disconnect switches for each of the 48 customer I/O points on the Mark VIe control terminal. This facilitates procedures such as continuity checking, isolation for test, and others. Two TBSW assemblies are required for each terminal board: one numbered 1-24, the other numbered 25-48, (GE part numbers 336A4940CHG1 and 336A4940CHG2, respectively). The TBSW fits and connects into the terminal board 24-point pluggable barrier terminal block receptacles.

Caution

The TBSW is not to be used for live circuit interruption. The circuit must be de-energized before it is either closed or opened by the TBSW.

The TBSW is designed for continuous 5 A rms current at 300 V rms and complies with EN61010-1 clearance specifications. The NEMA power/voltage class rating (A, E, F, G) for the TBSW is dependent on the terminal board the TBSW is mounted upon.



Top View Front View Side View

TBSW Mounted to Terminal Block

The following table lists the TBSW terminal board applications for the Mark VIe control. An *OK* in the column *TBSW Applications* indicates an approved application of the TBSW with regards to specifications for voltage and current. Those board points that require limiting the terminal board applications are indicated with a *Note #*.

TBSW Terminal Board Applications

Board	Type	TBSW Applications	
		CSA	NEMA
TBTCH1B TBTCH1C	Thermocouples	OK	OK
TRTDH1D TRTDH2D	RTDs	OK	OK
TBAIH1C	Analog inputs	OK	OK
TBAOH1C	Analog outputs	OK	OK
TBCIH1C TBCIH2C TBCIH3C TBCIH4C	Contact inputs	OK	OK
TICIH1A TICIH2A	Contact inputs	Note 1	Note 2
TRLYH1B TRLYH1C TRLYH2C TRLYH1D	Contact outputs	Note 1	Note 2
TSVCH1A TSVCH2A	Servo I/O	OK	OK
TTURH#C	Turbine I/O	OK	OK
TRPG		Note 3	Note 3
TREGH#B		OK	OK
TRPL		OK	OK
TREL		OK	OK
TRPS		OK	OK
TRES		OK	OK
TPROH1C TPROH2C		OK	OK
TVBAH1A TVBAH2A		OK	OK
TGNA		OK	OK

Table Notes

1. The inputs on the TICI and TRLY boards are high voltage isolated inputs. The TBSW is classified by CSA for use up to 300 V rms. Circuits applied to the TICI or TRLY terminal board with the TBSW installed must be externally limited to 300 V rms. Care must also be taken to assure that no adjacent circuits, that when both are operating, do not exceed 300 V rms between them.

2. NEMA Standards Publication No. ICS 1, Industrial Control and Systems - General Requirements

NEMA Clearance and Creepage distances are given according to the power and voltage limiting abilities of the circuit. The TICI and TRLY terminal boards carry no components that are designed to limit voltage or current. For this reason, the TBSW application limitations for these two terminal boards will depend on the customer's ability to install voltage and current limiting devices on the TBSW circuits according to NEMA guidelines. The following chart indicates the NEMA class and the voltage it must be limited too before it can be applied to the TBSW. Voltages are for circuit voltage, and circuit to adjacent circuit voltage.

Group	Voltage	Description
A	50 V rms or DC	All circuits which cannot be otherwise classified. Use this rating when no external current and voltage limiting devices are present.
E	225 V pk	Transient voltages are known and controlled.
F	300 V pk	Transient voltages are known and controlled, and the power supplying the circuit is limited to a short circuit current of 10 k VA or less.
G	300 V pk	Transient voltages are known and controlled, and the power supplying the circuit is limited to a short circuit current of 500 VA or less.

3. The TRPG require a 335 V dc circuit. The TBSW is classified by CSA and NEMA for use up to 300 V rms. Circuits applied to the TRPG terminal board with the TBSW installed must be must be limited to 300 V rms, disallowing the use of the TBSW during normal operation.

19.3 I/O Module Common Diagnostic Alarms

The following alarms are common, but not all of these alarms are applicable for every I/O module.

0

Description Diagnostic Alarm Reset

Possible Cause N/A

Solution N/A

2

Description Flash memory CRC failure

Possible Cause
During commissioning or maintenance:

- A firmware programming error occurred. The I/O pack or module did not go online with the controller.

During normal operation:

- The hardware failed.

Solution
During commissioning or maintenance:

- Rebuild the system, then download the application and the configuration to the I/O pack or module.

During normal operation:

- Replace the I/O pack or module.

3

Description CRC failure override is active

Possible Cause
During commissioning or maintenance:

- A firmware programming error occurred. The I/O pack or module did not go online with the controller.

During normal operation:

- The hardware failed.

Solution
During commissioning or maintenance:

- Rebuild the system, then download the application and the configuration to the I/O pack or module.

During normal operation:

- Replace the I/O pack or module.

4

Description I/O pack in stand alone mode

Possible Cause

During commissioning or maintenance:

- The I/O pack or module configuration is invalid.

During normal operation:

- The hardware failed.

Solution

During commissioning or maintenance:

- Rebuild the system, then download the application and the configuration to the I/O pack or module.

During normal operation:

- Replace the I/O pack or module.

5

Description I/O pack in remote I/O mode

Possible Cause

During commissioning or maintenance:

- The I/O pack or module configuration is invalid.

During normal operation:

- The hardware failed.

Solution

During commissioning or maintenance:

- Rebuild the system, then download the application and the configuration to the I/O pack or module.

During normal operation:

- Replace the I/O pack or module.

6

Description Special User Mode active. Now: [ ]

Possible Cause

During commissioning or maintenance:

- The I/O pack or module configuration is invalid.

During normal operation:

- The hardware failed.

Solution

During commissioning or maintenance:

- Rebuild system, then download the application and the configuration to the I/O pack or module.

During normal operation:

- Replace the I/O pack or module.

7

Description The I/O pack has gone to the Offline state

Possible Cause
During commissioning or maintenance:

- Ethernet cable disconnected or connected to wrong port

During normal operation:

- Controller is offline or restarted.
- Faulty Ethernet switch/cable

Solution
During commissioning or maintenance:

- Check the Ethernet cable.

During normal operation:

- Verify that the controller is not offline.
- Replace the Ethernet switch/cable.

16

Description System limit checking is disabled

Possible Cause System checking disabled by configuration

Solution System checking was disabled by the configuration.

20

Description ToolboxST application detects unhealthy link or loss of communication between [ ] and controller

Possible Cause

- I/O pack or module did not complete start up
- I/O pack or module configuration files missing
- I/O pack or module restarted
- I/O pack or module configured for dual networks, but only one network is connected
- Network issue preventing ToolboxST application connection
- Power failure to the I/O pack or module
- Terminal board barcode typed incorrectly in the ToolboxST configuration
- Wrong terminal board is configured in the ToolboxST application
- I/O pack or moduleis plugged into wrong jack on terminal board, or wrong jack number is configured in the ToolboxST application
- I/O pack or module configured in ToolboxST application, but configuration not downloaded to the controller
- I/O pack or module in program mode

Solution

- If the ToolboxST communication is working correctly, any additional diagnostics should indicate the cause of the problem.
- Perform a build and download parameters to the I/O pack or module.
- Download firmware and parameters to the I/O pack or module.
- Verify that the Ethernet cables and network switch are operating correctly.
- Verify that the I/O pack configuration (such as Type, HW Form, Bar Code, position) matches the actual hardware.
- Manually restart the I/O pack or module.
- Perform a build and download the configuration to the controller, wait for I/O pack communication status to change, then scan and download to the I/O pack.

Note This alarm is not reported to the WorkstationST Alarm Viewer. This alarm is generated by the ToolboxST application, not by the I/O pack or module.

21

Note This alarm is obsolete.

Description Control/Status communication failure between [ ] and controller

Possible Cause

- Asynchronous Drive Language (ADL) communication unhealthy
- Terminal board barcode is typed incorrectly in the ToolboxST configuration
- Wrong terminal board is configured in the ToolboxST application
- I/O pack or module is plugged into the wrong Jack on the terminal board, or the wrong jack number is configured in the ToolboxST application
- I/O pack or module is configured in the ToolboxST application, but the configuration is not downloaded to the controller
- I/O pack or module is in program mode

Solution

- Verify that the I/O pack or module configuration (such as Type, HW Form, Bar Code, position) matches the actual hardware.
- Perform a build and download the configuration to the controller, wait for communication status to change, then scan and download to the I/O pack or module.
- Manually restart the I/O pack or module.

22

Description ToolboxST application detects a diagnostic status signal (...L3DIAG, ATTN, and/or LINK_OK...) is [ ]; therefore, diagnostic status for this I/O module may be inaccurate, unknown, or indeterminate

Possible Cause

- I/O pack or module status signal quality is in warning state
- Signal quality is unhealthy, forced, or being simulated
- Status information is inaccurate

Solution

- Check status signal health
- Remove the force or simulated condition that is applied to the status signal.

Note This alarm is not reported to the WorkstationST Alarm Viewer. This alarm is generated by the ToolboxST application, not by the I/O pack or module.

23

Description ToolboxST application detects a major difference in [ ] controller application code

Possible Cause

- Compressing variables, EGD pages, distributed I/O, or NVRAM
- Changing frame or background period
- Changing controller or network redundancy
- Changing controller platform or NTP client mode
- Changing controller host name or IP address
- Changing IONet IP address
- Adding/removing first/last linking device (PFFA), respectively
- Removing a WCBM module
- Changing from multicast to broadcast (vice-versa) I/O communication
- Adding the first shared I/O module or connecting the first Controller to Controller I/O variable
- Removing the last Modbus Slave point
- Disabling controller web pages
- Disabling Wind Compress Data Log
- Disabling Wind Farm Management System

Solution Rebuild the controller and download.

Note This alarm is not reported to the WorkstationST Alarm Viewer. This alarm is generated by the ToolboxST application, not by the I/O pack or module.

24

Description ToolboxST application cannot retrieve diagnostics information from I/O pack [ ]

Possible Cause

- Cannot get the requested information from I/O pack or module.
- Communication program failure
- I/O pack or module unable to retrieve the IP address
- Terminal board barcode is typed incorrectly in the ToolboxST configuration
- Wrong terminal board is configured in the ToolboxST application
- I/O pack or module is plugged into the wrong Jack on the terminal board, or the wrong jack number in the ToolboxST configuration
- I/O pack or module is configured in the ToolboxST application, but the configuration is not downloaded to the controller
- I/O pack or module is in program mode
- I/O pack or module not able to load firmware
- Power failure to the I/O pack or module

Solution

- Verify that the I/O pack or module configuration (such as Type, HW Form, Bar Code, position) matches the actual hardware.
- Perform a build and download the configuration to the controller, wait for communication status to change, then scan and download to the I/O pack or module.
- Manually restart the I/O pack or module.
- Check the network cables for proper connection.
- Verify that the switch is functioning correctly.

Note This alarm is not reported to the WorkstationST Alarm Viewer. This alarm is generated by the ToolboxST application, not by the I/O pack or module.

25

Note This alarm is obsolete.

Description Control/Status communication Error: [ ]

Possible Cause

- Cannot get diagnostic information from I/O pack or module
- I/O pack or module is not able to load firmware

Solution

- Check the I/O pack or module configuration.
- Rebuild the application and download the firmware and the application to the I/O pack or module.
- Check the network cables for proper connection.
- Verify that the switch is functioning correctly.

30

Description Firmware/Configuration Incompatibility Error;Firmware: [ ] Config: [ ]

Possible Cause I/O pack or module configuration files are incompatible with the firmware. Files have wrong revision.

Solution

- Confirm the correct installation of the ToolboxST application.
- Verify that each I/O pack or module is upgraded to the latest version by right-clicking each I/O pack or module and selecting Upgrade.
- Rebuild the application and download the firmware and the application code to the affected I/O pack or module.

31

Note This alarm is obsolete.

Description Firmware/IO Configuration Incompatibile;Firmware: [ ] IO Config: [ ]

Possible Cause

- I/O pack or module configuration files are incompatible with the firmware.
- The files have the wrong revision.

Solution

- Confirm the correct installation of the ToolboxST application.
- Verify that each I/O pack or module is upgraded to the latest version by right-clicking each I/O module and selecting Upgrade.
- Rebuild the application, and download the firmware and application code to the affected I/O pack or module.

256

Description [ ]V Pwr supply voltage is low

Possible Cause Input voltage dropped below 18 V. I/O pack or module input power is required to be within range 28 V ±5%. I/O pack or module operation will be compromised or may stop completely.

Solution

- If PPDA is available to monitor control cabinet power, check the I/O pack or module for active alarms.
- Check the I/O pack or module power within the control cabinet; begin with power supplies and work toward the affected I/O pack or module.

257

Description [ ]V Pwr supply voltage is low

Possible Cause

- For BPPB-based I/O packs, input voltage has dropped below 26.5 V. Input voltage is required to be within the range 28 V ±5%.
- For BPPC-based I/O packs, input voltage has dropped below 24 V. Input voltage is required to be within the range 24 V ±10%.

Note In most cases, normal pack operation continues below this voltage, but field devices that require 24 V from the terminal board may begin to experience reduced voltage operation with undetermined results.

Solution

- If PPDA is available to monitor control cabinet power check the I/O pack or module for active alarms.
- Check I/O pack or module power within the control cabinet; begin with power supplies and working toward the affected I/O pack or module.

258

Description Temperature [ ] °F is out of range ([ ] to [ ] °F)

Possible Cause

- Temperature went outside -35°C to 66°C (-31 to 151 °F) limits for PCNO or PPRF.
- Temperature went outside -40°C to 90°C (-40 to 194 °F) limits for Mark VIe BPPC-based I/O modules.
- Temperature went outside -35°C to 85°C (-31 to 185 °F) limits for BPPB-based I/O modules, and for Mark VIeS Safety I/O modules.

Solution Check the environmental controls for the cabinet containing the I/O pack. The I/O pack does continue to operate beyond these temperature limits, but long-term operation at elevated temperatures may reduce equipment life.

259

Description Application Runtime Error - [ ] Frame overruns occurred

Possible Cause Overloaded processor sequencer malfunction (one or more frame overruns occurred)

Solution

For a controller, do the following to increase the frame idle time:

- Reduce the application or increase the EGD period.
- Upgrade the controller to one with a faster processor.
- Replace the controller.

For an I/O module, do the following:

- From the ToolboxST application, rebuild the system, then download the application and configuration to the I/O module.
- Replace the I/O module.

260

Description Application Runtime Error - [ ] Frame skips occurred

Possible Cause There is an overloaded processor or a processor malfunction. Frame number skips were detected. The frame number should monotonically increase during Controlling state.

Solution

For a controller, do the following:

- Reduce the application or increase the EGD period to reduce the processor load.
- Upgrade the controller to one with a faster processor.
- Replace the controller.

For an I/O module, do the following:

- From the ToolboxST application, rebuild the system, then download the application and configuration to the I/O module.
- Replace the I/O module.

261

Description Unable to read configuration file from flash

Possible Cause

During commissioning or maintenance:

- The I/O pack or module does not have the correct configuration file stored in its flash file system.
- There is a hardware problem.

During normal operation:

- There is a hardware failure.

Solution

During commissioning or maintenance:

- Confirm the correct installation of the ToolboxST application.
- Rebuild the system and download the application and the configuration to the I/O pack or module.

During normal operation:

- Replace the I/O pack or module.

262

Description Bad configuration file detected

Possible Cause

During commission/maintenance:

- The configuration file in the I/O pack or module is not compatible with loaded application code

During normal operation:

- There is a hardware failure

Solution

During commissioning or maintenance:

- Rebuild the system and download the application and the configuration to the I/O pack or module.

During normal operation:

- Replace the I/O pack or module.

263

Note This alarm is obsolete.

Description Invalid configuration file

Possible Cause

During commissioning or maintenance:

- The downloaded configuration file is for a different type of I/O module.

During normal operation:

- There is a hardware failure.

Solution

During commissioning or maintenance:

- Rebuild the control system and download the application and configuration to the I/O module.

During normal operation:

- Replace the I/O pack.

264

Note This alarm is obsolete.

Description Firmware/Configuration Incompatibility Error

Possible Cause

- I/O pack or module configuration files are incompatible with the firmware.
- The files have the wrong revision.

Solution

- Confirm the correct installation of the ToolboxST application.
- Verify that each I/O pack or module is upgraded to the latest version by right-clicking each I/O pack and selecting *Upgrade*.
- Rebuild the application, and download the firmware and application code to the affected I/O pack or module.

265

Description Configuration file load error - invalid I/O header size

Possible Cause

During commissioning or maintenance:

- Build error
- Controller EGD revision code is not supported
- Incompatible version of the I/O pack or module firmware was downloaded

During normal operation:

- There is a hardware failure.

Solution

During commissioning or maintenance:

- Confirm the correct installation of the ToolboxST application.
- Verify that each I/O pack or module is upgraded to the latest version by right-clicking each I/O pack and selecting *Upgrade*.
- Rebuild the application, and download the firmware and application code to the affected I/O module.

During normal operation:

- Replace the I/O pack or module.

266

Description Configuration file load error - invalid file length

Possible Cause

During commissioning or maintenance:

- The configuration file in the I/O pack or module does not have the correct size to match the application code that is loaded.

During normal operation:

- Hardware failure

Solution

During commissioning or maintenance:

- Confirm the correct installation of the ToolboxST application. Rebuild the application and download the firmware and the application code to the affected I/O pack or module.

During normal operation:

- Replace the I/O pack or module.

267

Description Firmware Load Error

Possible Cause

During commissioning or maintenance:

- Incompatible version of firmware downloaded

During normal operation:

- There is a hardware failure.

Solution

During commissioning or maintenance:

- Confirm the correct installation of the ToolboxST application.
- Ensure that each I/O pack or module is upgraded to the latest version. From the ToolboxST application, right-click each I/O pack or module and selecting **Upgrade**.
- Rebuild the application and download the firmware and the application code to the affected I/O pack or module.

During normal operation:

- Replace the I/O pack or module.

268

Description Firmware Load Error - Incompatible FPGA Revision: Found [ ] Need [ ]

Possible Cause
During commissioning or maintenance:

- Incompatible version of firmware downloaded

During normal operation:

- There is a hardware failure.

Solution
During commissioning or maintenance:

- Confirm the correct installation of the ToolboxST application.

During normal operation:

- Verify that each I/O pack or module is upgraded to the latest version by right-clicking each I/O pack or module and selecting Upgrade.
- Rebuild the application and download the firmware and the application code to the affected I/O pack or module.
- Replace the I/O pack or module.

269

Note This alarm is obsolete.

Description EGD communication Initialization Failure

Possible Cause Internal runtime error

Solution

- Restart the I/O pack or module.
- Upgrade the I/O pack or module firmware and application code.
- If the problem persists, replace the I/O pack or module.

270

Note This alarm is obsolete.

Description EGD communication terminated

Possible Cause Internal runtime error

Solution

- Restart the I/O pack or module.
- Upgrade the I/O pack or module firmware and application code.
- If the problem persists, replace the I/O pack or module.

271

Description Internal communication error - Exchange [ ] Export failed

Possible Cause
During commissioning or maintenance:

- I/O pack or module does not have correct configuration file stored in flash file system
- Internal runtime error

During normal operation:

- Internal runtime error

Solution
During commissioning or maintenance:

- From the ToolboxST application, confirm the correct configuration of the I/O pack or module.
- Rebuild the system, and download the application and configuration to the I/O pack or module.

During normal operation:

- Restart the I/O pack or module.
- If problem persists, replace the I/O pack or module.

272

Note This alarm is obsolete.

Description Internal EGD communication error - Exchange [ ] Import failed.

Possible Cause Internal runtime error

Solution

- Restart the I/O pack or module.
- Upgrade the I/O pack or module firmware and application code.
- If the problem persists, replace the I/O pack or module.

273

Note This alarm is obsolete.

Description Unsupported EGD message - Invalid EGD version

Possible Cause EGD protocol version incorrect, greater than current version

Solution

- Restart the I/O pack or module.
- Upgrade the I/O pack or module firmware and application code.
- If the problem persists, replace the I/O pack or module.

274

Note This alarm is obsolete.

Description IONET-EGD - Received Redundant Exchange from unknown address

Possible Cause Controller received EGD message from unknown address

Solution

- Restart the I/O pack or module.
- Upgrade the I/O pack or module firmware and application code.
- If the problem persists, replace the I/O pack or module.

275

Note This alarm is obsolete.

Description IONET-EGD - Out of order Exchange [ ] from Producer [ ], Rcvd [ ], Last [ ]

Possible Cause Message sequence number was out of order, less than required

Solution

- Restart the I/O pack or module.
- Upgrade the I/O pack or module firmware and application code.
- If the problem persists, replace the I/O pack or module.

276

Note This alarm is obsolete.

Description IONET-EGD - UNHEALTHY (Bad Configuration Time) Producer [ ], Exchange [ ]

Possible Cause Message version mismatch

Solution

- Restart the I/O pack or module.
- Upgrade the I/O pack or module firmware and application code.
- If the problem persists, replace the I/O pack or module.

277

Note This alarm is obsolete.

Description IONET-EGD - Exchange [ ] Signature mismatch from Producer [ ], expected [ ], received [ ]

Possible Cause Message version mismatch

Solution

- Restart the I/O pack or module.
- Upgrade the I/O pack or module firmware and application code.
- If the problem persists, replace the I/O pack or module.

278

Note This alarm is obsolete.

Description IONET-EGD - Producer [ ] gave bad length Exchange [ ], expected [ ], got [ ]

Possible Cause Exchange message wrong length

Solution

- Restart the I/O pack or module.
- Upgrade the I/O pack or module firmware and application code.
- If the problem persists, replace the I/O pack or module.

279

Description Could not determine platform type from hardware

Possible Cause

- During commissioning or maintenance, there is an incorrect firmware version or hardware malfunction (firmware could not recognize host hardware type)
- During normal operation, there is a hardware failure

Solution

- Verify that all connectors are aligned properly and fully seated.
- Check the firmware version for compatibility with platform. If it is correct, replace the I/O pack or module.

280

Description Platform hardware does not match configuration

Possible Cause

- During commissioning or maintenance, the platform type identified in the application configuration does not match actual hardware
- During normal operation, there is a hardware failure

Solution

- From the **General** tab, select **General Properties**, and **Platform** and fix the platform type.
- Rebuild and download the application.
- If the problem persists, replace the I/O pack or module.

281

Description Firmware Load Error - FPGA not programmed due to platform errors

Possible Cause File downloaded to configure the Field Programmable Gate Array (FPGA) not successfully applied

Solution

- Verify that all connectors are aligned properly and fully seated.
- Check the firmware version for compatibility with platform. If it is correct, replace the I/O pack or module.

282

Description Firmware Load Error - application independent processes failed to initialize

Possible Cause Runtime malfunction. An application-independent firmware process could not be started successfully.

Solution

- Reload firmware and application and restart.
- Controller: If the failure persists, remove the Compact Flash module and reprogram the boot loader using the ToolboxST configuration. Download using the Device | Download | Controller setup | Format Flash selection. After reinstalling the flash module and restarting, reload the firmware and application.
- Replace the module.
- I/O pack or module: Re-download the base load.

283

Description Firmware error - Internal process crashed

Possible Cause Runtime or hardware malfunction (runtime process failed)

Solution

- Reload firmware and application and restart.
- Re-download the baseload and the firmware.

284

Description Firmware error - Internal process failed

Possible Cause Runtime or hardware malfunction (runtime process failed)

Solution

- Reload the firmware and application, and restart the controller and/or I/O module.
- Re-download the baseload and the firmware.
- If this does not work, replace the I/O module or controller.

285

Description Unexpected reboot occurred - hardware fault

Possible Cause

- Runtime or hardware malfunction
- Runtime process stalled

Note This diagnostic alarm is detected on a processor startup after the processor or hardware has malfunctioned and caused a processor to reboot. Therefore, the diagnostic alarm timestamp may be delayed from when the actual fault occurred.

Solution

- Reload firmware and application and restart.
- If the problem persists, replace the processor module.

292

Description Application Error - application overrunning the frame

Possible Cause Application cannot start within frame.

Solution Check application loading and reduce the amount of application code or frequency of execution. Build application and download to all controllers.

293

Description Waiting on IP addr Ionet [ ] before continuing

Possible Cause I/O pack or module waiting to obtain network address from the controller using DHCP

- Network problem
- Controller problem
- I/O pack or module not configured correctly, or incorrect ID (barcode)
- I/O pack or module is configured with 2 network addresses in the ToolboxST application, but only has one network physically connected.

Solution

- Verify that the controller is online.
- Confirm that the correct terminal board ID is present in the ToolboxST configuration.
- Check IONet (switches, cables).
- From the ToolboxST application, verify that the I/O pack or module network configuration matches the physical network configuration.

295

Description IOPACK - The FPGA is not generating an I/O interrupt

Possible Cause There is a FPGA inside the I/O pack or module that controls I/O or module hardware. The logic in the FPGA generates an interrupt to the processor requesting that the I/O or module be serviced. That interrupt is not occurring as expected.

Solution Rebuild system and download to the I/O pack or module. If the problem persists, replace the I/O pack.

300

Description Application Code Load Failure

Possible Cause
During commissioning or maintenance:

- Invalid application configuration

During normal operation:

- There is a firmware or hardware malfunction

Solution

- Rebuild and download the application to all processors.
- Reload the firmware and application.
- If the problem persists, replace processor module.

301

Description Configuration Load Failure

Possible Cause

- I/O pack or module I/O configuration files missing
- I/O pack or module reseated on the terminal board (clears configuration from I/O pack or module)

Solution

- Rebuild and download the application to all the processors.
- Reload the firmware and application.
- If the problem persists, replace processor module.

338

Description Pack Firmware Error - Inputs are not being updated

Possible Cause

During commissioning or maintenance:

- The I/O pack or module application process is not providing system signal inputs to EGD every frame.

Solution

During commissioning or maintenance:

- Rebuild and download the firmware and the application.
- Verify that the idle time is adequate for the I/O pack or module and that the frame rate does not exceed defined limits.
- If the problem persists, replace the I/O pack or module.

339

Description Outputs are not being received

Possible Cause

- I/O pack or module not receiving outputs from the controller after previously receiving outputs
- Controller is restarting or has restarted
- Failed Ethernet connection between the I/O pack or module and controller
- Internal firmware failure

Solution

- Check for disconnected IONet cables or malfunctioning network switches.
- Verify that the controller is online and operating correctly.
- Rebuild and download the firmware and configuration to the I/O pack or module.

340

Description Memory Verification failed - Data structures

Possible Cause Hardware memory failure (data that should not change after I/O pack or module has gone online has been modified)

Solution

- Rebuild and download the application to all affected I/O packs or modules.
- Reload the firmware and application code.
- If problem persists, replace the I/O pack or module.

341

Note This alarm is obsolete.

Description Firmware or I/O Configuration Incompatibility

Possible Cause I/O pack or module configuration files incompatible with firmware (files do not contain necessary revision)

Solution

- Confirm the correct installation of the ToolboxST software.
- Verify that each I/O pack or module is upgraded to the latest version by right-clicking each I/O pack or module and selecting *Upgrade*.
- Rebuild the application, and download the firmware and application code to the affected I/O pack or module.

342

Description Firmware or Configuration Incompatible

Possible Cause I/O pack or module configuration files incompatible with firmware (files do not contain necessary revision)

Solution

- Confirm the correct installation of the ToolboxST application.
- Verify that each I/O pack or module is upgraded to the latest version by right-clicking each I/O pack and selecting *Upgrade*.
- Rebuild the application, and download the firmware and application code to the affected I/O pack or module.

343

Description Memory Verification failed - Firmware Libraries

Possible Cause Hardware memory failure (data that should not change after the I/O pack or module has gone online was modified)

Solution

- Rebuild and download the application to all affected I/O packs or modules.
- Reload the firmware and application code.
- If the problem persists, replace the I/O pack or module.

348

Description Intermittent communications on IONet1 - Packet loss exceeded [ ]

Possible Cause

- Power cycled on I/O producer (controller or I/O pack or module)
- IONet malfunction
- I/O message corruption
- Communication errors occurred on more than 5% of data transmissions on IONet1

Solution

- Check for evidence of pack restart (diagnostic alarms, error logs).
- Faulty Ethernet cable from pack to network switch and/or from switch to controller. Replace cable(s).
- Replace the I/O pack or module.
- Faulty network switch; place the I/O pack or module's Ethernet cable into an empty port. If problem persists, replace the network switch.

349

Description Intermittent communications on IONet2 - Packet loss exceeded [ ]

Possible Cause

- Power cycled on I/O producer (controller or I/O pack or module)
- IONet malfunction
- I/O message corruption
- Communication errors occurred on more than 5% of data transmissions on IONet2

Solution

- Check for evidence of pack restart (diagnostic alarms, error logs).
- Faulty Ethernet cable from pack to network switch and/or from switch to controller. Replace cable(s).
- Replace the I/O pack or module.
- Faulty network switch; place the I/O pack or module's Ethernet cable into an empty port. If problem persists, replace the network switch.

350

Description Intermittent communications on IONet3 - Packet loss exceeded [ ]

Possible Cause

- Power cycled on I/O producer (controller or I/O pack or module)
- IONet malfunction
- I/O message corruption
- Communication errors occurred on more than 5% of data transmissions on IONet3

Solution

- Check for evidence of pack restart (diagnostic alarms, error logs).
- Faulty Ethernet cable from pack to network switch and/or from switch to controller. Replace cable(s).
- Replace the I/O pack or module.
- Faulty network switch; place the I/O pack or module's Ethernet cable into an empty port. If problem persists, replace the network switch.

351

Description Internal Firmware error - Thread [ ] timing overrun

Possible Cause An application task scheduled with a scan rate either occurred twice as fast or twice as slow as the expected rate.

Solution

- Check the idle time on the I/O pack or module, and verify that the frame rate is correct.
- Reload the firmware and application code.
- If the problem persists, replace the I/O pack or module.

357

Description Internal Runtime error - Sequencer out-of-order or overrun detected

Possible Cause There is a possible hardware malfunction. Sequencer critical clients were scheduled out of order or were overrun. This alarm occurs following three successive frames of sequencer critical client out-of-order detections. After five, the I/O module is put into the FAILURE control state.

Solution Replace the I/O module.

358

Description Internal Runtime error - Sequencer client execution underrun

Possible Cause Possible hardware malfunction. Sequencer critical client underrun detected. Alarm occurs after a sequencer critical client has been run slower than its nominal rate three times in a row. After five in a row, the I/O module is put into FAILURE control state.

Solution

- Ignore alarm if it occurs during a restart of the I/O module.
- Replace the I/O module, if the alarm occurs during normal operation.

359

Description Internal Runtime error - Sequencer client execution overrun

Possible Cause Possible hardware malfunction. Sequencer critical client overrun detected. This alarm occurs after a sequencer critical client has been run faster than its nominal, rate three times in a row. After five times in a row, the I/O module is put into FAILURE control state.

Solution

- Ignore this alarm if it occurs during a restart of the I/O module.
- Replace the I/O module, if the alarm occurs during normal operation.

360

Description Internal Runtime error - Sequencer frame period out-of-bounds (±15%)

Possible Cause Possible hardware malfunction. Frame period greater than ±15% of nominal. This alarm occurs following frame period out-of-bounds condition occurring three frames in a row. After five frames in a row, the I/O module is put into FAILURE control state.

Solution

- Ignore this alarm if it occurs during a restart of the I/O module.
- Replace the I/O module, if the alarm occurs during normal operation.

361

Description Internal Runtime error - Sequencer frame state timeout out-of-bounds (±15%)

Possible Cause Possible hardware malfunction. Sequencer frame state timeout greater than ±15% of nominal. This alarm occurs following a sequencer frame state timeout being out-of-bounds for three frames in row. After five frames in a row, the I/O module is put into FAILURE control state.

Solution

- Ignore this alarm if it occurs during a restart of the I/O module.
- Replace the I/O module if the alarm occurs during normal operation.

362

Description Internal Runtime error - Sequencer frame number skip detected

Possible Cause Possible hardware or IONet malfunction. Frame number skips detected. Frame number should monotonically increase until rollover. This alarm occurs following three skips in a row. After five skips in a row, the I/O module is put into FAILURE control state.

Solution

- Ignore alarm if it occurs during a restart of the I/O module.

During normal operation:

- Check for hardware or network switch malfunction.
- Check for loose or defective network cables.
- Replace the I/O module.

363

Description Memory Validation failed - Sequencer data structures

Possible Cause Hardware memory failure (sequencer process data that should not change after the I/O module is online was modified).

Solution Replace the I/O module.

365

Note This alarm is obsolete.

Description EGD communication terminated

Possible Cause Internal runtime error

Solution

- Restart the I/O pack or module.
- Upgrade the I/O pack or module firmware and application code.
- If the problem persists, replace the I/O pack or module.

366

Description Initialization failure - IO firmware

Possible Cause I/O pack or module did not initialize correctly

Solution

- Restart the I/O pack or module.
- Upgrade the I/O pack or module firmware and application code.
- Download the firmware and application code.
- If the problem persists, replace the I/O pack or module.

367

Description Internal communications error - HSSL Comm link down

Possible Cause Internal runtime error

Solution

- Check the High Speed Serial Link (HSSL) cables.
- Upgrade the I/O pack or module firmware and application code.
- Download the firmware and application code.
- If the problem persists, replace the I/O pack or module.

368

Description Configuration file load error - invalid header size

Possible Cause
During commissioning or maintenance:

- Build error
- Controller EGD revision code not supported
- Incompatible version of I/O pack or module firmware was downloaded

During normal operation:

- There is a hardware failure.

Solution
During commissioning or maintenance:

- Confirm the correct installation of the ToolboxST application.
- Verify that each I/O pack or module is upgraded to the latest version by right-clicking each I/O pack and selecting *Upgrade*.
- Rebuild the application, and download the firmware and application code to the affected I/O pack or module

During normal operation: Replace the I/O pack or module.

369

Description Internal communication error - Exchange [ ] Export failed

Possible Cause Internal runtime error

Solution

- Restart the I/O pack or module.
- Upgrade the I/O pack or module firmware and application code.
- If the problem persists, replace the I/O pack or module.

370

Note This alarm is obsolete.

Description Internal EGD communication error - Exchange [ ] Import failed

Possible Cause Internal runtime error

Solution

- Restart the I/O pack or module.
- Upgrade the I/O pack or module firmware and application code.
- If the problem persists, replace the I/O pack or module.

371

Description IONet-EGD signal inputs are not being updated

Possible Cause
During commissioning or maintenance:

- The I/O pack or module application process is not providing system signal inputs to EGD every frame.

Solution
During commissioning or maintenance:

- Rebuild and download the firmware and application code.
- Verify that the idle time is adequate for the I/O pack or module, and that the frame rate does not exceed defined limits.
- If the problem persists, replace the I/O pack or module.

372

Description Memory Validation failed - Data structures

Possible Cause Hardware memory failure (process data that should not change after the controller goes online was modified)

Solution Replace the I/O pack or module.

373

Description Firmware/IO Configuration Incompatible

Possible Cause I/O pack or module configuration files are incompatible with the firmware (files do not contain necessary revision)

Solution
During commissioning or maintenance:

- Confirm the correct installation of the ToolboxST application.
- Verify that each I/O pack or module is upgraded to the latest version by right-clicking each I/O pack or module and selecting *Upgrade*.
- Rebuild the application, and download the firmware and application code to the affected I/O pack or module.

During normal operation:

- Replace the I/O pack or module.

445

Description Incorrect or Missing Acquisition Board on HSSL link 1

Possible Cause The acquisition board on High Speed Serial Link 1 is not connected or does not agree with the ToolboxST configuration.

Solution

- Verify that the correct acquisition board is connected to the specified HSSL connector on the UCSA.
- Verify that the ToolboxST configuration for the appropriate HSSL connector matches the hardware.

446

Description Incorrect or Missing Acquisition Board on HSSL link 2

Possible Cause The acquisition card on High Speed Serial Link 2 is not connected or does not agree with the ToolboxST configuration.

Solution

- Verify that the correct acquisition card is connected to the specified HSSL connector on the UCSA.
- Verify that the ToolboxST configuration for the appropriate HSSL connector matches the hardware.

447

Description Incorrect or Missing Acquisition Board on HSSL link 3

Possible Cause The acquisition card on High Speed Serial Link 3 is not connected or does not agree with the ToolboxST configuration.

Solution

- Verify that the correct acquisition card is connected to the specified HSSL connector on the UCSA.
- Verify that the ToolboxST configuration for the appropriate HSSL connector matches the hardware.

448

Description Acquisition Board barcode mismatch on HSSL link 1

Possible Cause The barcode on the acquisition card connected to High Speed Serial Link 1 does not agree with those provided in the ToolboxST application

Solution Verify that the correct acquisition card is connected to the link and that the correct barcode has been entered in the ToolboxST application

449

Description Acquisition Board barcode mismatch on HSSL link 2

Possible Cause The barcode on the acquisition card connected to High Speed Serial Link 2 does not agree with those provided in the ToolboxST application

Solution Verify that the correct acquisition card is connected to the link and that the correct barcode has been entered in the ToolboxST application

450

Description Acquisition Board barcode mismatch on HSSL link 3

Possible Cause The barcode on the acquisition card connected to High Speed Serial Link 3 does not agree with those provided in the ToolboxST application

Solution Verify that the correct acquisition card is connected to the link and that the correct barcode has been entered in the ToolboxST application

451

Description Communication Lost on HSSL Link 1

Possible Cause The UCSA can no longer communicate with the acquisition card on High Speed Serial Link 1

Solution Verify that the Ethernet cable is connected and that the acquisition card is healthy.

452

Description Communication Lost on HSSL Link 2

Possible Cause The UCSA can no longer communicate with the acquisition card on High Speed Serial Link 2

Solution Verify that the Ethernet cable is connected and that the acquisition card is healthy.

453

Description Communication Lost on HSSL Link 3

Possible Cause The UCSA can no longer communicate with the acquisition card on High Speed Serial Link 3

Solution Verify that the Ethernet cable is connected and that the acquisition card is healthy.

485

Description Configuration mismatch with Auto-Reconfiguration server

Possible Cause Some or all of the I/O pack or module configuration files do not match those on the Auto-Reconfiguration server

Solution Perform a scan and download using the ToolboxST application

490

Description Software watchdog has been disabled

Possible Cause

- A runtime malfunction has disabled the software watchdog protective function.
- An invalid version of firmware has been downloaded.

Solution

- Reload the base load, firmware, and application code to the I/O pack or module, and restart.
- If failure persists, remove the flash memory from the Mark VIe controller and reprogram the boot loader using the ToolboxST application. Download using the Device | Download | Controller setup | Format Flash selection. After reinstalling the flash memory and restarting, reload the firmware and application code.
- If the problem persists, replace the I/O pack or module or the Mark VIe controller.

491

Description Hardware watchdog has been disabled

Possible Cause

- A runtime malfunction has disabled the hardware watchdog protective function.
- A hardware failure has disabled the hardware watchdog protective function.

Solution

- Reload the firmware and restart the I/O pack or module.
- If the problem persists, replace the I/O pack or module or the Mark VIe controller.

499

Description I/O pack is connected to an unknown board

Possible Cause

- The terminal board or auxiliary terminal board connected to the I/O pack or module is not recognized by this version of firmware.
- This can occur if a new terminal board has been connected but the I/O pack is configured with firmware that does not support the new hardware.

Solution

- Upgrade the ControlST software suite to a version that supports the new hardware.
- Download latest firmware and parameters to the I/O pack or module.

500

Description I/O pack is connected to the wrong terminal board

Possible Cause The I/O pack or module is connected to a recognized terminal board that is not supported.

Solution

- Refer to one of the following system guides for a list of supported hardware combinations: *GEH-6721_Vol_II, GEH-6800,* or *GEH-6779*. From the Start Menu, select *All Programs*, *GE ControlST*, *Documentation*.
- Verify that the I/O pack is connected to a terminal board that is supported.
- Replace the I/O pack or terminal board to create a supported combination.
- Use the ToolboxST application to reconfigure the I/O module.

1008-1010, 1264-1266

Description Outputs unhealthy on IONet [ ] - Message Timeout

Possible Cause

- Controller is rebooting or has rebooted
- Application/configuration does not match in I/O pack or module and controller.
- Failed Ethernet connection between the I/O pack or module and the controller.

Solution

- Reset all diagnostic alarms.
- Rebuild and download the application to all the processors, including I/O packs or modules.
- Reload the firmware and the application.
- Verify that the Ethernet cable on the I/O pack or module matches the ToolboxST configuration.
- Check for a faulty Ethernet cable from the I/O pack or module to the network switch and/or from the switch to the controller. Replace cable(s) if necessary.
- Replace the I/O pack or module.
- Faulty network switch; place the I/O pack or module's Ethernet cable into an empty port. If the problem persists, replace the network switch.

1008-1010, 1264-1266

Description Outputs unhealthy on IONet [ ] - Message Length not valid

Possible Cause Application/configuration does not match in I/O pack or module and controller

Solution

- Rebuild and download the application/parameters to all controllers and I/O packs or modules.
- Reload the firmware and parameters to the affected I/O pack or module.
- Reload the firmware and the application to all controllers.
- If the problem persists, replace affected I/O pack or module, then replace the controller.

1008-1010, 1264-1266

Description Outputs unhealthy on IONet [ ] - Major Signature Mismatch

Possible Cause Application/configuration does not match in I/O pack or module and controller

Solution

- Rebuild and download the application/parameters to all the controllers and I/O packs or modules.
- Reload the firmware and the parameters to the affected I/O pack or module.
- Reload the firmware and the application to all controllers.
- If the problem persists, replace affected I/O pack or module, then replace the controller.

1008-1010, 1264-1266

Description Outputs unhealthy on IONet [ ] - Minor Signature Mismatch

Possible Cause Application/configuration does not match in I/O pack or module and controller

Solution

- Rebuild and download the application/parameters to all the controllers and I/O packs or modules.
- Reload the firmware and the parameters to the affected I/O pack or module.
- Reload the firmware and the application to all the controllers.
- If the problem persists, replace affected I/O pack or module, then replace the controller.

1008-1010, 1264-1266

Description Outputs unhealthy on IONet [ ] - Timestamp Mismatch

Possible Cause Application/configuration does not match in I/O pack or module and controller

Solution

- Rebuild and download the application/parameters to all the controllers and I/O packs or modules.
- Reload the firmware and the parameters to the affected I/O pack or module.
- Reload the firmware and the application to all the controllers.
- If the problem persists, replace affected I/O pack or module, then replace the controller.

Notes

20 Maintenance and Replacement

Warning

This equipment contains a potential hazard of electric shock or burn. Only personnel who are adequately trained and thoroughly familiar with the equipment and the instructions should install, operate, or maintain this equipment.

20.1 Maintenance

Caution

Do not use compressed air to clean the boards. The compressed air may contain moisture that could combine with dirt and dust and damage the boards. If the compressed air pressure is too strong, components could be blown off the boards or delicate solder runs could be damaged.

20.1.1 Terminal Boards and Cables

The control system should be inspected every 30000 hours (3.4 years) to ensure the components are functioning properly. This inspection should include, but is not limited to terminal boards and cables.

- **To clean terminal boards:** remove the dirt and dust from the boards using a grounded, natural bristle drapery brush or paint brush.

- **To clean cables:** remove dirt and dust with a lint free cotton cloth.

20.1.2 Ethernet Switches

The UDH, PDH, and IONet use Fast Ethernet switches preconfigured specifically for the Mark VIe and Mark VIeS control systems. Any replacement switch must also be configured with the appropriate configuration for the controls application. Redundant switches provide multiple communications links to the controllers and HMI systems.

Some basic troubleshooting techniques are useful in the diagnosis and repair of these systems as follows:

In the event of a network link failure, check the status LEDs at both ends of the link. Unlit LEDs indicate a failure in that specific link. Troubleshoot the switch, cable, HMI, or controller by substituting known working Ethernet components until the link status LEDs display health.

On large systems, there may be many switches. It will be necessary to pursue a half-interval (binary search) technique when troubleshooting the network system. This half-interval approach involves isolating different local areas of the network by removing the cables between different areas. These individual areas can then be diagnosed using the method described above. Once all of the individual areas are functioning, they can be connected one at a time until the complete network is restored.

20.1.3 Distributed I/O Heat Exchanger Fans

The Mark VIe distributed I/O wall mount enclosures are industry standard NEMA 4 or NEMA 4X and contain the Mark VIe hardware. The enclosures are typically mounted in close proximity to the field equipment and may be outdoors or in other harsh environments. For this reason, the distributed I/O enclosures are outfitted with air-to-air heat exchanger fans to ensure that Mark VIe control hardware remains within rated operating temperatures.

It is recommended to keep spare fans on hand for quick replacement. The following spare parts (fans, mounting hardware, and finger guards) are required in the event that fans need replacement.

GE Part Number	Description
EBM_6224NU	Heat exchanger fan
103T5502P0001	Fan finger guard
DIN85M4X60-4.8A2J	Fan mounting screws

The heat exchanger fan on the outside of the distributed I/O enclosure should be checked for obstructions. Maintenance should be conducted according to the following table.

Action	Frequency
Check external heat portion of heat exchanger for dirt or debris blocking fans. Clean as necessary.	Every six months or immediately, if high operating temperature diagnostic alarms are reported.
Replace internal and external air circulation fans.	Every four years.

The distributed I/O panel will continue to operate even if one or both of the fans fails. In the event of fan failure, the Mark VIe and Mark VIeS equipment may run at temperatures higher than desired and diagnostic alarms may be generated indicating this condition.

Attention

If diagnostic alarms are generated, the failed component should be replaced as soon as possible without exposing the equipment to inclement weather.

20.2 Replacement

Replacement parts may contain static-sensitive components. Therefore, GE ships replacement parts in anti-static bags. When handling electronics, make sure to store them in anti-static bags or boxes and use a grounding strap (per the following Caution criteria).

Caution

To prevent component damage caused by static electricity, treat all boards with static-sensitive handling techniques. Wear a wrist grounding strap when handling boards or components, but only after boards or components have been removed from potentially energized equipment and are at a normally grounded workstation.

Warning

To prevent personal injury or damage to equipment, follow all GE safety procedures, Lockout Tagout (LOTO), and site safety procedures as indicated by Employee Health and Safety (EHS) guidelines.

Warning

This equipment contains a potential hazard of electric shock, burn, or death. Only personnel who are adequately trained and thoroughly familiar with the equipment and the instructions should install, operate, or maintain this equipment.

Troubleshooting should be done at the system component level. The failed system component (least replaceable part) should be removed, returned to GE, and replaced with a known good spare. Do not attempt to repair system components.

Warning

To prevent electric shock, turn off power to the equipment, then test to verify that no power exists in the board before touching it or any connected circuits.

Caution

To prevent equipment damage, do not remove, insert, or adjust board connections while power is applied to the equipment.

Attention

Replacement of the terminal board requires full reconfiguration of the changed component using the ToolboxST application. For this reason, it is generally preferable to replace only the I/O pack unless the terminal board is known to be the point of failure.

20.2.1 Replacement Procedures

Refer to the following sections for replacement instructions for specific components:

- *PVIB I/O Pack Replacement*
- *YVIB I/O Pack Replacement*
- *PUAA I/O Pack Replacement*
- *SUAA Terminal Board Replacement*
- *UCSB Controller Replacement*
- *UCSA Controller Replacement*
- *UCPA Controller Replacement*

20.2.1.1 Replace Mark VIeS Safety I/O Packs with Same Hardware Form

Attention

Never upgrade the I/O pack firmware to a version that is not supported by the hardware form. Refer to the I/O pack *Compatibility* section of this document for more information.

1. Verify that the replacement I/O pack is compatible with one being replaced.
2. Follow all site safety procedures.
3. Remove the power connector on the side of the I/O pack.
4. Unplug the Ethernet cable(s) and mark their positions.
5. Loosen the two mounting nuts on the I/O pack threaded shafts.
6. Unplug the I/O pack.
7. Plug in the replacement I/O pack. Make sure the I/O pack connector is fully seated on all sides, then properly tighten mounting nuts.
8. Plug the Ethernet and power cables back into the I/O pack.
9. From the ToolboxST application, download the firmware and application code to the new I/O pack.

20.2.1.2 Replace Mark VIeS Safety I/O Packs with Upgraded Hardware Form

Attention

Redundant Safety I/O packs mounted on the same terminal board must all be of the same hardware form, and running the same firmware version.

Do NOT attempt this replacement unless having enough I/O packs with the newer hardware form available, including spares.

It is also recommended to backup the ToolboxST .tcw system file prior to upgrading the system.

Note For YVIBS1B replacement instructions, refer to the procedure provided in the section *YVIB I/O Pack Replacement*.

1. Follow all site safety procedures.
2. Verify that the replacement I/O pack is compatible with one being replaced.
3. Verify that the ControlST* software at site has been upgraded to V06.01 or later.
4. Remove the power connector on the side of the I/O pack(s).
5. Unplug the Ethernet cable(s) and mark their positions.
6. Loosen the two mounting nuts on the I/O pack threaded shafts.
7. Unplug the I/O pack(s).
8. Plug in the replacement I/O pack(s). Make sure the I/O pack connector is fully seated on all sides, then properly tighten mounting nuts.
9. Plug the Ethernet and power cables back into the I/O pack(s) and re-energize the equipment.
10. From the ToolboxST application perform a firmware **Upgrade**. Select the correct firmware revision as listed in the I/O pack *Compatibility* section of this document. This **Upgrade** function loads the correct I/O pack firmware and application to the Mark VIeS Safety controller.
11. From the ToolboxST application, download the firmware and application code to the new I/O pack(s).

20.2.1.3 Replacing a PFFA Linking Device

➢ **To replace a linking device in a redundant set of linking devices**

Attention

PFFAs are not capable of online interaction while the controller is not in the Inputs Enabled or Controlling state. After reboot, if the controller is delayed (such as with a Frame synchronization delay) in achieving the Inputs Enabled state, the PFFA will be offline until the Inputs Enabled state is achieved. This differs from all other I/O packs, which can achieve online communications before the Inputs Enabled state is achieved by a controller.

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1. Identify the defective linking device. Refer to the section *PFFAH1A LEDs* or *PFFAH1B LEDs*, for an indication of the non-operational device.
2. Disconnect the 24 V dc power supply from the linking device by removing the power supply cable.
3. Remove the RS-232 cable (redundancy link) and the Ethernet cable from the linking device.
4. Record the channels (FF 1, FF 2, FF 3, FF 4) where each H1 link is connected, and disconnect each H1 link from the linking device.
5. Remove the old linking device by sliding a screw driver horizontally underneath the housing into the locking bar. Slide the bar downwards without tilting the screwdriver, and fold the linking device upwards.
6. Install the new linking device and record the new Device ID.
7. Plug in the H1 links, ensuring they are installed on the same channels as before.
8. Connect the RS-232 cable and the Ethernet cable.

Note For proper operation, ensure the RS-232 cable is connected prior to plugging in the 24 V dc power cable.

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9. Connect the 24 V dc power cable and turn the power on.
10. Change the configuration in the ToolboxST application to reflect the new Device ID for the PFFA module being replaced, and build and download to the controller.
11. Once the controller has been downloaded successfully, the PFFA startup process and configuration download takes about one minute to complete. Refer to the section *PFFAH1A LEDs* or *PFFAH1B LEDs*, for an indication of the proper operation as a secondary device.

20.2.1.4 PPNG Module Replacement

1. Perform lockout/tagout procedures and isolate the power sources.
2. Disconnect the power connector from the ID assembly.
3. Disconnect the ID assembly from the PPNG.
4. Mark the positions of the Ethernet cables and then unplug them from the PPNG.
5. Loosen the screws holding the PPNG in place. The mounting is a keyhole design. Refer to the figure, *PPNG Envelope and Mounting Dimensions*.
6. Remove the PPNG by lifting to align the large portion of the keyhole with the mounting screws and pull forward.
7. Reinstall the new PPNG by reversing steps 2 through 6.
8. From the ToolboxST application, run the **I/O Pack Setup Wizard** to transfer the PPNG Base Load from the Mark VIe controller to the PPNG. This requires an unencrypted minimum 4 GB USB memory stick or the alternate method uses a serial cable from the COM port. Help for this wizard is available from the ToolboxST application.
9. Configure and download to the new PPNG. Refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6700), the section *PPNG PROFINET Module Configuration*.

20.2.1.5 Replacing Other I/O Packs

Replacement of the terminal board requires full reconfiguration of the changed component using the ToolboxST application. For this reason, it is generally preferable to replace only the I/O pack unless the terminal board is known to be the point of failure.

➢ **To replace an I/O pack**

1. Verify that the replacement I/O pack is compatible with one being replaced.
2. If replacing a BPPB-based I/O pack with a functionally compatible BPPC-based I/O pack:
   a. The site's ControlST* software must be minimum V04.04. Verify the version and upgrade the site if needed.
   b. If needed, download the BPPC I/O Upgrade package from the GE Intelligent Platforms Support website or check the version of ControlST software suite at site to verify that it contains the required I/O pack firmware version.
   c. If needed, install the required I/O pack firmware to the HMI.
   d. From the ToolboxST application, perform an upgrade of the firmware. This modifies the .tcw system file on the HMI. Do this prior to physically replacing the I/O pack hardware. Refer to the *ToolboxST User Guide for Mark Controls Platform* (GEH-6703) for help with this upgrade feature.
3. Lockout tagout the field equipment and isolate the power source.
4. Remove the power to the I/O pack. For the PSVP, turn SW1 on the SSVP to the P28OFF position. For other I/O packs, remove the power plug located in the connector on the side of the I/O pack.
5. Unplug the Ethernet cables and mark the positions of the removed cables.
6. Loosen the two mounting nuts on the I/O pack threaded shafts.
7. Unplug the I/O pack.
8. Plug in the replacement I/O pack. Make sure the I/O pack connector is fully seated on all sides, then properly tighten mounting nuts.
9. Plug the Ethernet and power cables back into the I/O pack and re-energize the equipment.
10. If replacing a BPPB-based I/O pack with a functionally compatible BPPC-based I/O pack: from the ToolboxST application, change the hardware form, build, and download the application code to the Mark VIe controller.
11. If replacing a Mark VIe PCAA: from the ToolboxST application, download the application code to the controller and then download the firmware to the I/O pack (auto-reconfiguration is not available).
12. If replacing a Mark VIe P-pack (not PCAA) and the Auto-Reconfiguration feature is enabled, the Mark VIe controller detects the I/O module running with a different configuration, and a reconfiguration file is automatically downloaded from the controller to the new I/O module.

20.2.1.6 ESWx to ESWx Switch Replacement

➢ **To replace an ESWx switch**

1. Remove the power connector(s) from the ESWx, located on the right side of the switch.
2. Remove the Cat 5e cable connections, recording the port where the cables were installed.
3. Remove the fiber-optic cable connections (if present), recording the port where the cables were installed.
4. Remove the switch module from the panel.
5. If replacing a DIN-rail mounted ESWx, transfer the DIN-rail mounting clip from the failed unit to the replacement unit.
6. If replacing a standard panel mounted ESWx, transfer the mounting bracket from the failed unit to the replacement unit.
7. To interface an existing SC fiber termination to the LC fiber port, connect the port adapter. GE part # 336A5026P01 is required for multi-mode fiber (most common). GE part # 336A5026P02 is required for single-mode fiber.

Port Adapter

8. Mount the replacement switch module into the panel.
9. Reconnect the Cat 5e cables and fiber-optic cables.
10. Reconnect the power connections.

20.2.1.7 Replacing a DACA

➢ **To replace a DACA power conversion module**

1. Remove power from the DACA module. Allow 1 minute for the output voltage to discharge.
2. Remove the power input/output cable (JZ) on the right side of the module top.
3. Remove the four bolts securing the DACA module to the floor of the cabinet.
4. Remove the DACA module.
5. Make note of which receptacle the capacitor power plug is in. This is on the left side of the module top. JTX1 is for 115 V ac and JTX2 is for 230 V ac.
6. Ensure the capacitor power plug is in the same position as the one removed. JTX1 is for 115 V ac and JTX2 is for 230 V ac.
7. Place the new DACA module in the same position as the one removed
8. Secure the DACA module to the cabinet floor with the four bolts removed from the previous module.
9. Install the power input/output plug (JZ) on the right side of the module top
10. Restore power to the DACA module.

20.2.1.8 Replacing D-type Boards

➢ **To replace the board**

1. Lockout and/or tag out the field equipment and isolate the power source.
2. Unplug the I/O cable (J-plugs).
3. Disconnect all field wire and thermocouples along with shield wire.
4. Remove the terminal board and install the new board.
5. Reconnect all field wire and thermocouples as before.
6. Plug the I/O cable (J-plug) back.

20.2.1.9 Replacing J-type Boards

1. Lockout and/or tag out the field equipment and isolate the power source.
2. Check the voltage on each terminal to ensure no voltage is present.
3. Verify the label and unplug all connectors.
4. Loosen the two screws on each of the terminal blocks and remove the top portion leaving all field wiring in place. If necessary, tie the block to the side out of the way.
5. Remove the mounting screws and the terminal board.
6. Install a new terminal board. Check that all jumpers, if applicable, are in the same position as the ones on the old board.
7. Tighten it securely to the cabinet.
8. Replace the top portion of the terminal blocks and secure it with the screws on each end. Ensure all field wiring is secure.
9. Plug in all wiring connectors.

20.2.1.10 Replacing the SSVP

➢ **To replace the board**

1. Lockout and/or tagout the field equipment and isolate the power source.
2. Check the voltage on each terminal to ensure there is no voltage present.
3. Turn SW1 on the SSVP terminal board to the P28OFF position.
4. Remove both the WSVO servo driver module and the PSVP I/O pack.
5. Unplug Ethernet cables from connectors JUA, JLA, JUB and JLB when the PSVP is configured for dual redundancy.
6. Unplug the 2-pin plug from the P28IN Mate-N-Lok® connector on the SSVP.
7. Remove the 24-point connector plug from the TB1 connector on the SSVP.
8. If the DIN-rail base needs to be removed, then remove the grounding screws on the left side of the Din-rail base.

20.2.1.11 Replacing Other S-type Boards

➢ **To replace the S-type terminal board**

1. Perform lockout/tagout procedures and isolate the power sources.
2. Check the voltage on each terminal to ensure that there is no voltage present.
3. Unplug the I/O cable (J-plugs)
4. If applicable, unplug JF1, JF2, and JG1.
5. If applicable, remove the TB3 power cables.
6. If removable terminal block, gently pry the segment of the terminal block containing the field wiring away from the part attached to the terminal board, leaving the wiring in place. If necessary, tie the block to the side out of the way.
7. Remove the mounting screws and terminal board.
8. Install a new terminal board. Check to ensure that all jumpers (if applicable) are in the same position as the ones on the old board.
9. Tighten it securely to the cabinet.
10. If removable terminal block, from the new board, gently pry the segment of the terminal block that would contain the field wiring away from the part attached to the terminal. Then, slide the segment containing the field wiring from the old board into the new terminal block. Ensure that the numbers on the segment with the field wires match the numbers on the terminal block. Press together firmly. Ensure that all field wiring is secure.

20.2.1.12 Replacing a TSVC Terminal Board

➢ **To replace the TSVC**

1. Lockout and/or tagout the field equipment and isolate the power source.
2. Check the voltage on each terminal and ensure no voltage is present.
3. Unplug the 28 V dc cable, J28.
4. Loosen the two screws on the wiring terminal blocks and remove the blocks, leaving the field wiring attached.
5. Unplug the non-isolated excitation outputs, TB3 and TB4.
6. Unplug the external suicide cable from the PPRO for a simplex configuration, if applicable.
7. Unplug the WSVO Servo Driver modules from JR2 (SMX/TMR), JS2 and JT2 (TMR only).
8. Unplug the PSVO I/O packs from JR1 (TMR/SMX), JS1 and JT1 (TMR only).
9. Remove the terminal board and replace it with a spare board, check that all jumpers are set correctly (the same as in the old board).
10. Restore all plug, terminal blocks, modules and I/O packs removed in steps three through eight.

20.2.1.13 Replacing Other T-type Boards

1. Lockout tagout the field equipment and isolate the power source.
2. Check the voltage on each terminal and ensure no voltage is present.
3. Unplug the I/O cable (J-Plugs).
4. If applicable, unplug JF1, JF2, and JG1.
5. If applicable, remove TB3 power cables.
6. Loosen the two screws on the wiring terminal blocks and remove the blocks, leaving the field wiring attached.
7. Remove the terminal board and replace it with a spare board, check that all jumpers are set correctly (the same as in the old board).
8. Screw the terminal blocks back in place and plug in the J-plugs and connect cable to TB3 as before.

20.2.1.14 Replacing Fuses

➢ **To replace a fuse**

1. Lockout and/or tagout the field equipment and follow all equipment and site safety guidelines including use of safety glasses and any additional PPE.
2. Using a flat blade screwdriver, twist the fuse holder cap 1/8 turn counter-clockwise.
3. Remove the fuse and cap from the circuit board mounted holder.
4. Remove the old fuse from the fuse holder cap.
5. Inspect the new fuse to verify that the fuse being replaced has the same voltage, current, and interrupting current (IC) ratings. Confirm that this rating matches the specification for the board or values provided in the application system elementary. There is also a table in GEH-6721_Vol_I that lists fuses and terminal boards.
6. Insert the new fuse into the fuse holder cap in the same orientation as the one removed.
7. Place the fuse and cap into the fuse holder. Using the flat blade screwdriver, quickly push-in and twist 1/8 turn clockwise.

Note If the fuse opening fault condition has not been removed, you may fail the new fuse when it is inserted into the holder.

20.2.1.15 Replacing Heat Exchanger Fans

➢ **To replace a distributed I/O heat exchanger fan**

1. Open the electronics enclosure and turn off the ac power breaker located in the lower left corner of the cabinet. Lockout and/or tagout the breaker per local site requirements.
2. Disconnect the fan wiring from the fan power supply. The fan power supply is attached to the left side wall just below the internal heat exchanger fan.
3. Remove the mounting screws attaching the fan to the heat exchanger and remove the fan. The mounting screws and fan finger guard should be retained for use on the new fan.
4. Attach the replacement fan with finger guard to the heat exchanger using the original mounting screws (or equivalent M4 x 60 mm hardware). For external fans, it is necessary to cover the fan lead wires in heat shrink tubing to ensure proper sealing of the enclosure side wall gland seal.
5. Connect the fan wiring to the fan power supply with the following fan wire polarity: Red = Positive; Blue = Negative.
6. Unlock the ac breaker and re-energize the ac circuit.

20.3 Ordering Parts

Renewals and spares (or those not under warranty) should be ordered by contacting the nearest GE Sales or Service Office, or an authorized GE Sales Representative.

Prior to ordering a replacement part:

- Determine if the part is under warranty
- Identify the part
- Refer to the *Mark VIe and Mark VIeS Control System Volume I: System Guide* (GEH-6721_Vol_I), the section *Component Part Numbers*.

Control system electronics are identified by a 12-character alphanumeric part number and a single revision letter. When ordering, be sure to include the complete part number and revision letter. All digits are important when ordering or replacing any device. The factory may substitute newer versions based on availability and design enhancements, however, GE ensures backward compatibility of replacements.

Notes